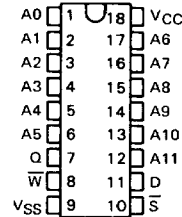


- Single +5-V Supply ( $\pm 10\%$  Tolerance)
- High Density 300-mil (7.62 mm) 18-Pin Package
- Fully Static Operation (No Clocks, No Refresh, No Timing Strobe)
- 4 Performance Ranges:

TMS4044/TMS40L44 . . . NL PACKAGE  
(TOP VIEW)



ACCESS READ OR WRITE

	TIME (MAX)	CYCLE (MIN)
TMS4044-12, TMS40L44-12	120 ns	120 ns
TMS4044-20, TMS40L44-20	200 ns	200 ns
TMS4044-25, TMS40L44-25	250 ns	250 ns
TMS4044-45, TMS40L44-45	450 ns	450 ns

- 400-mV Guaranteed DC Noise Immunity with Standard TTL Loads - No Pull-Up Resistors Required
- Common I/O Capability
- 3-State Outputs and Chip Select Control for OR-Tie Capability
- Fan-Out to 2 Series 74, 1 Series 74S, or 8 Series 74LS TTL Loads
- Low Power Dissipation

	MAX (OPERATING)	MAX (STANDBY)
TMS4044	303 mW	84 mW
TMS40L44	220 mW	60 mW

PIN NOMENCLATURE	
A0 - A11	Addresses
D	Data In
Q	Data Out
$\bar{S}$	Chip Select
VCC	+5-V Supply
VSS	Ground
W	Write Enable

description

This series of static random-access memories is organized as 4096 words of 1 bit. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. Because this series is fully static, chip select may be tied low to further simplify system timing. Output data is always available during a read cycle.

All inputs and outputs are fully compatible with Series 74, 74S or 74LS TTL. No pull-up resistors are required. This 4K Static RAM series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship. All versions are characterized to retain data at  $V_{CC} = 2.4$  V to reduce power dissipation.

The TMS4044/40L44 series is offered in the 18-pin dual-in-line plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil (7.62 mm) centers. The series is guaranteed for operation from 0°C to 70°C.

# TMS4044, TMS40L44

## 4096-WORD BY 1-BIT STATIC RAMS

### operation

#### addresses (A0-A11)

The twelve address inputs select one of the 4096 storage locations in the RAM. The address inputs must be stable for the duration of a write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

#### chip select ( $\bar{S}$ )

The chip-select terminal, which can be driven directly from standard TTL circuits, affects the data-in and data-out terminals. When chip select is at a logic low level, both terminals are enabled. When chip select is high, data-in is inhibited and data-out is in the floating or high-impedance state.

#### write enable ( $\bar{W}$ )

The read or write mode is selected through the write enable terminal. A logic high selects the read mode; a logic low selects the write mode.  $\bar{W}$  must be high when changing addresses to prevent erroneously writing data into a memory location. The  $\bar{W}$  input can be driven directly from standard TTL circuits.

#### data-in (D)

Data can be written into a selected device when the write enable input is low. The data-in terminal can be driven directly from standard TTL circuits.

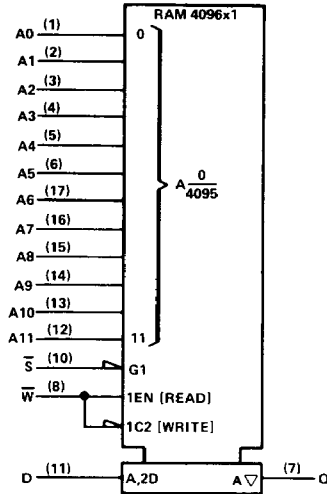
#### data-out (Q)

The three-state output buffer provides direct TTL compatibility with a fan-out of two Series 74 TTL gates, one Series 74S TTL gate, or eight Series 74LS TTL gates. The output is in the high-impedance state when chip select ( $\bar{S}$ ) is high or whenever a write operation is being performed, facilitating device operation in common I/O systems. Data-out is the same polarity as data-in.

### standby operation

The standby mode, which will retain data while reducing power consumption, is attained by reducing the  $V_{CC}$  supply from 5 volts to 2.4 volts. When reducing supply voltage during the standby mode,  $\bar{S}$  and  $\bar{W}$  must be high to retain data. The  $V_{CC}$  transition rate should not exceed 26 mV/ms. During standby operation, data can not be read or written into the memory. When resuming normal operation, five cycle times must be allowed after normal supplies are returned for the memory to resume steady state operation conditions.

logic symbol †



FUNCTION TABLE

INPUTS		OUTPUT	MODE
S̄	W̄	Q	
H	X	HI-Z	DEVICE DISABLED
L	L	HI-Z	WRITE
L	H	DATA OUT	READ

† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating free-air temperature (unless otherwise noted) †

Supply voltage, $V_{CC}$ (see Note 1)	-0.5 V to 7 V
Input voltage (any input) (see Note 1)	-1 V to 7 V
Continuous power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-55°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT	
Supply voltage, $V_{CC}$	TMS4044-12	Operating	4.5	5	5.5	V
	TMS40L44-12	Standby	2.4		5.5	
	TMS4044-20	Operating	4.5		5.5	
	TMS40L44-20	Standby	2.4		5.5	
	TMS4044-25	Operating	4.5		5.5	
	TMS40L44-25	Standby	2.4		5.5	
	TMS40L44-45	Operating	4.5		5.5	
Supply voltage, $V_{SS}$			0		V	
High-level input voltage, $V_{IH}$		2		5.5	V	
Low-level input voltage, $V_{IL}$ (see Note 2)		-1		0.8	V	
Operating free-air temperature, $T_A$		0		70	°C	

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

**TMS4044, TMS40L44**  
**4096-WORD BY 1-BIT STATIC RAMS**

Static RAM and Memory Support Devices

electrical characteristics over recommended operating free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 4.5 V	2.4			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 3.2 mA	V <sub>CC</sub> = 4.5 V			0.4	V
I <sub>I</sub>	Input current	V <sub>I</sub> = 0 V to 5.5 V				10	μA
I <sub>OZ</sub>	Off-state output current	S at 2 V or W at 0.8 V V <sub>O</sub> = 0 V to 5.5 V				± 10	μA
I <sub>CC</sub>	Supply current from V <sub>CC</sub>	I <sub>O</sub> = 0 mA T <sub>A</sub> = 0°C (worst case)	TMS40L44	V <sub>CC</sub> = MAX	25	40	mA
				V <sub>CC</sub> = 2.4 V	15	25	
			TMS4044-12	V <sub>CC</sub> = MAX	50	55	
			TMS4044-20	V <sub>CC</sub> = 2.4 V	25	35	
			TMS4044-25	V <sub>CC</sub> = MAX	50	55	
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = 0 V, f = 1 MHz				8	pF
C <sub>o</sub>	Output capacitance	V <sub>O</sub> = 0 V, f = 1 MHz				8	pF

†All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

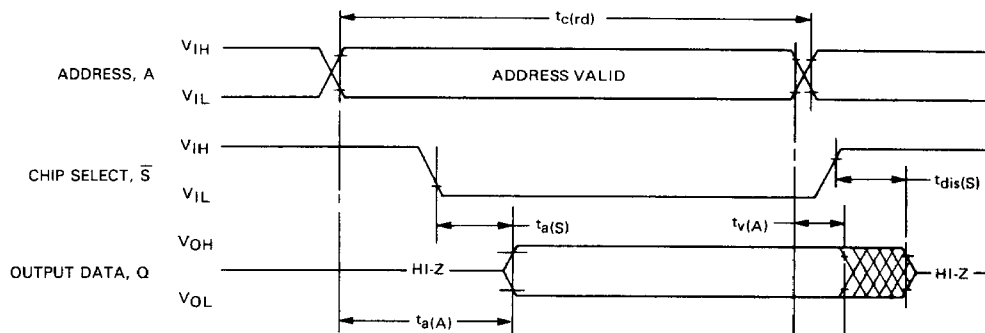
timing requirements over recommended supply voltage range, T<sub>A</sub> = 0°C to 70°C, 1 Series 74 TTL load, C<sub>L</sub> = 100 pF

PARAMETER	TMS4044-12		TMS4044-20		TMS4044-25		TMS4044-45		UNIT
	TMS40L44-12		TMS40L44-20		TMS40L44-25		TMS40L44-45		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>c(rd)</sub>	Read cycle time		120	200	250	450			ns
t <sub>c(wr)</sub>	Write cycle time		120	200	250	450			ns
t <sub>v(W)</sub>	Address valid to end of write		110	180	230	230			ns
t <sub>w(W)</sub>	Write pulse width		60	60	75	200			ns
t <sub>su(A)</sub>	Address set up time		0	0	0	0			ns
t <sub>su(S)</sub>	Chip select set up time		60	60	75	200			ns
t <sub>su(D)</sub>	Data set up time		50	60	75	200			ns
t <sub>h(D)</sub>	Data hold time		0	0	0	0			ns
t <sub>h(A)</sub>	Address hold time		0	0	0	0			ns

switching characteristics over recommended voltage range,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ , 1 Series 74 TTL load,  $C_L = 100$  pF

PARAMETER	TMS4044-12		TMS4044-20		TMS4044-25		TMS4044-45		UNIT
	TMS40L44-12		TMS40L44-20		TMS40L44-25		TMS40L44-45		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_a(A)$ Access time from address	120		200		250		450		ns
$t_a(S)$ Access time from chip select low	70		70		100		100		ns
$t_a(W)$ Access time from write enable high	70		70		100		100		ns
$t_v(A)$ Output data valid after address change	20		20		20		20		ns
$t_{dis(S)}$ Output disable time after chip select high	50		60		60		80		ns
$t_{dis(W)}$ Output disable time after write enable low	50		60		60		80		ns

read cycle timing (see Note 3)

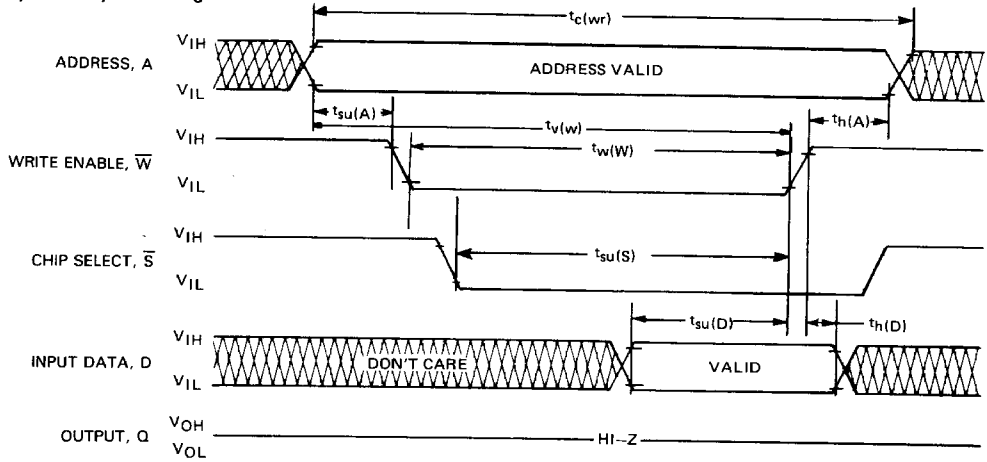


All timing reference points are 0.8 V and 2.0 V on inputs and 0.6 V and 2.2 V on outputs (90% points). Input rise and fall times = 10 ns.

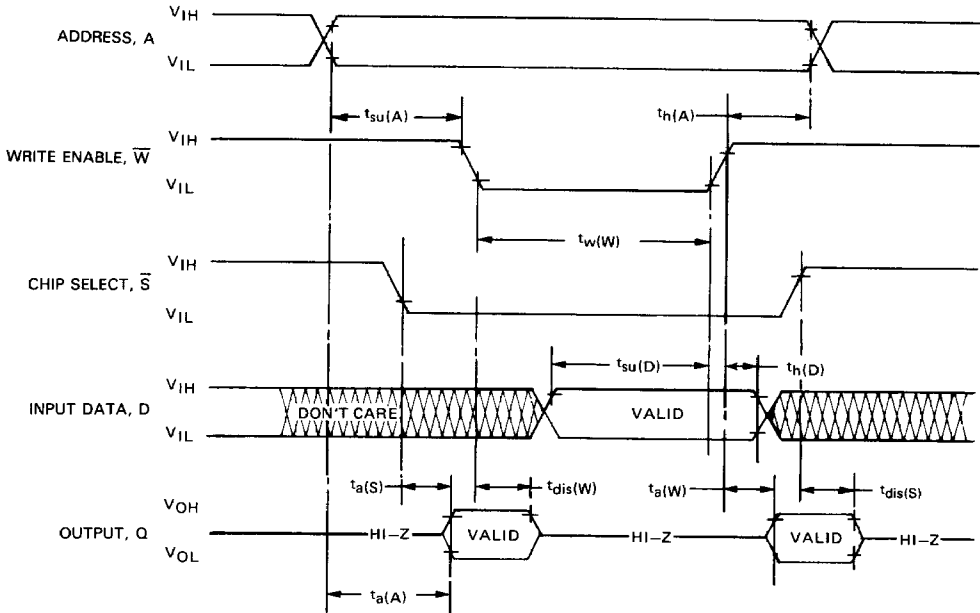
NOTE 3. Write enable is high for a read cycle.

**TMS4044, TMS40L44**  
**4096-WORD BY 1-BIT STATIC RAMS**

**early write cycle timing**



**read-write cycle timing**



Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.