

Dual NPN General Purpose Amplifier Transistor

EMX1DXV6T1G, EMX1DXV6T5G

This NPN transistor is designed for general purpose amplifier applications. This device is housed in the SOT-563 package which is designed for low power surface mount applications, where board space is at a premium.

Features

- Reduces Board Space
- High h_{FE} , 210–460 (Typical)
- Low $V_{CE(sat)}$, < 0.5 V
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{(BR)CBO}$	60	Vdc
Collector-Emitter Voltage	$V_{(BR)CEO}$	50	Vdc
Emitter-Base Voltage	$V_{(BR)EBO}$	7.0	Vdc
Collector Current – Continuous	I_C	100	mAdc

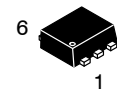
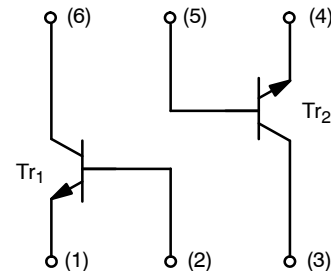
THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	357 (Note 1) 2.9 (Note 1)	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	350 (Note 1)	$^\circ\text{C}/\text{W}$
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	500 (Note 1) 4.0 (Note 1)	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	250 (Note 1)	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

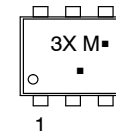
1. FR-4 @ Minimum Pad

DUAL NPN GENERAL PURPOSE AMPLIFIER TRANSISTORS SURFACE MOUNT



SOT-563
CASE 463A
STYLE 1

MARKING DIAGRAM



3X = Specific Device Code
M = Month Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

EMX1DXV6T1G, EMX1DXV6T5G

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage (I _C = 50 μAdc, I _E = 0)	V _{(BR)CBO}	60	-	-	Vdc
Collector-Emitter Breakdown Voltage (I _C = 1.0 mAdc, I _B = 0)	V _{(BR)CEO}	50	-	-	Vdc
Emitter-Base Breakdown Voltage (I _E = 50 μAdc, I _C = 0)	V _{(BR)EBO}	7.0	-	-	Vdc
Collector-Base Cutoff Current (V _{CB} = 60 Vdc, I _E = 0)	I _{CBO}	-	-	0.5	μA
Emitter-Base Cutoff Current (V _{EB} = 7.0 Vdc, I _B = 0)	I _{EBO}	-	-	0.5	μA
Collector-Emitter Saturation Voltage (Note 2) (I _C = 50 mAdc, I _B = 5.0 mAdc)	V _{CE(sat)}	-	-	0.4	Vdc
DC Current Gain (Note 3) (V _{CE} = 6.0 Vdc, I _C = 1.0 mAdc)	h _{FE}	120	-	560	-
Transition Frequency (V _{CE} = 12 Vdc, I _C = 2.0 mAdc, f = 30 MHz)	f _T	-	180	-	MHz
Output Capacitance (V _{CB} = 12 Vdc, I _C = 0 Adc, f = 1 MHz)	C _{OB}	-	2.0	-	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Device mounted on a FR-4 glass epoxy printed circuit board using the minimum recommended footprint.

3. Pulse Test: Pulse Width ≤ 300 μs, D.C. ≤ 2%.

ORDERING INFORMATION

Device	Package	Shipping [†]
EMX1DXV6T1G, NSVEMX1DXV6T1G	SOT-563 (Pb-Free)	4000 Units / Tape & Reel
EMX1DXV6T5G	SOT-563 (Pb-Free)	8000 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

EMX1DXV6T1G, EMX1DXV6T5G

TYPICAL ELECTRICAL CHARACTERISTICS

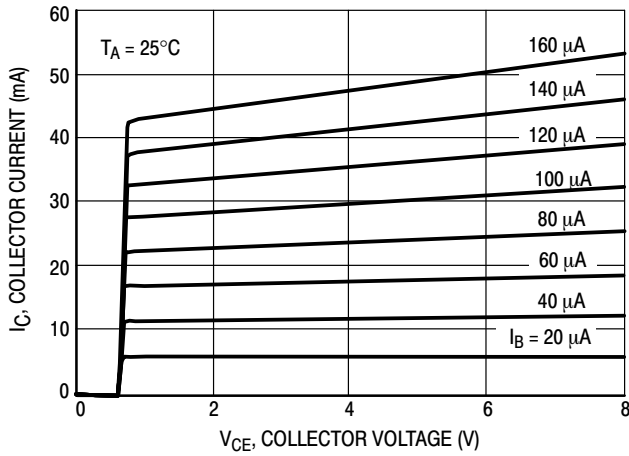


Figure 1. $I_C - V_{CE}$

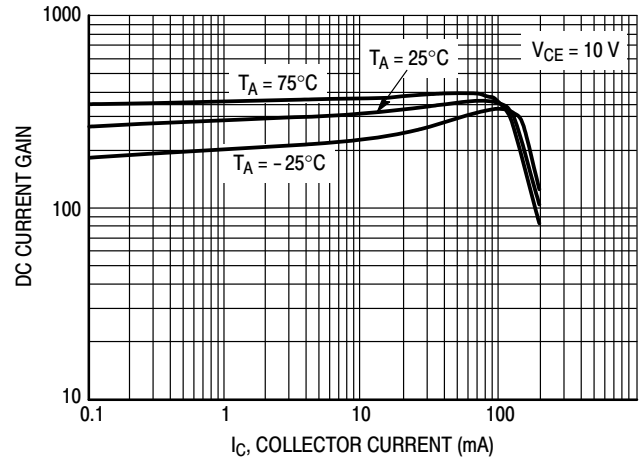


Figure 2. DC Current Gain

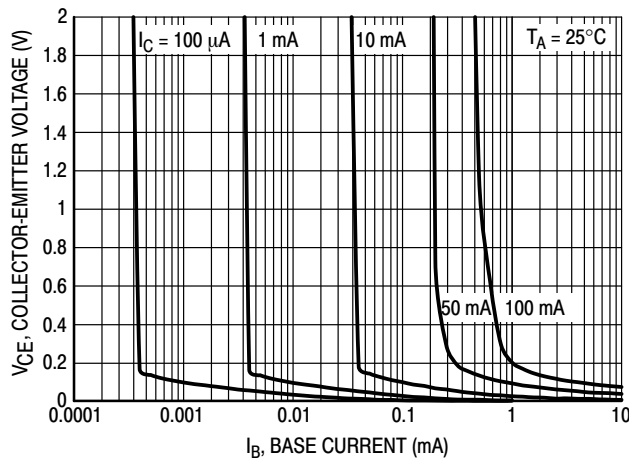


Figure 3. Collector Saturation Region

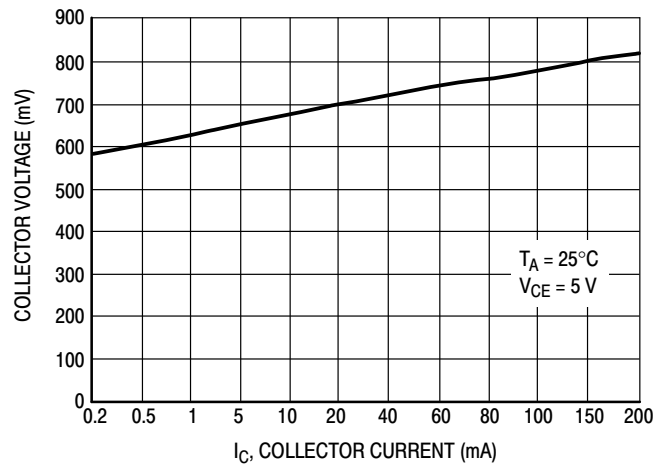


Figure 4. On Voltage

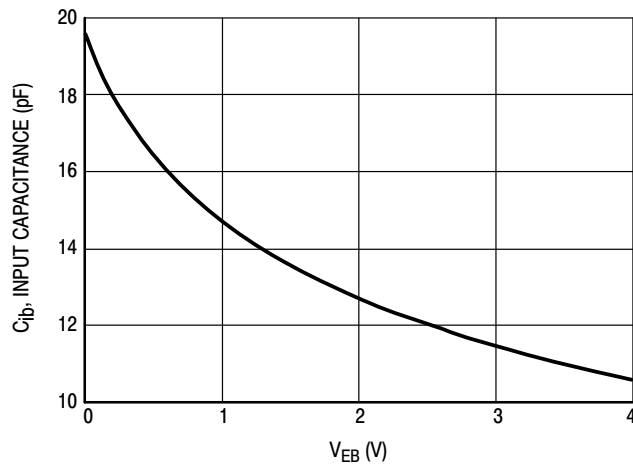


Figure 5. Capacitance

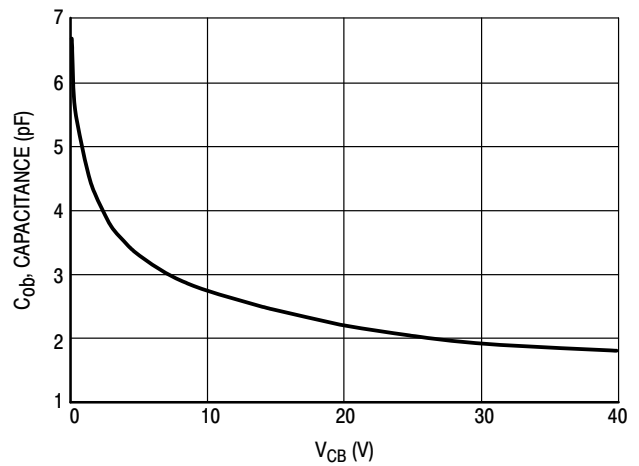


Figure 6. Capacitance

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



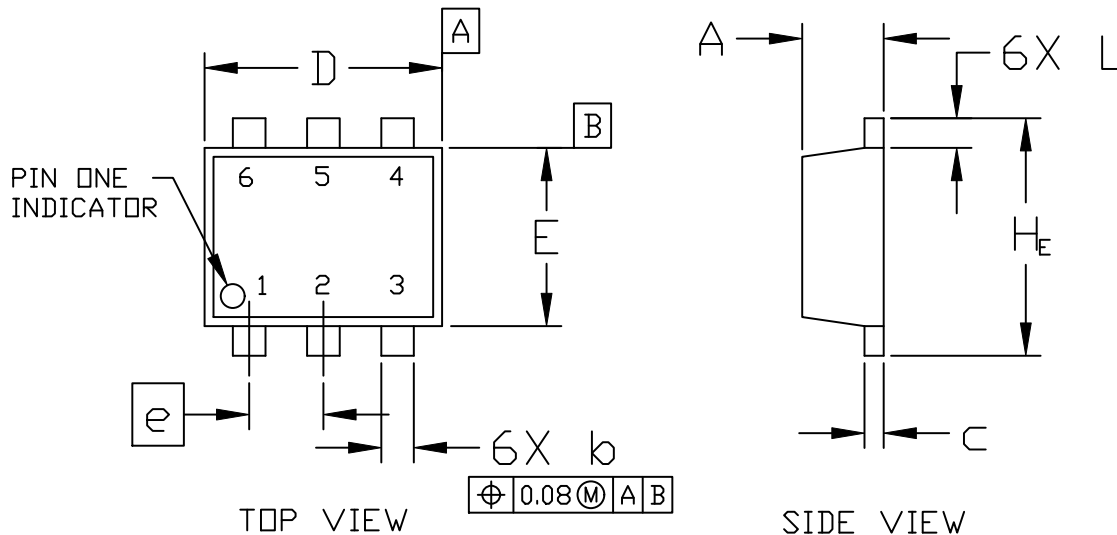
SCALE 4:1

SOT-563, 6 LEAD
CASE 463A
ISSUE H

DATE 26 JAN 2021

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.50	1.60	1.70
E	1.10	1.20	1.30
e	0.50 BSC		
L	0.10	0.20	0.30
H _E	1.50	1.60	1.70

RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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SOT-563, 6 LEAD
CASE 463A
ISSUE H

DATE 26 JAN 2021

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

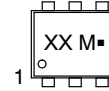
STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

**GENERIC
MARKING DIAGRAM***



XX = Specific Device Code
M = Month Code
■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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