

## DM7490A, DM7493A Decade and Binary Counters

### General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 90A and divide-by-eight for the 93A.

All of these counters have a gated zero reset and the 90A also has gated set-to-nine inputs for use in BCD nine's complement applications.

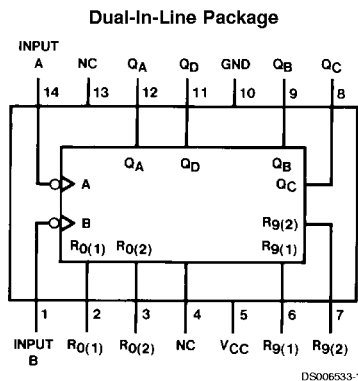
To use their maximum count length (decade or four-bit binary), the B input is connected to the  $Q_A$  output. The input count pulses are applied to input A and the outputs are as

described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 90A counters by connecting the  $Q_D$  output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output  $Q_A$ .

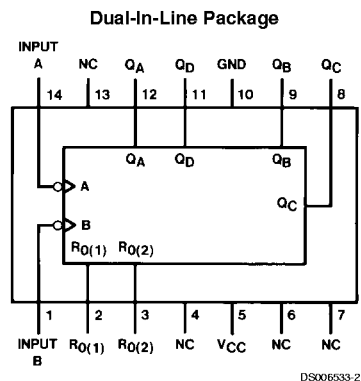
### Features

- Typical power dissipation
  - 90A 145 mW
  - 93A 130 mW
- Count frequency 42 MHz

### Connection Diagrams



Order Number DM5490J, DM5490W  
or DM7490AN  
See Package Number J14A, N14A or W14B



Order Number DM7493AN  
See Package Number N14A

## Absolute Maximum Ratings (Note 1)

Supply Voltage	7V	DM54	-55°C to +125°C
Input Voltage	5.5V	DM74	0°C to +70°C
Operating Free Air Temperature Range		Storage Temperature Range	-65°C to +150°C

## Recommended Operating Conditions

Symbol	Parameter	DM5490			DM7490A			Units
		Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			2			V
V <sub>IL</sub>	Low Level Input Voltage			0.8			0.8	V
I <sub>OH</sub>	High Level Output Current			-0.8			-0.8	mA
I <sub>OL</sub>	Low Level Output Current			16			16	mA
f <sub>CLK</sub>	Clock Frequency (Note 6)	A	0	32	0		32	MHz
		B	0	16	0		16	
t <sub>w</sub>	Pulse Width (Note 6)	A	15		15			ns
		B	30		30			
		Reset	15		15			
t <sub>REL</sub>	Reset Release Time (Note 6)	25			25			ns
T <sub>A</sub>	Free Air Operating Temperature	-55		125	0		70	°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## '90A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = -12 mA			-1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	2.4	3.4		V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IH</sub> = Min, V <sub>IL</sub> = Max (Note 5)		0.2	0.4	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max V <sub>I</sub> = 2.7V	A		80	μA
			Reset		40	
			B		120	
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max V <sub>I</sub> = 0.4V	A		-3.2	mA
			Reset		-1.6	
			B		-4.8	
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 3)	DM54	-20	-57	mA
			DM74	-18	-57	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 4)		29	42	mA

**Note 2:** All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

**Note 3:** Not more than one output should be shorted at a time.

**Note 4:** I<sub>CC</sub> is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

**Note 5:** Q<sub>A</sub> outputs are tested at I<sub>OL</sub> = Max plus the limit value of I<sub>IL</sub> for the B input. This permits driving the B input while maintaining full fan-out capability.

**Note 6:** T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

## '90A Switching Characteristics

at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$ $C_L = 15\text{ pF}$		Units
			Min	Max	
$f_{MAX}$	Maximum Clock Frequency	A to $Q_A$	32		MHz
		B to $Q_B$	16		
$t_{PLH}$	Propagation Delay Time Low to High Level Output	A to $Q_A$		16	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	A to $Q_A$		18	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	A to $Q_D$		48	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	A to $Q_D$		50	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	B to $Q_B$		16	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	B to $Q_B$		21	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	B to $Q_C$		32	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	B to $Q_C$		35	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	B to $Q_D$		32	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	B to $Q_D$		35	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	SET-9 to $Q_A, Q_D$		30	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	SET-9 to $Q_B, Q_C$		40	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	SET-0 Any Q		40	ns

## Recommended Operating Conditions

Symbol	Parameter		DM7493A			Units
			Min	Nom	Max	
$V_{CC}$	Supply Voltage		4.75	5	5.25	V
$V_{IH}$	High Level Input Voltage		2			V
$V_{IL}$	Low Level Input Voltage				0.8	V
$I_{OH}$	High Level Output Current				-0.8	mA
$I_{OL}$	Low Level Output Current				16	mA
$f_{CLK}$	Clock Frequency (Note 11)	A	0		32	MHz
		B	0		16	
$t_w$	Pulse Width (Note 11)	A	15			ns
		B	30			
		Reset	15			
$t_{REL}$	Reset Release Time (Note 11)		25			ns
$T_A$	Free Air Operating Temperature		0		70	$^\circ C$

## '93A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 7)	Max	Units
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -12 \text{ mA}$			-1.5	V
$V_{OH}$	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	2.4	3.4		V
$V_{OL}$	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IH} = \text{Min}, V_{IL} = \text{Max}$ (Note 10)		0.2	0.4	V
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5\text{V}$			1	mA
$I_{IH}$	High Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.4\text{V}$	Reset		40	$\mu\text{A}$
			A		80	
			B		80	
$I_{IL}$	Low Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.4\text{V}$	Reset		-1.6	mA
			A		-3.2	
			B		-3.2	
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 8)	-18		-57	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$ (Note 9)		26	39	mA

Note 7: All typicals are at  $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$ .

Note 8: Not more than one output should be shorted at a time.

Note 9:  $I_{CC}$  is measured with all outputs open, both R0 inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 10:  $Q_A$  outputs are tested at  $I_{OL} = \text{Max}$  plus the limit value of  $I_{IL}$  for the B input. This permits driving the B input while maintaining full fan-out capability.

Note 11:  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

## '93A Switching Characteristics

at  $V_{CC} = 5\text{V}$  and  $T_A = 25^\circ\text{C}$

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$ $C_L = 15 \text{ pF}$		Units
			Min	Max	
$f_{MAX}$	Maximum Clock Frequency	A to $Q_A$	32		MHz
		B to $Q_B$	16		
$t_{PLH}$	Propagation Delay Time Low to High Level Output	A to $Q_A$		16	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	A to $Q_A$		18	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	A to $Q_D$		70	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	A to $Q_D$		70	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	B to $Q_B$		16	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	B to $Q_B$		21	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	B to $Q_C$		32	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	B to $Q_C$		35	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	B to $Q_D$		51	ns

### '93A Switching Characteristics (Continued)

at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$ $C_L = 15\text{ pF}$		Units
			Min	Max	
$t_{PHL}$	Propagation Delay Time High to Low Level Output	B to $Q_D$		51	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40	ns

### Function Tables (Note 15)

#### 90A BCD Count Sequence

(Note 12)

Count	Outputs			
	$Q_D$	$Q_C$	$Q_B$	$Q_A$
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

#### 93A Count Sequence

(Note 14)

Count	Outputs			
	$Q_D$	$Q_C$	$Q_B$	$Q_A$
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

#### 90A BCD Bi-Quinary (5-2)

(Note 13)

Count	Outputs			
	$Q_A$	$Q_D$	$Q_C$	$Q_B$
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

**Function Tables** (Note 15) (Continued)

**90A  
Reset/Count Function Table**

Reset Inputs				Outputs			
R0(1)	R0(2)	R9(1)	R9(2)	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

**93A  
Reset/Count Function Table**

Reset Inputs		Outputs			
R0(1)	R0(2)	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

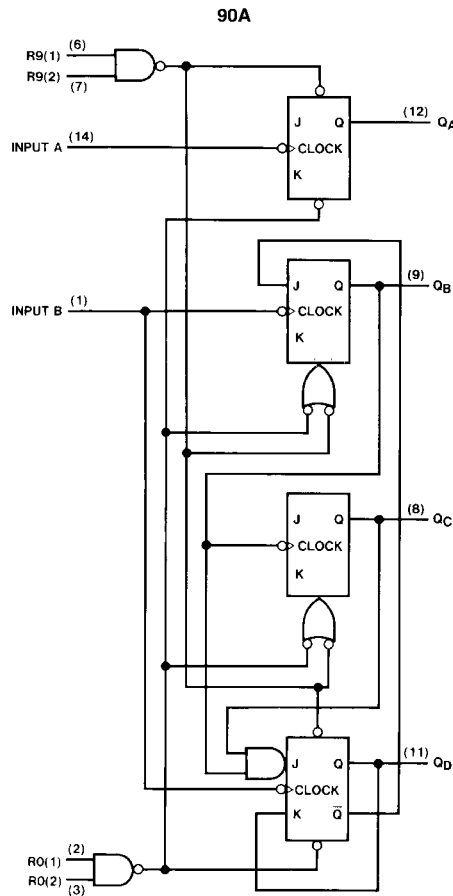
**Note 12:** Output Q<sub>A</sub> is connected to input B for BCD count.

**Note 13:** Output Q<sub>D</sub> is connected to input A for bi-quinary count.

**Note 14:** Output Q<sub>A</sub> is connected to input B.

**Note 15:** H = High Level, L = Low Level, X = Don't Care.

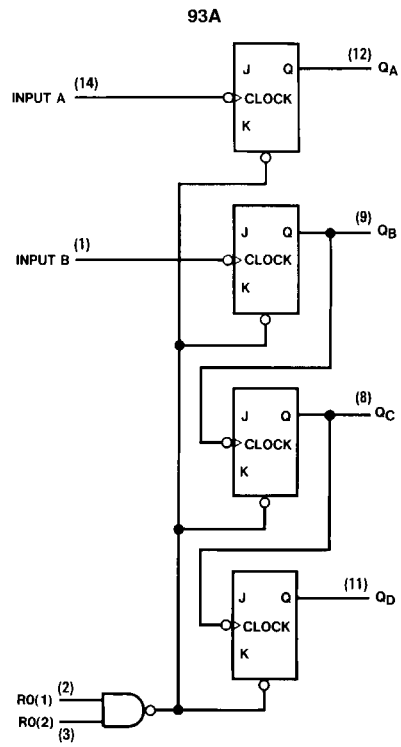
**Logic Diagrams**



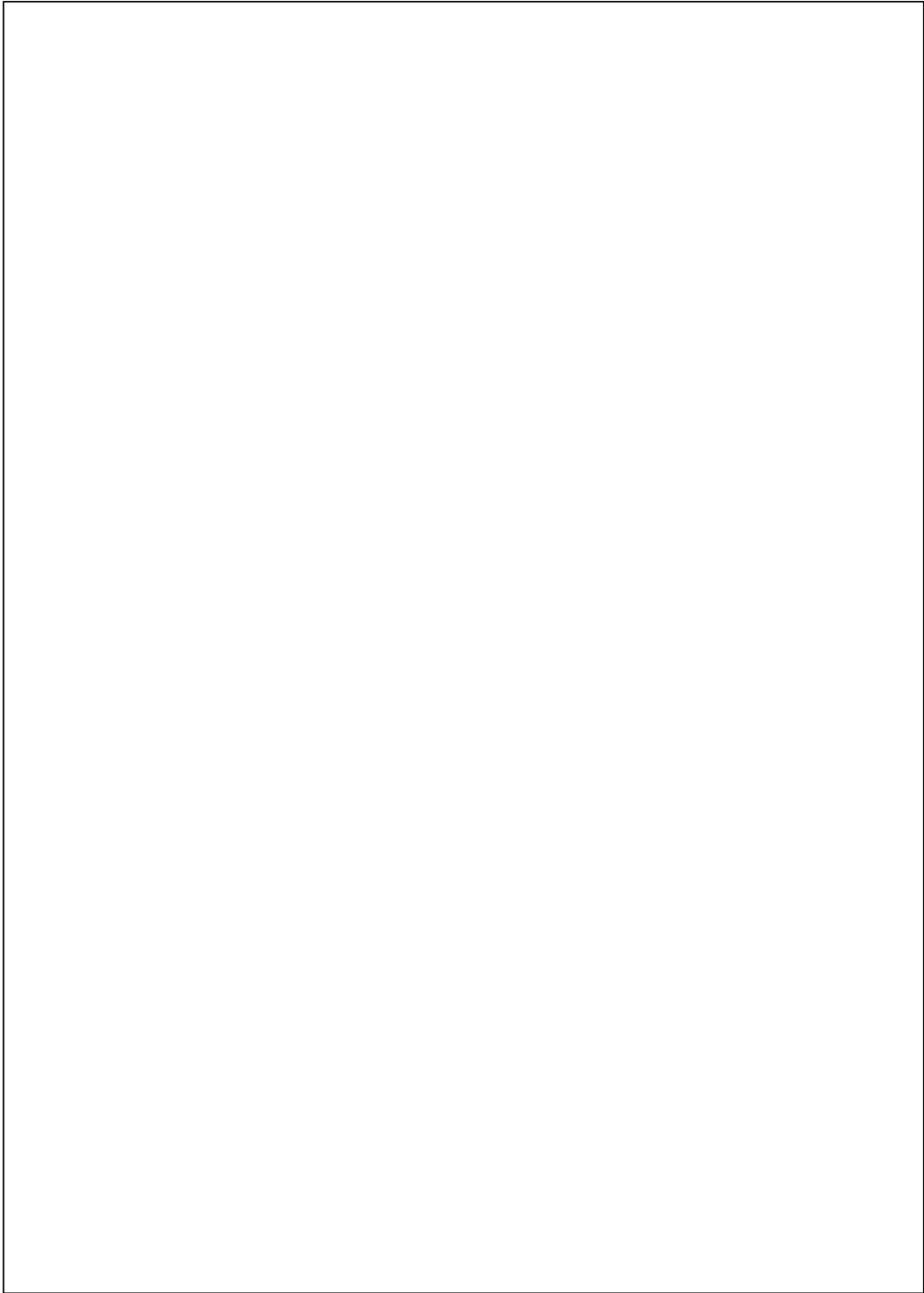
DS006533-3

The J and K inputs shown without connection are for reference only and are functionally at a high level.

# Logic Diagrams (Continued)



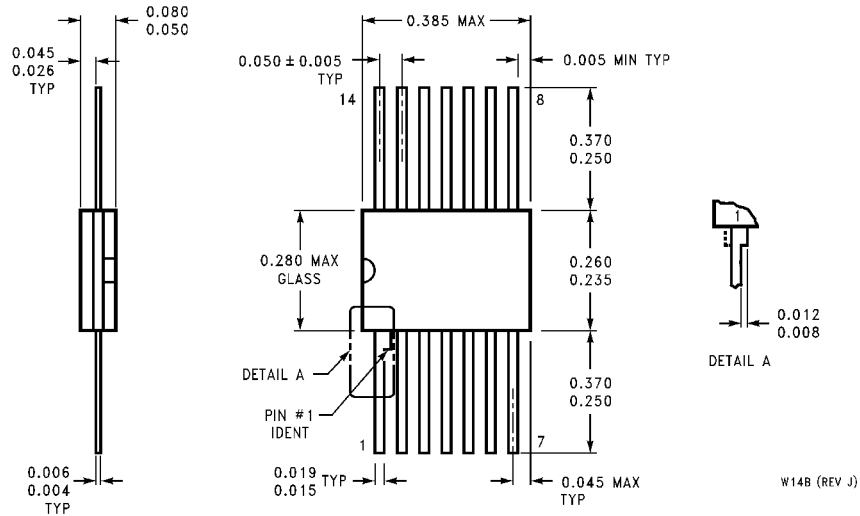
DS006533-4







**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**14-Lead Ceramic Flat Package (W)**  
**Order Number DM5490W**  
**Package Number W14B**

W14B (REV J)

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Corporation  
 Americas  
 Customer Response Center  
 Tel: 1-888-522-5372

Fairchild Semiconductor Europe  
 Fax: +49 (0) 1 80-530 85 86  
 Email: europe.support@nsc.com  
 Deutsch Tel: +49 (0) 8 141-35-0  
 English Tel: +44 (0) 1 793-85-68-56  
 Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.  
 13th Floor, Straight Block,  
 Ocean Centre, 5 Canton Rd.  
 Tsimshatsui, Kowloon  
 Hong Kong  
 Tel: +852 2737-7200  
 Fax: +852 2314-0061

National Semiconductor Japan Ltd.  
 Tel: 81-3-5620-6175  
 Fax: 81-3-5620-6179

www.fairchildsemi.com