Quad Voltage Monitor and Sequencer

ADM1185

FEATURES

- Powered from 2.7 V to 5.5 V on the VCC pin
- Monitors 4 supplies via 0.8% accurate comparators
- Logical core with internal timeouts provides power supply sequencing and fault protection
- 4 inputs can be programmed to monitor different voltage levels with resistor dividers
- 3 open-drain enable outputs
- Open-drain power-good output (PWRGD)
- 10-lead MSOP

APPLICATIONS

- Monitor and alarm functions
- Power supply sequencing
- Telecommunication and data communication equipment
- PCs/servers

FUNCTIONAL BLOCK DIAGRAM

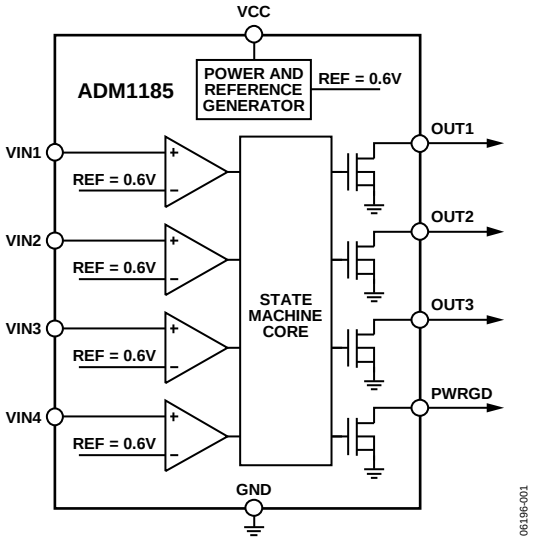

Figure 1.

GENERAL DESCRIPTION

The ADM1185 is an integrated, 4-channel, voltage monitoring and sequencing device. A 2.7 V to 5.5 V power supply is required on the VCC pin to power the device.

Four precision comparators monitor four voltage rails. All comparators have a 0.6 V reference with a worst-case accuracy of 0.8%. Resistor networks that are external to the VIN1, VIN2, VIN3, and VIN4 pins set the trip points for the monitored supply rails.

A digital core interprets the status of the comparator outputs.

Internal time delays can be used for sequencing the startup of subsequent power supplies enabled by the outputs. Supplies falling out of range are also detected and, as a result, appropriate outputs are disabled.

The ADM1185 has four open-drain outputs. In a typical configuration, OUT1 to OUT3 are used to enable power supplies, while PWRGD is a common power-good output, indicating the status of all monitored supplies.

The ADM1185 is available in a 10-lead mini small outline package (MSOP).

APPLICATIONS DIAGRAM

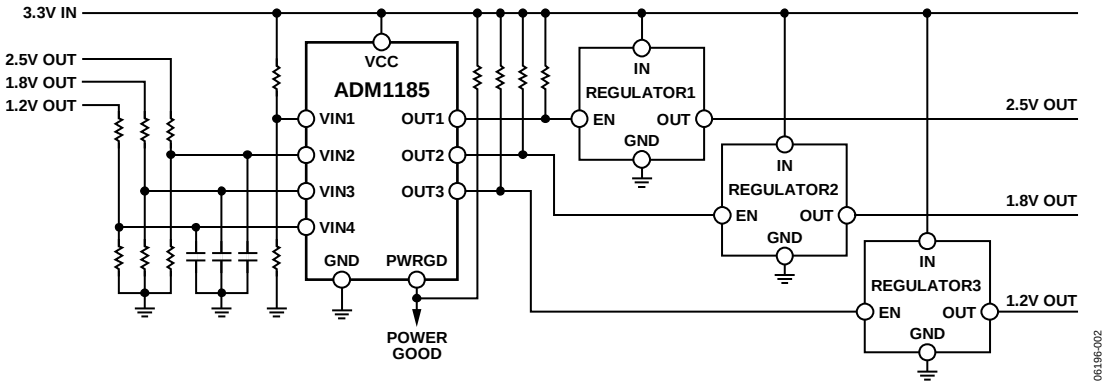

Figure 2.

Rev. B

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REVISION HISTORY

4/09—Rev. A to Rev. B

Changes to Input Rising Threshold, V_{THR} Parameter, Table 1 3

11/07—Rev. 0 to Rev. A

Changes to Table 5 9
Changes to Figure 20 and Figure 21 11

3/07—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 2.7 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions
VCC PIN					
Operating Voltage Range, V_{CC}	2.7	3.3	5.5	V	
Supply Current, I_{VCC}		24	80	µA	
VIN1 TO VIN4 (VINx) PINS					
Input Current, $I_{VINLEAK}$	−20		+20	nA	V_{VINx} = 0.7 V
Input Rising Threshold, V_{THR}	0.5952	0.6000	0.6048	V	
OUT1 TO OUT3 (OUTx), PWRGD PINS					
Output Low Voltage, V_{OUTL}			0.4	V	V_{CC} = 2.7 V, I_{SINK} = 2 mA
			0.4	V	V_{CC} = 1 V, I_{SINK} = 100 µA
Leakage Current, I_{ALERT}	−1		+1	µA	
V_{CC} that Guarantees Valid Outputs	1			V	All outputs are guaranteed to be either low or giving a valid output level from V_{CC} = 1 V
TIMING DELAYS					Delays only applicable to certain operations states; refer to state diagram (Figure 19) for more details
VIN1 to OUT1 Rising Delay	100	190	280	ms	V_{CC} = 3.3 V, see Figure 7
VIN4 to PWRGD Rising Delay	100	190	280	ms	V_{CC} = 3.3 V, see Figure 7
VIN2 to OUT2, VIN3 to OUT3					
Low-to-High Propagation Delay		30		µs	V_{CC} = 3.3 V, see Figure 9
High-to-Low Propagation Delay, All Inputs		30		µs	V_{CC} = 3.3 V, see Figure 10

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
VCC Pin	−0.3 V to +6 V
VINx Pins	−0.3 V to +6 V
OUTx, PWRGD Pins	−0.3 V to +6 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature Soldering (10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
10-Lead MSOP	137.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

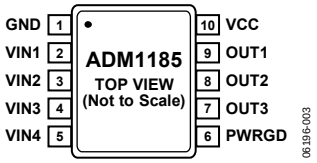

Figure 3.

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Chip Ground Pin.
2	VIN1	Noninverting Input of Comparator 1. The voltage on this pin is compared with a 0.6 V reference. Can be used to monitor a voltage rail via a resistor divider. The output of this comparator is monitored by the state machine core. This input can also be driven by a logic signal to initiate a power-up sequence.
3	VIN2	Noninverting Input of Comparator 2. The voltage on this pin is compared with a 0.6 V reference. Can be used to monitor a voltage rail via a resistor divider. The output of this comparator is monitored by the state machine core.
4	VIN3	Noninverting Input of Comparator 3. The voltage on this pin is compared with a 0.6 V reference. Can be used to monitor a voltage rail via a resistor divider. The output of this comparator is monitored by the state machine core.
5	VIN4	Noninverting Input of Comparator 4. The voltage on this pin is compared with a 0.6 V reference. Can be used to monitor a voltage rail via a resistor divider. The output of this comparator is monitored by the state machine core.
6	PWRGD	Active-High, Open-Drain Output. This output is pulled low once VCC = 1 V. When the voltage on each VINx input exceeds 0.6 V, the state machine moves from STATE4 to STATE5, and PWRGD is asserted. Once in STATE5 (the PWRGD state), this output is driven low if the voltage on VIN1, VIN2, VIN3, or VIN4 falls below 0.6 V.
7	OUT3	Active-High, Open-Drain Output. This output is pulled low once VCC = 1 V. When the voltage on VIN3 exceeds 0.6 V, the state machine moves from STATE3 to STATE4, and OUT3 is asserted. Once the power-up sequence is complete and STATE5 (the PWRGD state) is reached, this output is driven low if the voltage on VIN1 falls below 0.6 V.
8	OUT2	Active-High, Open-Drain Output. This output is pulled low once VCC = 1 V. When the voltage on VIN2 exceeds 0.6 V, the state machine moves from STATE2 to STATE3, and OUT2 is asserted. Once the power-up sequence is complete and STATE5 (the PWRGD state) is reached, this output is driven low if the voltage on VIN1 falls below 0.6 V.
9	OUT1	Active-High, Open-Drain Output. This output is pulled low once VCC = 1 V. When the voltage on VIN1 exceeds 0.6 V, the state machine moves from STATE1 to STATE2, and OUT1 is asserted. A time delay of 190 ms (typical) is included before the assertion of this pin. Once the power-up sequence is complete and STATE5 (the PWRGD state) is reached, this output is driven low if the voltage on VIN1 falls below 0.6 V.
10	VCC	Positive Supply Input Pin. The operating supply voltage range is 2.7 V to 5.5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

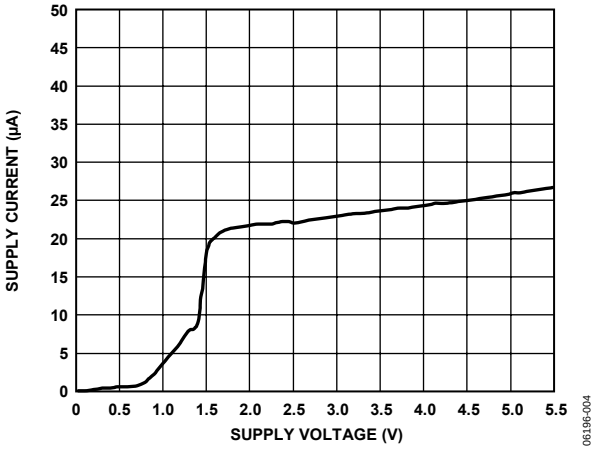

Figure 4. Supply Current vs. Supply Voltage

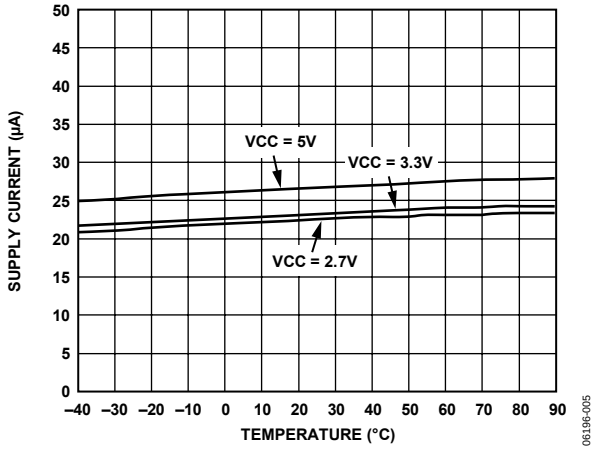

Figure 5. Supply Current vs. Temperature

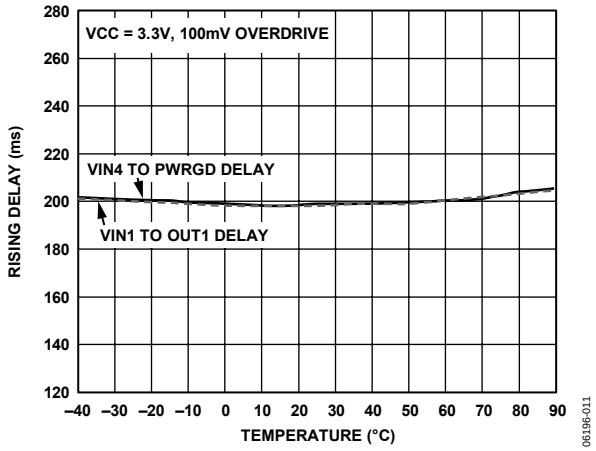

Figure 6. VIN1/VIN4 to OUT1/PWRGD Rising Delay vs. Temperature

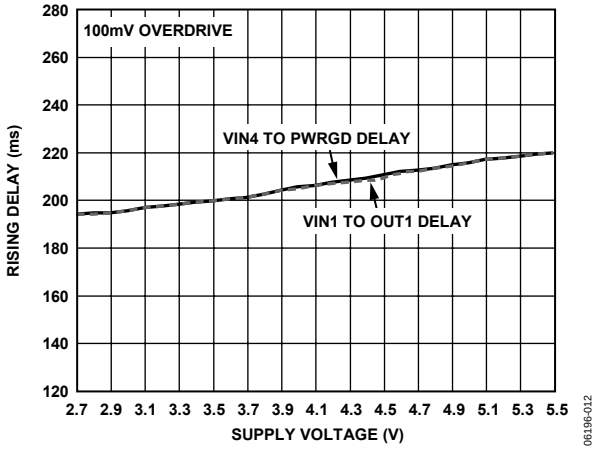

Figure 7. VIN1/VIN4 to OUT1/PWRGD Rising Delay vs. Supply Voltage

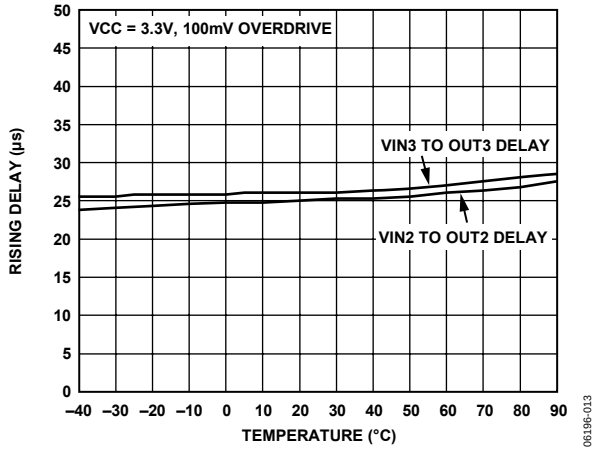

Figure 8. VIN2/VIN3 to OUT2/OUT3 Rising Delay vs. Temperature

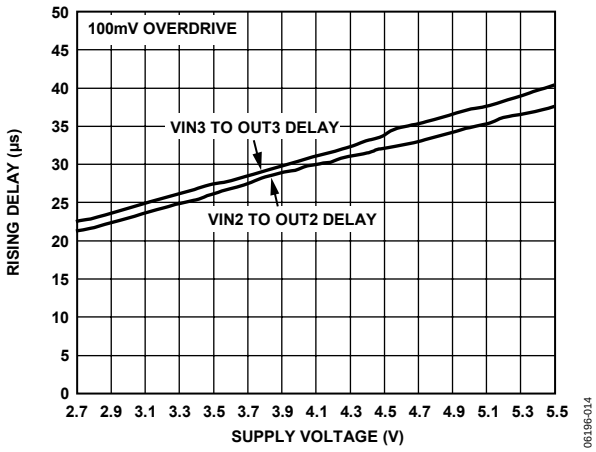

Figure 9. VIN2/VIN3 to OUT2/OUT3 Rising Delay vs. Supply Voltage

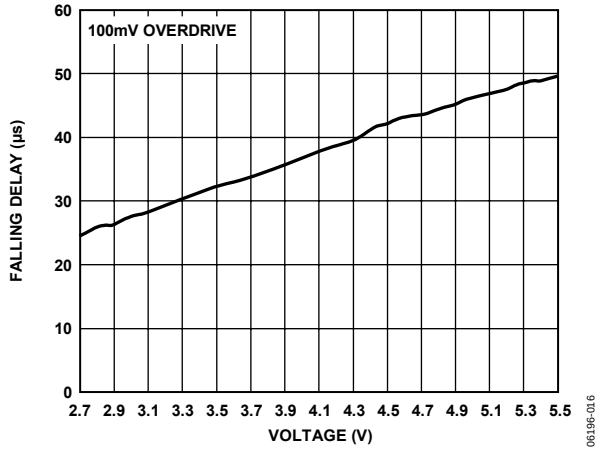

Figure 10. VIN1 to OUT1 Falling Delay vs. Supply Voltage

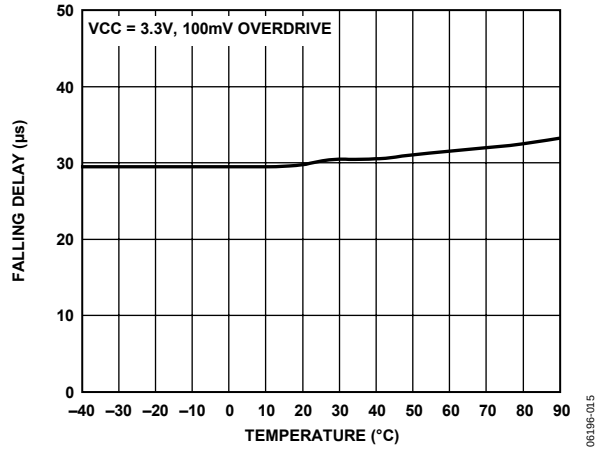

Figure 11. VINx to Output Falling Delay vs. Temperature

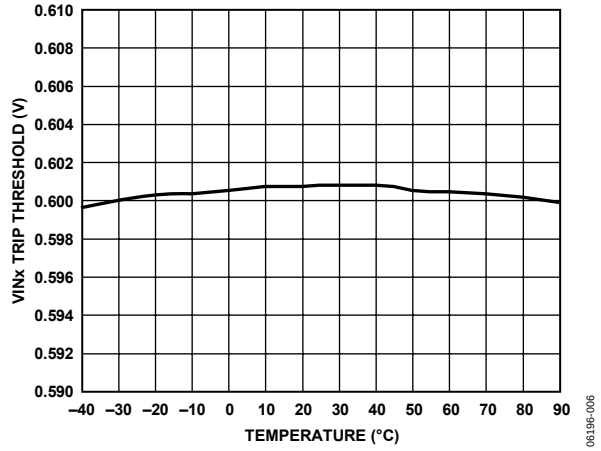

Figure 12. VINx Trip Threshold vs. Temperature

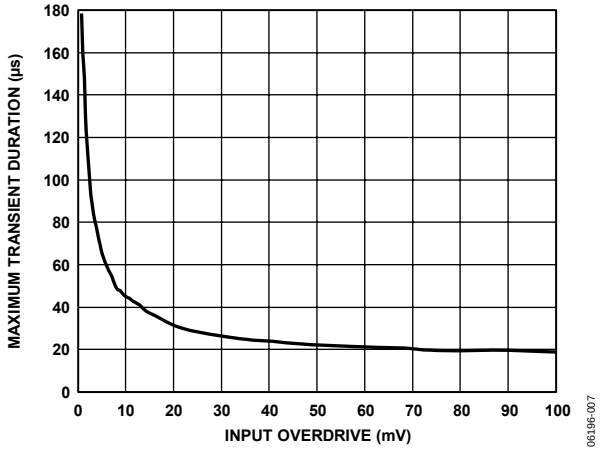

Figure 13. Trip Threshold Maximum Transient Duration vs. Input Overdrive

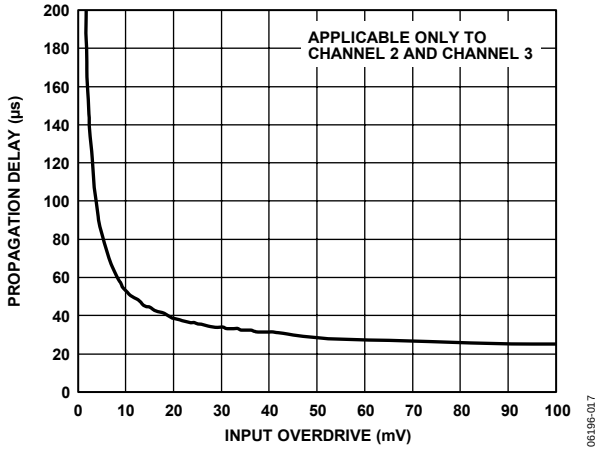

Figure 14. Propagation Delay vs. Input Overdrive

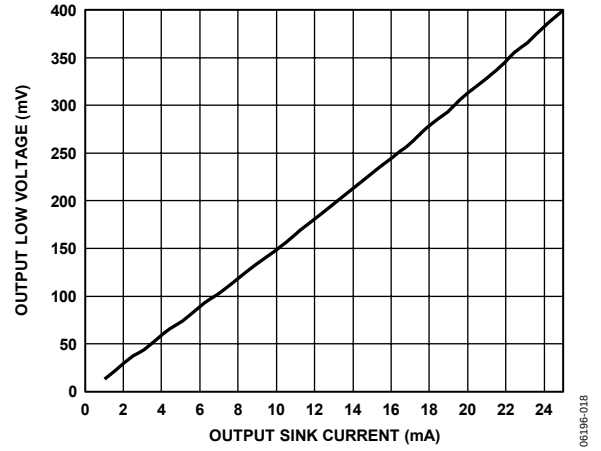

Figure 15. Output Low Voltage vs. Output Sink Current

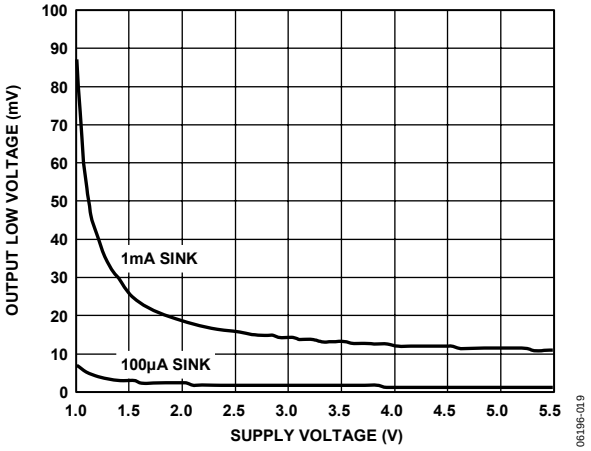

Figure 16. Output Low Voltage vs. Supply Voltage

THEORY OF OPERATION

The operation of the ADM1185 is explained in this section in the context of the device in a voltage monitoring and sequencing application (see Figure 18). In this application, the ADM1185 monitors four separate voltage rails, turns on three regulators in a predefined sequence, and generates a power-good signal to turn on a controller when all power supplies are up and stable.

POWER-ON SEQUENCING AND MONITORING

The main supply, in this case 3.3 V, powers up the device via the VCC pin as the voltage rises. A supply voltage of 2.7 V to 5.5 V is needed to power the device.

The VIN1 pin monitors the main 3.3 V supply. An external resistor divider scales this voltage down for monitoring at the VIN1 pin. The resistor ratio is chosen so that the VIN1 voltage is 0.6 V when the main voltage rises to the preferred level at start-up (a voltage below the nominal 3.3 V level). R1 is 4.6 kΩ and R2 is 1.2 kΩ, so a voltage level of 2.9 V corresponds to 0.6 V on the noninverting input of the first comparator (see Figure 17).

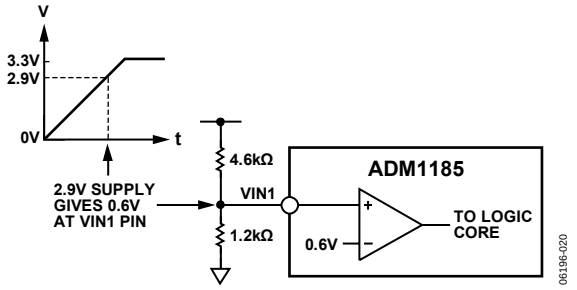

Figure 17. Setting the Undervoltage Threshold with an External Resistor Divider

OUT1 is an open-drain, active high output. In this application, OUT1 is connected to the enable pin of a regulator. Before the voltage on VIN1 reaches 0.6 V, this output is switched to ground, disabling Regulator 1. Note that all outputs are driven to ground as long as there is 1 V on the VCC pin of the ADM1185. When the main system voltage reaches 2.9 V, VIN1 detects 0.6 V. This causes OUT1 to assert after a 190 ms (typical) delay. When this occurs, the open-drain output switches high, and the external pull-up resistor pulls the voltage on the Regulator 1 enable pin above its turn-on threshold, turning on the output of Regulator 1.

The assertion of OUT1 turns on Regulator 1. The 2.5 V output of this regulator begins to rise. This is detected by Input VIN2 (with a similar resistor divider scheme, as shown in Figure 18). When VIN2 detects the 2.5 V rail rising above its UV point, it asserts Output OUT2, which turns on Regulator 2. A capacitor can be placed on the VIN2 pin to slow the rise of the voltage on this pin. This effectively sets a time delay between the 2.5 V rail powering up and the next enabled regulator.

The same scheme is implemented with the other input and output pins. Every rail that is turned on via an output pin, OUTx, is monitored via an input pin VIN(x + 1).

The final comparator inside the VIN4 pin detects the final supply turning on, which is 1.2 V in this case. The output pins, OUT1 to OUT3 are logically AND'ed together to generate a system power-good signal (PWRGD). There is an internal 190 ms delay (typical) associated with the assertion of the PWRGD output.

Table 5 is a truth table that steps through the power-on sequence of the outputs. Any associated internal time delays are also shown.

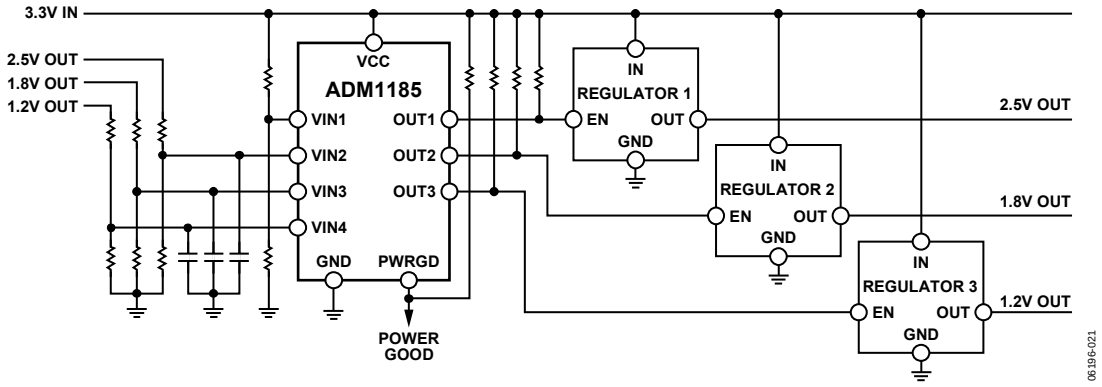

Figure 18. Voltage Monitoring and Sequencing Application Diagram

Table 5. Truth Table

State	State Name	OUT1	OUT2	OUT3	PWRGD	Next Event	Next State
1	Reset	0	0	0	0	VIN1 high for 190 ms	OUT1 On
2	OUT1 On	1	0	0	0	VIN1 and VIN2 high for 30 µs	OUT1, OUT2 On
3	OUT1, OUT2 On	1	1	0	0	VIN1, VIN2, and VIN3 high for 30 µs	OUT1, OUT2, OUT3 On
4	OUT1, OUT2, OUT3 On	1	1	1	0	All high for 190 ms	Power Good
5	Power Good	1	1	1	1	VIN2 , VIN3, or VIN4 low for 30 µs	OUT1, OUT2, OUT3 On

VOLTAGE MONITORING AFTER POWER-ON

Once PWRGD is asserted, the logical core latches into a different mode of operation. During the initial power-up phase, each output directly depends on an input (for example, VIN3 asserting causes OUT3 to assert). When power-up is complete, this function is redundant.

Once in the PWRGD state, the following behavior can be observed:

- If the main 3.3 V supply monitored via VIN1 faults in the power-good state, the PWRGD output is deasserted to warn the downstream controller. All outputs (OUT1 to OUT3) are immediately turned off, disabling all locally generated supplies.
- If a supply monitored by VIN2 to VIN4 fails, the PWRGD output is deasserted to warn the controller, but the other outputs are not deasserted.

Figure 20 and Figure 21 show waveforms that highlight the behavior of the ADM1185 under various fault situations during normal operation (that is, in the mode of operation after PWRGD is asserted).

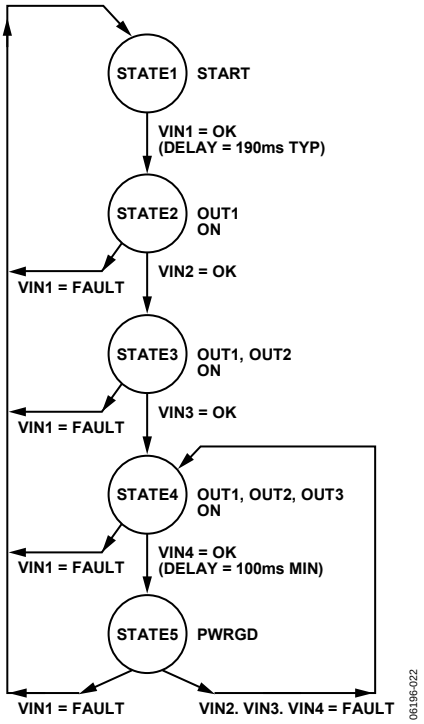

Figure 19. Flow Diagram Highlighting the Different Modes of Operation of the Logical Core

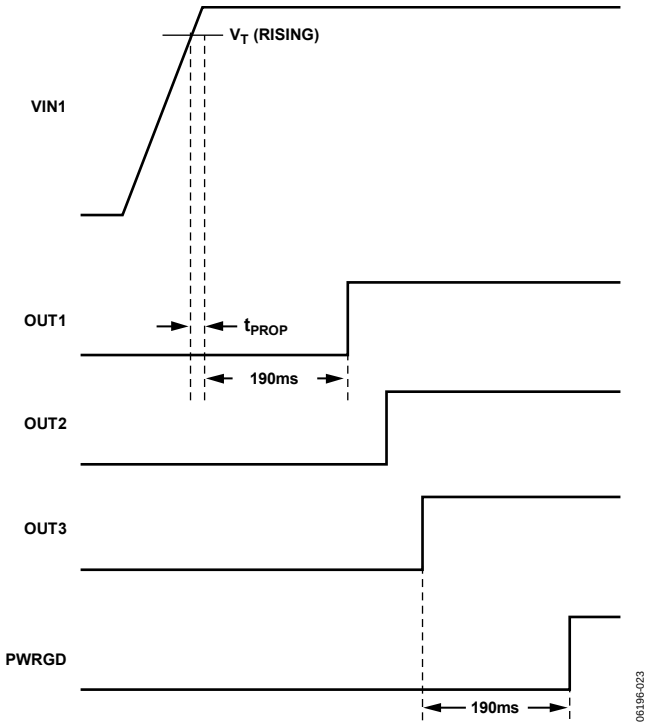

Figure 20. Power-Up Waveforms

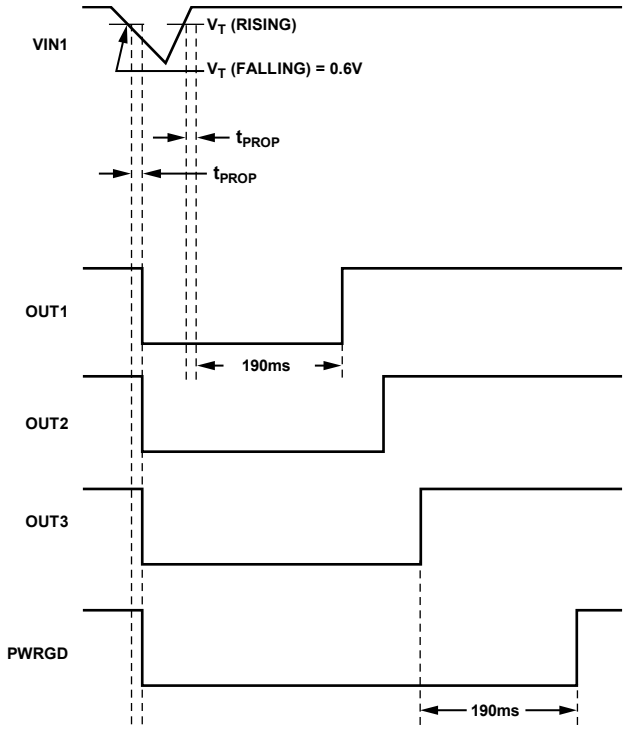

Figure 21. Waveforms Showing Reaction to a Temporary Low Glitch on the Main Supply

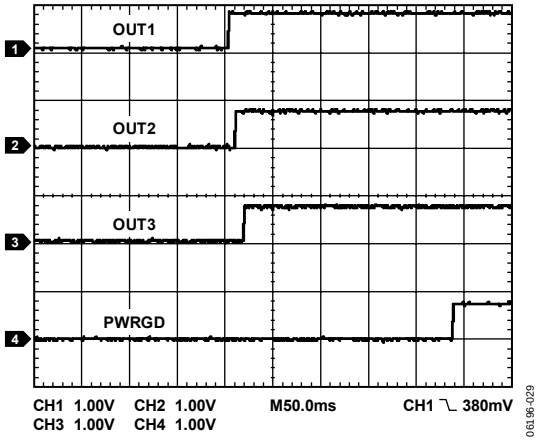

Figure 22. Plot of OUT1, OUT2, OUT3, and PWRGD Outputs at Startup in an Application Similar to that Shown in Figure 18

CASCADING MULTIPLE DEVICES

Multiple ADM1185 devices can be cascaded in situations where a large number of supplies must be monitored and/or sequenced. There are numerous configurations for interconnecting devices. The most suitable configuration depends on the application. Figure 23 and Figure 24 show two methods for cascading multiple ADM1185 devices.

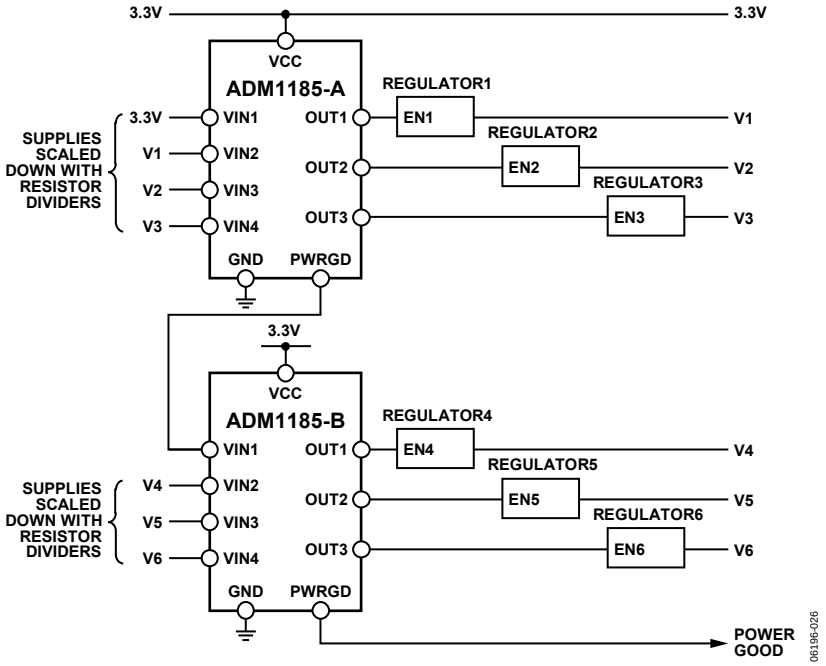

Figure 23. Cascading Multiple ADM1185 Devices, Option 1

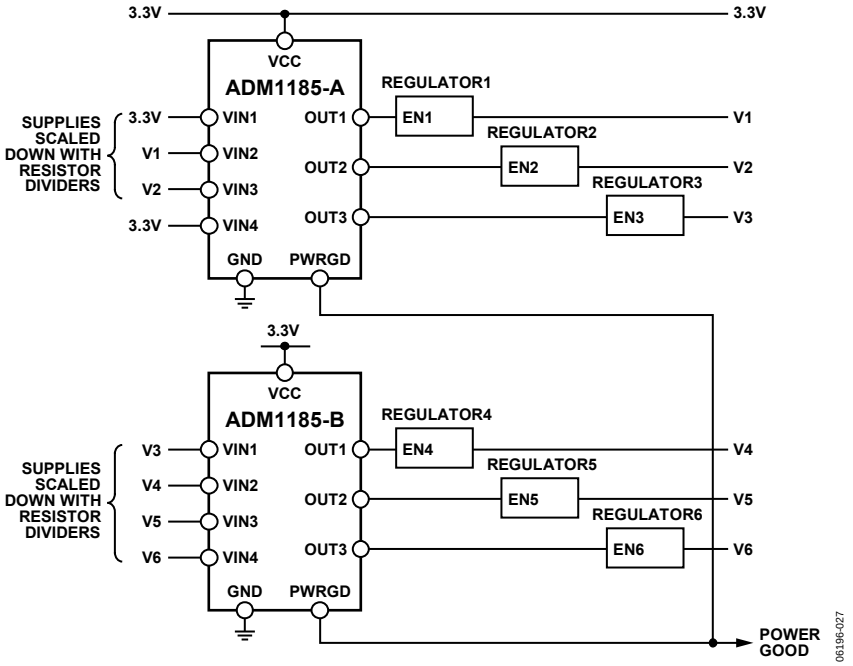

Figure 24. Cascading Multiple ADM1185 Devices, Option 2

OUTLINE DIMENSIONS

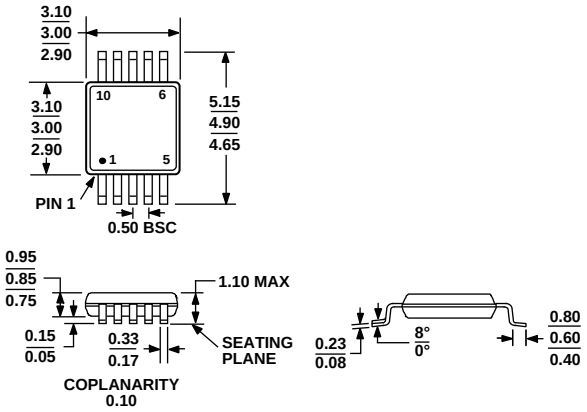

Figure 25. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADM1185ARMZ-1[1]	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	M9W
ADM1185ARMZ-1REEL7[1]	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	M9W
EVAL-ADM1185EBZ[1]		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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