intel

82750LA
Technical Specifications

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82750LA (KAGA)
Keying and Audio Gate Array

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INTRODUCTION

The Keying and Audio Gate Array (KAGA) serves three functions: (1) It is the interface between the Audio Digital Signal Processor (ADSP) and both the DVI Bus and the analog conversion components; (2) it generates keying signals to allow various video sources to be combined; (3) it contains portions of the phaselock loop which both provides video genlock capability and generates clock signals for the entire DVI System.

The following figure shows a simplified block diagram of the KAGA gate array interconnections in a typical DVI system. The ADSP outputs stereo digital audio to a dual D/A converter through a set of registers in the gate array. These analog outputs, filtered to a 17 KHz bandwidth, comprise the audio output of the DVI system. Similarly, digital stereo audio is input to the ADSP from a dual A/D converter through a set of registers in the gate array. Additional registers in KAGA provide the mechanism for the ADSP to communicate with DVI Bus components, especially the Host Processor for programming information and VRAM for audio data.

The KAGA chip provides the control signals for analog multiplexing the Intel 82750DB DVI Display Processor (DB) video with either the host's VGA video or an external source on a pixel-by-pixel basis. The actual video source selection is performed in mux chips capable of instantaneously switching inputs. The control for the keying is generated in KAGA for the VGA video by monitoring the video feature bus and in a black detect circuit for the external RGB video. The keying parameters are determined by registers in the gate array.

In order for the DB video to be combined with other video sources into a unified video stream, the sources must be synchronized or genlocked; i.e. their horizontal and vertical scanning must be carefully aligned. This is accomplished, in part, by synchronizing the DB horizontal scanning to either the VGA or external RGB horizontal sync using a phaselock loop. The loop is comprised of a phase detector and input counters in the gate array and a loop filter and VCO located off-chip. Together, these components lock the horizontal syncs and provide a pixel clock for the DB video. Alternatively, when genlocking is not required, the phaselock loop can be locked to a 10 MHz crystal to generate the timing for a wide variety of video formats, with pixel rates up to 50 MHz. The selection of clock and sync sources, as well as phaselock loop parameters are determined by registers internal to KAGA.

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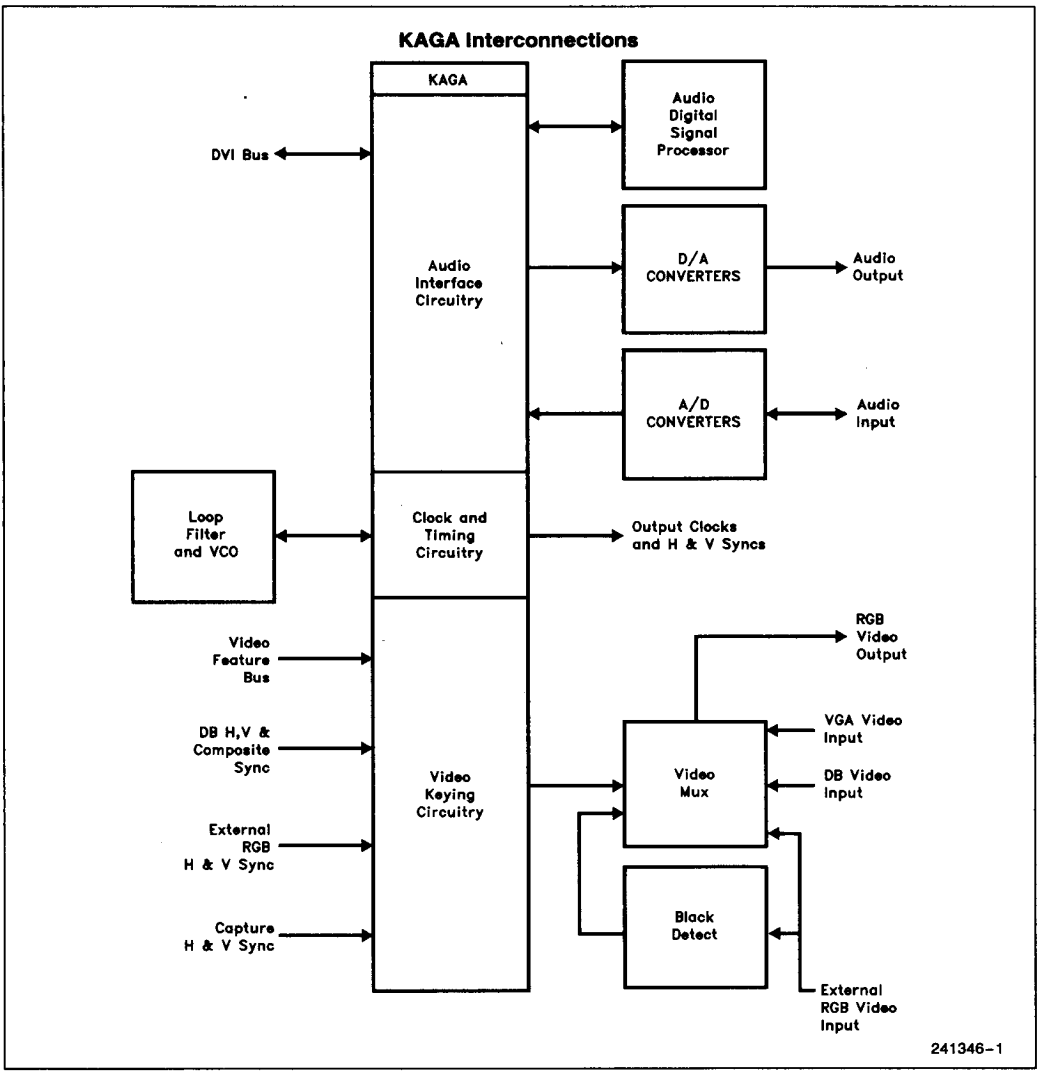
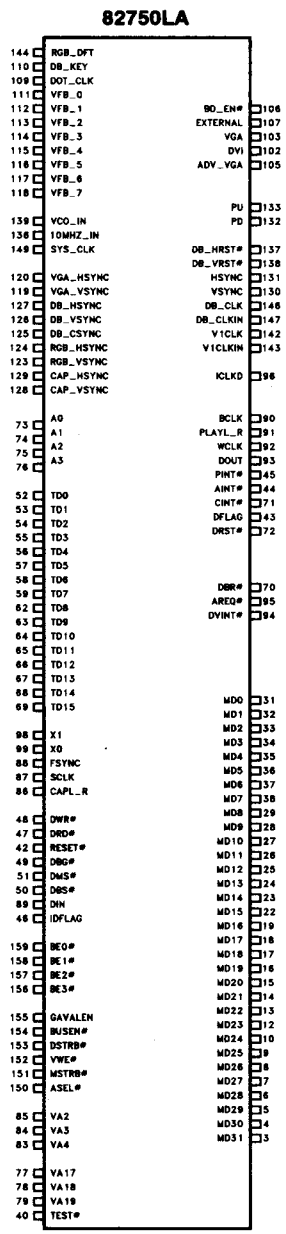


1.0 PIN DESCRIPTION

1.1 Pinout



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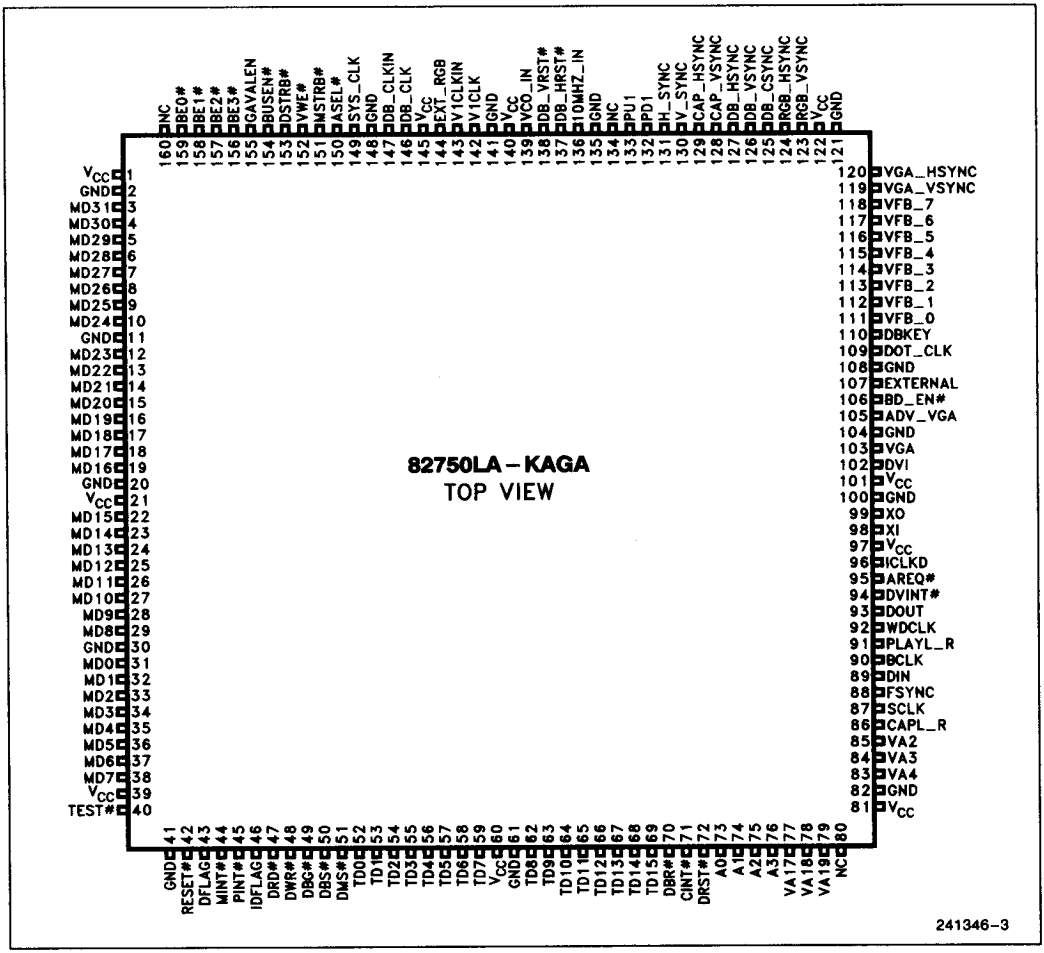


Figure 1-1. 82750LA Pinout

Table 1-1. Pin Cross Reference by Pin Name

Pin Name	Location
10MHZ__IN	136
A0	73
A1	74
A2	75
A3	76
ADV__VGA	105
AREQ#	95
ASEL#	150
BCLK	90
BD__EN#	106
BE0#	159
BE1#	158
BE2#	157
BE3#	156
BUSEN#	154
CAP HSYNC	129
CAP VSYNC	128
CAPL R	86
CINT#	71
DB CLK	146
DB CLKIN	147
DB CSYNC	125
DB HRST#	137
DB HSYNC	127
DB__VRST#	138
DB__VSYNC	126
DBG#	49
DBKEY	110
DBR#	70
DBS#	50
DFLAG	43
DIN	89
DMS#	51
DOT__CLK	109
DOUT	93
DRD#	47
DRS#	72
DSTRB#	153
DVI	102
DVINT#	94

Pin Name	Location
DWR#	48
EXT__RGB	144
EXTERNAL	107
FSYNC	88
GAVALEN	155
GND	2
GND	11
GND	20
GND	30
GND	41
GND	61
GND	82
GND	100
GND	104
GND	108
GND	121
GND	135
GND	141
GND	148
HSYNC	131
ICLKD	96
IDFLAG	46
MD0	31
MD1	32
MD2	33
MD3	34
MD4	35
MD5	36
MD6	37
MD7	38
MD8	29
MD9	28
MD10	27
MD11	26
MD12	25
MD13	24
MD14	23
MD15	22
MD16	19
MD17	18

Pin Name	Location
MD18	17
MD19	16
MD20	15
MD21	14
MD22	13
MD23	12
MD24	10
MD25	9
MD26	8
MD27	7
MD28	6
MD29	5
MD30	4
MD31	3
MINT#	44
MSTRB#	151
NC	80
NC	134
NC	160
PD1	132
PINT#	45
PLAYL__R	91
PU1	133
RESET#	42
RGB__HSYNC	124
RGB__VSYNC	123
SCLK	87
SYS__CLK	149
TD0	52
TD1	53
TD2	54
TD3	55
TD4	56
TD5	57
TD6	58
TD7	59
TD8	62
TD9	63
TD10	64
TD11	65

Pin Name	Location
TD12	66
TD13	67
TD14	68
TD15	69
TEST#	40
V1CLK	142
V1CLKIN	143
V__SYNC	130
VA2	85
VA3	84
VA4	83
VA17	77
VA18	78
VA19	79
V_{CC}	1
V_{CC}	21
V_{CC}	39
V_{CC}	60
V_{CC}	81
V_{CC}	97
V_{CC}	101
V_{CC}	122
V_{CC}	140
V_{CC}	145
VCO__IN	139
VFB__0	111
VFB__1	112
VFB__2	113
VFB__3	114
VFB__4	115
VFB__5	116
VFB__6	117
VFB__7	118
VGA	103
VGA__HSYNC	120
VGA__VSYNC	119
VWE#	152
WDCLK	92
XI	98
XO	99

Table 1-2. Pin Cross Reference by Pin Number

Pin Name	Location	Pin Name	Location	Pin Name	Location	Pin Name	Location
1	V_{CC}	41	GND	81	V_{CC}	121	GND
2	GND	42	RESET#	82	GND	122	V_{CC}
3	MD31	43	DFLAG	83	VA4	123	RGB_VSYNC
4	MD30	44	MINT#	84	VA3	124	RGB_HSYNC
5	MD29	45	PINT#	85	VA2	125	DB_CSYNC
6	MD28	46	IDFLAG	86	CAPL_R	126	DB_VSYNC
7	MD27	47	DRD#	87	SCLK	127	DB_HSYNC
8	MD26	48	DWR#	88	FSYNC	128	CAP_VSYNC
9	MD25	49	DBG#	89	DIN	129	CAP_HSYNC
10	MD24	50	DBS#	90	BCLK	130	V_SYNC
11	GND	51	DMS#	91	PLAYL_R	131	H_SYNC
12	MD23	52	TD0	92	WDCLK	132	PD1
13	MD22	53	TD1	93	DOUT	133	PU1
14	MD21	54	TD2	94	DVINT#	134	NC
15	MD20	55	TD3	95	AREQ#	135	GND
16	MD19	56	TD4	96	ICLKD	136	10MHZ_IN
17	MD18	57	TD5	97	V_{CC}	137	DB_HRST#
18	MD17	58	TD6	98	XI	138	DB_VRST#
19	MD16	59	TD7	99	XO	139	VCO_IN
20	GND	60	V_{CC}	100	GND	140	V_{CC}
21	V_{CC}	61	GND	101	V_{CC}	141	GND
22	MD15	62	TD8	102	DVI	142	V1CLK
23	MD14	63	TD9	103	VGA	143	V1CLKIN
24	MD13	64	TD10	104	GND	144	EXT_RGB
25	MD12	65	TD11	105	ADV_VGA	145	V_{CC}
26	MD11	66	TD12	106	BD_EN#	146	DB_CLK
27	MD10	67	TD13	107	EXTERNAL	147	DB_CLKIN
28	MD9	68	TD14	108	GND	148	GND
29	MD8	69	TD15	109	DOT_CLK	149	SYS_CLK
30	GND	70	DBR#	110	DBKEY	150	ASEL#
31	MD0	71	CINT#	111	VFB_0	151	MSTRB#
32	MD1	72	DRST#	112	VFB_1	152	VWE#
33	MD2	73	A0	113	VFB_2	153	DSTRB#
34	MD3	74	A1	114	VFB_3	154	BUSEN#
35	MD4	75	A2	115	VFB_4	155	GAVALEN
36	MD5	76	A3	116	VFB_5	156	BE3#
37	MD6	77	VA17	117	VFB_6	157	BE2#
38	MD7	78	VA18	118	VFB_7	158	BE1#
39	V_{CC}	79	VA19	119	VGA_VSYNC	159	BE0#
40	TEST#	80	NC	120	VGA_HSYNC	160	NC

1.2 Pin Descriptions

1.2.1 KAGA AUDIO AND DVI BUS SIGNAL DEFINITIONS

Symbol	Type	Name and Function
A3–A0	I	**A3–A0:** DSP address output used in the decode of external data memory and boot memory space.
AREQ#	O	**AUDIO REQUEST SIGNAL:** This signal is asserted indicating that the DSP is requesting control of the DMA Channel for VRAM accesses.
ASEL#	I	**AUDIO SELECT SIGNAL:** This signal indicates that the Host has acknowledged the audio request.
BCLK	O	**DAC BIT CLOCK SIGNAL:** The rising edge of this clock will shift the serial data into the internal serial shift register of the DAC.
BE#3–BE#0	BI	**BYTE ENABLES 3–0:** These signals are used by PB and DVI bus devices to indicate which bytes in the 32-bit VRAM word are being accessed. These signals should be driven by the device causing the DVI bus cycle during a VRAM access. These signals are driven by the host interface logic during a host access of registers residing in KAGA.
BUSEN#	I	**BUS ENABLE SIGNAL:** This signal is driven by PB in response to the HREQ# signal. BUSEN# indicates that the DVI bus can now be used by KAGA provided the ASEL# signal is asserted.
CAPL__R	I	**CAPTURE LEFT/RIGHT CLOCK:** This signal is generated in the ADC. KAGA receives this clock from the ADC whose output frequency is at the word rate. When this clock is high, left channel data is output. When this signal is low, right channel data is output.
CINT#	O	**CAPTURE INTERRUPT:** Generated internal to KAGA. This signal is connected to the highest priority interrupt on the DSP (IRQ2#). The signal CAPL__R initiates a CINT#. CINT# is negated when either of the audio input registers are read.
DBG#	I	**BUS GRANT INPUT:** This signal originates from the DSP (signal BG#). Control of the DSP bus is transferred to the DVI Device when the DSP asserts the BG# signal.
DBR#	O	**BUS REQUEST OUTPUT:** This signal is connected to the DSP BR# signal. When the DVI Device requires access to the DSP external bus or if the DVI Device must halt the DSP it will assert DBR#. If the DSP is not performing an external access, then it will respond to the DBR# signal in the same cycle by tri-stating the DSP data and address bus as well as DMS#, DBS#, DRD#, and DWR#.
DBS#	I	**BOOT MEMORY SELECT:** This signal is the DSP BMS# signal. The DSP signal DBS# is used to select the boot memory interface.
DFLAG	O	**DSP FLAG:** This signal is the DMARDY (DMA Ready) signal generated internal to KAGA. This signal is tied to the asynchronous input FI (Flag In) of the DSP. When DMARDY is asserted (high) the DSP is then able to read or write VRAM.
DIN	I	**SERIAL DATA INPUT:** This is the serial data received from the ADC. Audio data bits are presented MSB first, in 2's complement format.
DVINT#	O	**DVI DEVICE INTERRUPT:** Generated internal to KAGA. This signal is asserted when the DSP writes to the Message to DVI Device register (MDVI). This signal is negated when the DVI Device reads the most significant byte of the MDVI register.
DMS#	I	**DATA MEMORY SELECT:** DSP strobe signal for data memory accesses. When the DMS# signal is asserted this indicates that the address bus is being driven with a data memory address and memory can be selected.
DOUT	O	**DATA OUTPUT:** Serial data presented to the playback DAC. The DAC receives this data (with the MSB first) in Binary Two's Complement (BTC) form. The DAC takes this data as input and converts it into analog form.

1.2.1 KAGA AUDIO AND DVI BUS SIGNAL DEFINITIONS (Continued)

Symbol	Type	Name and Function
DRD#	I	**MEMORY READ ENABLE INPUT:** This signal is the DSP RD# signal. RD# is a DSP control signal, indicating the direction of the data transfer. When this signal is asserted the operation will be a DSP read of internal registers to KAGA.
DRST#	O	**DSP RESET:** DRST# halts DSP execution and returns all registers to a known state. When this bit is negated, the booting sequence takes place.
DWR#	I	**MEMORY WRITE ENABLE INPUT:** This signal is the DSP WR# signal. WR# is a DSP control signal, indicating the direction of the data transfer. When this signal is asserted the operation will be a DSP write to internal registers of KAGA.
DSTRB#	I	**DEVICE STROBE:** This signal is used to access one of the eight DVI Devices. This signal is generated whenever a VRAM access falls above the 15M byte boundary.
FSYNC	I	**FRAME SYNC SIGNAL:** This signal is generated internal to the ADC. KAGA receives this clock from the ADC. This is an output clock which goes high coincident with the start of the first data bit (MSB) and falls immediately after the last data bit (LSB).
GAVALEN	I	**GATE ARRAY VALID ADDRESS LATCH ENABLE:** This signal is used to latch the VRAM address from the MD31–MD0) lines. The MD31–MD0) bus is latched at the falling edge of GAVALEN. When GAVALEN and BUSEN# are asserted, the MD31–MD0) bus is used for VRAM address information.
ICKLD	O	**INPUT CLOCK DIGITAL:** This clock is generated in KAGA. This is the source clock for the ADC. This clock runs the digital filter internal to the ADC on the CS2 board. ICLKD must be 384 times the desired sample rate.
IDFLAG	I	**INPUT DSP FLAG:** Input signal to KAGA form the DSP. This signal may be set, toggled, or cleared in software to signal events or conditions to the DVI Device.
MD31–MD0	BI	**MEMORY DATA:** This bus is the DVI bus data path. MD(0) is the least significant bit. This bus can be used at the start of a DVI bus cycle to temporarily hold the VRAM address until latched by GAVALEN.
MINT#	O	**MESSAGE BIT:** Generated in KAGA. This signal is asserted when the DVI Device completes a write to the Message to DSP register (MDSP). This signal is negated when the DSP reads the MDSP register.
MSTRB#	I	**MEMORY STROBE:** This signal is used to latch data during a VRAM access. This signal is generated whenever a VRAM access falls below the 15M byte boundary.
PINT#	O	**PLAYBACK INTERRUPT:** Generated in KAGA. Interrupt signal to the DSP. This signal is connected to the next highest priority interrupt on the DSP (IRQ1#). The frequency of PINT# is equivalent to the audio output sample rate. This signal is negated when either of the audio playback registers are written.
PLAYL__R	O	**PLAYBACK LEFT/RIGHT CLOCK:** This signal is the playback left/right selector signal. PLAYL__R has a 50% duty cycle and is equivalent to the playback sample rate. When this signal is high the DOUT data is right channel information.
RESET#	I	**KAGA RESET INPUT:** This signal when asserted will initialize KAGA internal registers and counters. When asserted, KAGA will place the DSP in a reset state.
SCLK	I	**SERIAL DATA CLOCK:** Capture bit clock generated internal to the ADC. Data is clocked out on the rising edge of this clock. This signal is 64 times the source clock (ICLKD) of the ADC.
TD15–TD0	BI	**DSP DATA BUS:** Data communications for register transfers between KAGA and DSP.
TEST#	I	**TEST PIN:** When this signal is asserted the outputs of KAGA are tri-stated.
V1CLKIN	I	**V1 CLOCK:** This is the main synchronizing signal for the DVI bus. Although the DVI bus is asynchronous in nature and is meant to be event driven, there are some signals that must be applied to PB synchronously.

1.2.1 KAGA AUDIO AND DVI BUS SIGNAL DEFINITIONS (Continued)

Symbol	Type	Name and Function
VWE#	BI	**VRAM WRITE ENABLE:** This signal is the read/write status line that further defines the bus cycle into a read or write type of cycle. This signal is driven by KAGA when KAGA is causing a DVI bus cycle. VWE# is asserted for a write operation and negated for a read operation. When performing Device Register accesses this signal is driven by the host.
VA4–VA2	I	**VRAM ADDRESSES VA4–VA1:** These are the bits that define the offset for a DVI Device register access. The audio portion of KAGA uses only 2 locations (0000b, 0001b).
VA19–VA17	I	**VRAM ADDRESSES VA19–VA17:** These are the bits that define the DVI Device ID for a DVI Device register access. KAGA has been assigned an ID of 5 (101B).
WDCLK	O	**WORD CLOCK:** This is a playback clock. This clock is generated in KAGA. Clock frequency is 2 times the playback sample rate.
XI	I	**CRYSTAL INPUT (16.9344 MHz):** Source clock for audio capture and playback clock generation circuitry.
XO	O	**CLOCK OUTPUT (16.9344 MHz):** Oscillator output signal.

1.2.2 KAGA KEYING/GENLOCK SIGNAL DEFINITIONS

Symbol	Type	Name and Function
ADV__VGA	O	**ADVANCE VGA:** Not used in this design. This is a pre-VGA signal.
BD__EN#	O	**BLACK DETECT ENABLE:** Enable signal for the Black Detect circuitry. Black Detect examines the R G and B external video input and generates video mux control signals when black is detected.
10MHZ__IN	I	**10 MHz INPUT CLOCK:** The source of this clock is the 10 MHz oscillator output of the DSP chip. This clock can be selected as the source clock for the PB or DB.
SYS__CLK	I	**25 MHz INPUT CLOCK:** The source of this clock is a 25 MHz oscillator. This clock can be selected as the source clock for the PB or DB.
DB__CSYNC	I	**DB COMPOSITE SYNC INPUT:** The source of this signal is the Video Display Processor (DB). This signal contains the vertical serration and equalization information as well as horizontal synchronization pulses.
DOT__CLK	I	**VGA DOT CLOCK:** Dot frequency originating from the Video Graphics Adaptor (VGA) circuitry.
DVI	O	**DVI VIDEO SELECT:** Active high signal. When this signal is asserted the video mux passes the DVI video to the output video amplifiers.
EXTERNAL	O	**EXTERNAL SELECT:** Software can force this signal. If this signal is active then the external video (R,G,B) will pass through the video mux on the DS2 board to the video output.
EXT__RGB	I	**EXTERNAL RGB:** Status bit which determines the power on default state for video keying operation.
DB__HRST#	O	**HORIZONTAL RESET OUTPUT:** KAGA generates this signal. Assertion of this signal will reset all of the horizontal timing to the start of the horizontal line.
CAP__HSYNC	I	**CAPTURE HORIZONTAL SYNC:** Horizontal video synchronization signal. The source of this signal is the Video Capture circuitry.
VGA__HSYNC	I	**VGA BUS HORIZONTAL SYNC:** Horizontal video synchronization signal. The source of this signal is the VGA circuitry.
DB__HSYNC	I	**DB HORIZONTAL SYNC:** The source of this signal is the Video Display Processor (DB). This is a video synchronization signal which is asserted at the beginning of every line and ends a programmed time later.
RGB__HSYNC	I	**EXTERNAL HORIZONTAL SYNC:** Horizontal video synchronization signal. The source of this signal is the External RGB circuitry.
PD1	O	**PUMP DOWN OUTPUT:** Phase Detector output. This signal together with the PU1 signal are inputs to the charge pump to the PLL circuit.
PU1	O	**PUMP UP OUTPUT:** Phase Detector output. This signal together with the PD1 signal are inputs to the charge pump to the PLL circuit.
V1CLK	O	**PB CLOCK SOURCE:** This signal provides the fundamental timing for the 82750PB.
V1CLKIN	I	**PB CLOCK INPUT TO KAGA:** This is the PB clock input signal. The V1 CLK signal is fed back into KAGA so that timing referenced to V1 CLK internal to KAGA is identical to timing referenced to all other devices.
DB__CLK	O	**DB CLOCK SOURCE:** This signal provides the fundamental timing for the 82750DB.
DB__CLKIN	I	**DB CLOCK INPUT TO KAGA:** The DB__CLK signal is fed back into KAGA so that timing referenced to DB__CLK internal to KAGA is identical to timing referenced to all other devices.

1.2.2 KAGA KEYING/GENLOCK SIGNAL DEFINITIONS (Continued)

Symbol	Type	Name and Function
DB__KEY	I	**DB KEY:** The 82750DB Alpha Bit-7. This signal is used with the VGA signal in order to define a valid area on the active display for VGA Keying.
VGA	O	**VGA VIDEO SELECT:** Active high signal. When this signal is asserted the video mux passes the VGA video to the output video amplifiers.
VFB7-VFB0	I	**VIDEO FEATURE BUS:** Pixel Select Inputs originating from the Video Feature Connector. These signals are compared to the Chroma Register value to generate the DVI/VGA keying signals.
DB__VRST#	O	**VERTICAL RESET OUTPUT:** Assertion of this signal by KAGA will reset all vertical timing in the DB.
CAP__VSYNC	I	**CAPTURE VERTICAL SYNC:** Vertical Video Sync signal originating from the capture circuitry.
DB__VSYNC	I	**DB VERTICAL SYNC:** Video Sync signal which can be programmed to start and end in each field. DB is the source of this signal.
VGA__VSYNC	I	**VGA VERTICAL SYNC:** Vertical Video Sync signal generated by the VGA circuitry.
HSYNC	O	**HORIZONTAL SYNC:** System Output Horizontal Sync to monitors etc.
VSYNC	O	**VERTICAL SYNC:** System Output Vertical Sync to monitors etc.
VCO__IN	I	**VCO INPUT:** The source of this clock is the VCO. This clock can be selected as the source for the PB or DB.
RGB__VSYNC	I	**EXTERNAL VERTICAL SYNC:** Vertical Video Sync signal generated by the External RGB circuitry.

2.0 INTERNAL ARCHITECTURE

2.1 Audio

2.1.1 OVERVIEW

The audio portion of KAGA consists of 18 memory-mapped registers addressable from the DVI Bus, the ADSP Bus or both, plus logic to support their functions. The ADSP typically accesses these registers to communicate with the Host, to input data from the A/D Converters, to output data to the D/A Converters, and to exchange audio and program data with VRAM. Similarly, the Host (or other DVI device) will access these registers to load audio software or to check the status of the audio subsystem. A detailed block diagram of the audio portion of KAGA and its interconnections to the ADSP, the DVI Bus and the A/D and D/A Converters is shown in Figure 2-1. Each of the audio gate array functional components is described in greater detail in the following sections of this chapter.

2.1.2 REGISTER CONFIGURATION

The ADSP registers are implemented in low external data memory space (0000–000BH). Table 2-1 shows a listing of their names, addresses and accessibility from each bus. All are 16 bits except for the BOOT Register, which is determined by the ADSP to be 8 bits. Each 16-bit register can be accessed with either byte or word operations. Some pairs of registers share the same address, with one read-only and the other write-only with respect to the ADSP Bus.

The DVI registers are located in the range of FA0000H to FA0007H on the DVI Bus, which conforms to the Audio subsystem having a DVI Device ID of 5. Each register can be accessed with either byte, word or long word operations.

Table 2-1. Audio Registers

Register	DVI Address	DVI R/W	ADSP Address	ADSP R/W	Register Description
ACS			0000H	R/W	Audio Command and Status
MDVI	FA0002H	R	0001H	R/W	Message to DVI Device
MDSP	FA0004H	R/W	0002H	R	Message to DSP Device
SRCS			0003H	R/W	Sample Rate Command and Status
RVR0/WVR0			0004H	R/W	Least Significant VRAM Read/Write Data*
RVR1/WVR1			0005H	R/W	Most Significant VRAM Read/Write Data*
CPAR			0006H	R/W	Capture/Playback Audio Right*
CPAL			0007H	R/W	Capture/Playback Audio Left*
WVRADD0			0008H	R/W	Least Significant VRAM Write Address
WVRADD1			0009H	R/W	Most Significant VRAM Write Address
RVRADD0			000AH	R/W	Least Significant VRAM Read Address
RVRADD1			000BH	R/W	Most Significant VRAM Read Address
DCS	FA0006H	R/W			DVI Device Command and Status
BOOT	FA0000H	R/W			BOOT

NOTE:
*Two registers sharing one address.

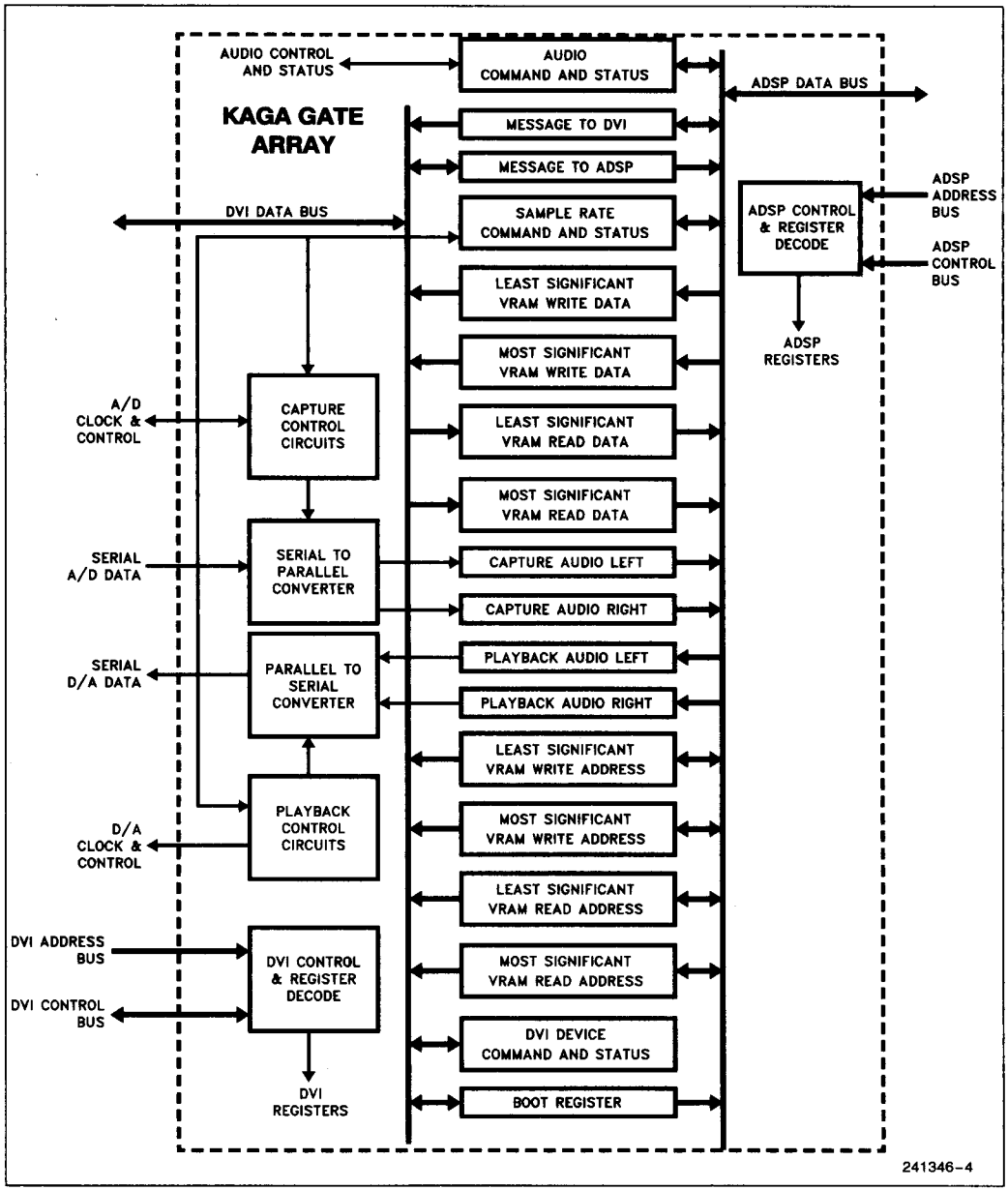


Figure 2-1. Audio Gate Array Architecture

2.1.3 DMA REGISTERS

The audio subsystem's interface to the DVI Bus consists of four 16-bit DMA Data Registers (RVR0, RVR1, WVR0, WVR1) which are used to hold VRAM data, two 16-bit DMA Write Address Registers (WVRADDO, WVRADD1) and two 16-bit Read Address Registers (RVRADD0, RVRADD1).

The ADSP writes data to VRAM by first loading the VRAM destination into the Write Address Registers and then loading the data into the WVR Data Registers, least significant word first. The VRAM write operation begins when the most significant Data Register is loaded.

The ADSP reads data from VRAM by loading the VRAM access location into the Read Address Registers, least significant word first. The data can then be read from the RVR Data Registers. The VRAM read operation begins when the most significant Read Address Register is loaded.

After a DMA read or write operation is initiated, the hardware requests control of the DVI Bus for one transfer. Once handshaking signals are exchanged, the data is transferred and another DMA operation may then be requested.

If blocks of contiguous VRAM data are to be transferred, the autoincrement mode should be used. When this mode is selected for writing VRAM data, the Write Address Register is post-incremented by a long or double word after the completion of each audio DMA cycle. Additionally, a new cycle is initiated each time the most significant word of data is written. When this mode is selected for reading VRAM data, the read address register is post-incremented by a double word after the completion of each audio DMA cycle. Additionally, a new cycle is initiated each time the most significant word of data is read.

2.1.4 BOOT REGISTER

The Boot Register is an 8-bit register that is used to initially load the ADSP internal program RAM. The gate array allows a DVI device to emulate a Boot ROM, which is typically used for this purpose. Handshaking signals are used with the ADSP to operate it in single-step mode to allow for the long access time required to obtain boot data from the DVI Bus.

2.1.5 MESSAGE REGISTERS

The KAGA gate array has two 16-bit registers that are used to exchange data between the ADSP and DVI Buses. The first is the Message to DVI Register (MDVI). This is a read/write register on the ADSP Bus which can be read by DVI Devices. The DVI Command and Status Register (DCS) indicates when there are unread messages in this register and an output pin on the array can be used as a message interrupt. The second is the Message to DSP Register (MDSP). Similarly, this is a read/write register on the DVI Bus which can be read by the ADSP. The Audio Command and Status Register (ACS) indicates when there are unread messages in this register and an output pin on the array can be used as a message interrupt. The MDSP Register is typically used to load program data to the ADSP once the boot loading process is complete.

2.1.6 PLAYBACK AND CAPTURE REGISTERS

Two write-only 16-bit Playback Audio Registers (PAL, PAR) are available to the ADSP to output stereo audio data to the dual D/A Converter. These contain the left and right channels of audio, respectively. Data placed in these registers is combined to form a 32-bit serial data word which is then shifted out to the D/A Converter.

Two read-only 16-bit Capture Audio Registers (CAL, CAR) are available to the ADSP to acquire stereo audio data from the dual A/D Converter. These contain the left and right channels of audio, respectively. Data contained in these registers has been converted from a 32-bit serial data word which was previously shifted in from the A/D Converter.

The rate at which data is played back and captured is determined by two independent six-bit numbers stored in the Sample Rate Command and Status Register (SRCS).

2.1.7 COMMAND AND STATUS REGISTERS

There are two 16-bit read-write KAGA registers, ACS and DCS, which are accessible to the ADSP and DVI Buses respectively. They are used to control configurations and modes of operation of the audio subsystem and to monitor the status of various operations taking place within the system.

2.2 Keying and Genlock

2.2.1 OVERVIEW

The keying and genlocking portion of the KAGA gate array performs several functions: It provides the timing and control signals to allow DVI-generated video to be synchronized and mixed with either digital VGA or analog RGB sources. It also permits the DVI video to be locked to an external synchronization source, such as a video capture board or studio sync. Additionally, it contains components for a crys-

tal-based frequency synthesizer which can produce pixel clocks up to 50 MHz to satisfy a wide range of video format options. Finally, it allows an independent selection of external clock frequencies up to 50 MHz to drive both the DVI Display Processor (DB) and the DVI Pixel Processor (PB).

The gate array contains several subsystems to perform the above tasks: (1) four multiplexers to select horizontal and vertical sync signals for the system's video output and DB; (2) two multiplexers to select the clocks used for DB and PB; (3) two 12-bit counters and a phase detector for use in the phaselock loop generating and synchronizing clock frequencies; (4) keying logic to select the mode of the video keying and to control the keying of the DVI video with the VGA video; and (5) seven memory-mapped registers addressable from the DVI Bus to control and monitor the operation of the other subsystems in this portion of the gate array. A detailed block diagram of the keying and genlock portion of KAGA and its interconnections to the DVI Bus, PB, DB, various video and clock sources, the phaselock loop and the keying circuit is shown in Figure 2-2. Each of the keying and genlock functional components is described in greater detail in the following sections of this chapter.

2.2.2 VIDEO SYNC MUXES

The Video Sync Muxes select the horizontal and vertical sync pulses which accompany the output video of the DVI system. The Horizontal Sync Mux can select from DB, VGA and RGB Horizontal Syncs and DB Composite Sync. The Vertical Sync Mux can select from DB, VGA, RGB and Capture Vertical Syncs. If VGA or RGB video is the only output of the system, choosing the respective syncs is in order. If the Display Processor is to be genlocked to those or other video sources, the appropriate combination of DB syncs should be chosen. Although the Capture Vertical Sync can be selected for Video Sync Output, it is advisable to synchronize the DB to it by selecting it for the DB Vertical Reset and then choosing the DB Vertical Sync in the Video Sync Mux.

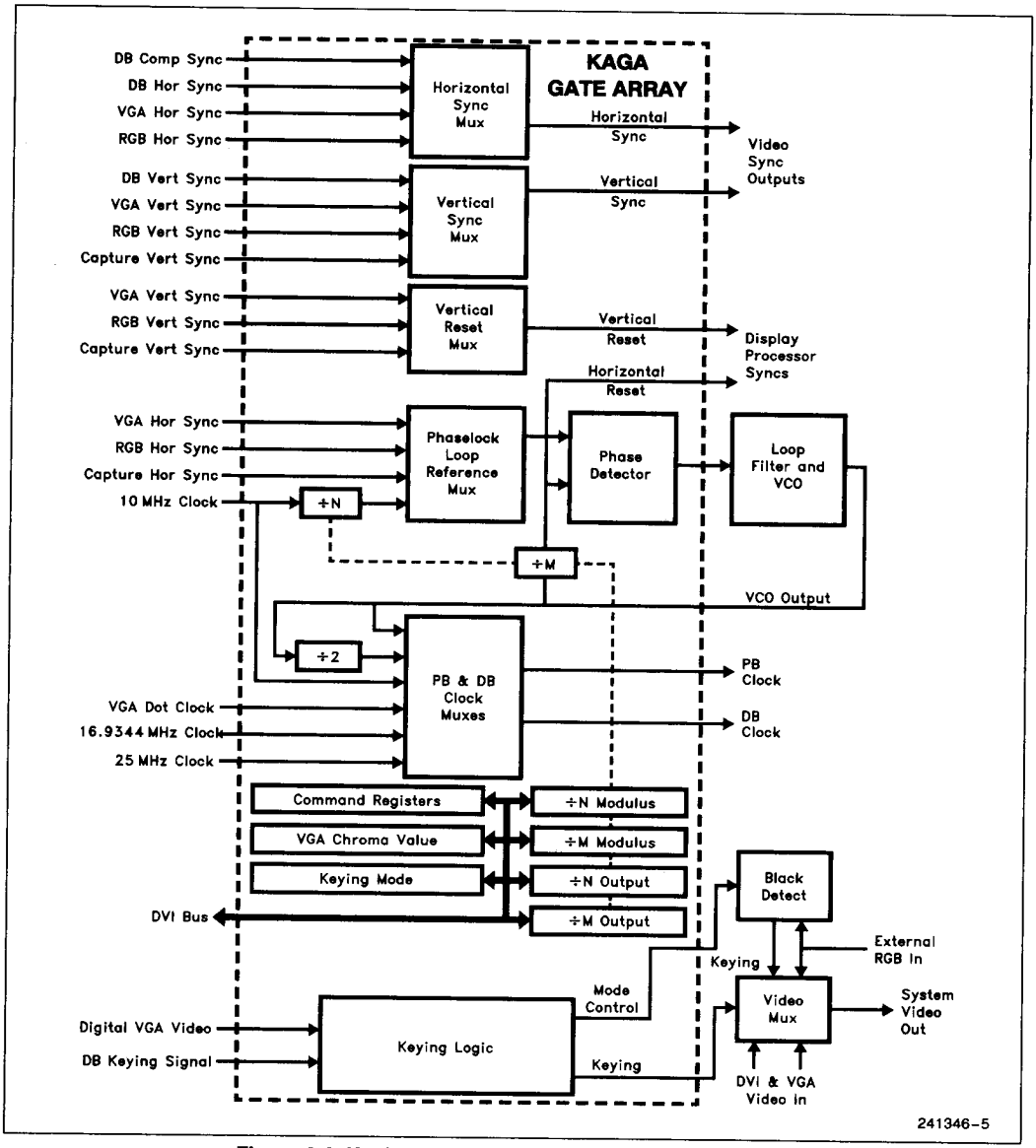


Figure 2-2. Keying and Genlock Gate Array Architecture

2.2.3 DISPLAY PROCESSOR VERTICAL RESET MUX

The Display Processor Vertical Reset Mux selects the sync pulse which is used to reset the vertical display counter in the DB. The Vertical Reset Mux can select from VGA, RGB and Capture Vertical Syncs and is used for genlocking purposes.

2.2.4 PHASELOCK LOOP COMPONENTS

The block diagram of a frequency synthesizer phaselock loop is shown in Figure 2-3. A stable input frequency (F_{REF}) is used as a reference to generate the desired output frequency. Its frequency is first divided in a ÷N Counter after which it is used as one input to a Phase Detector. The other input comes from a Voltage Controlled Oscillator (VCO) whose output frequency (F_{OSC}) is divided in a ÷M Counter. The Phase Detector output represents the difference in phase between these two divided down frequencies. This output goes to an external loop filter which controls many of the performance parameters of the loop. The filtered control voltage then goes to an external VCO whose output is driven toward a frequency and phase that minimizes the phase error out of the detector. When this error approaches zero, the loop will achieve lock (i.e., the two phase detector inputs will be the same). In order for this to occur, the frequency $F_{REF} \div N$ must be equal $F_{OSC} \div M$. Rearranging terms:

$$F_{OSC} = F_{REF} \times \left(\frac{M}{N}\right)$$

By using a crystal source for F_{REF} and appropriately choosing N and M, a wide range of stable frequencies can be achieved at the output.

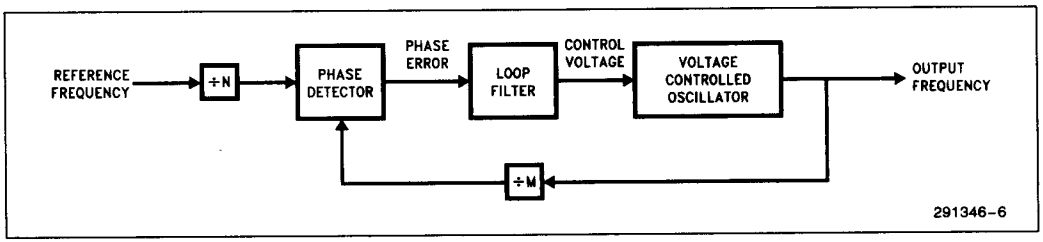


Figure 2-3. Frequency Synthesizer Phaselock Loop Block Diagram

The main use for this synthesized frequency is as a programmable pixel clock for the DVI Display Processor. Accurate clock rates up to 50 MHz can be achieved using a reference frequency of 10 MHz. Alternatively, the phaselock loop can be used to genlock the DVI video to an external video source. In this mode the reference input to the Phase Detector is the external input video horizontal sync selected by the Phaselock Loop Reference Mux. The ÷N Counter is not used (see Figure 2-2). The modulus of the ÷M Counter is set equal to the desired number of pixels per line. When the loop locks, the DVI Display Processor will then be producing pixels in synchronism with the external source video.

Within the KAGA gate array, the ÷M and ÷N Counters are implemented as 12-bit counters and each can be set for any even modulus between 10 and 4096. Each can also be selected to change state on the positive or negative transition of its input. The Phase Detector is also located in the gate array. It compares the negative-going edges of the ÷M and ÷N waveforms and produces timing pulses proportional to the phase error between the two. (The ÷M output can optionally be inverted before being applied to the Phase Detector.) This operation can be seen more clearly by referring to the Phase Detector logic diagram in Figure 2-4 and the timing diagram of Figure 2-5.

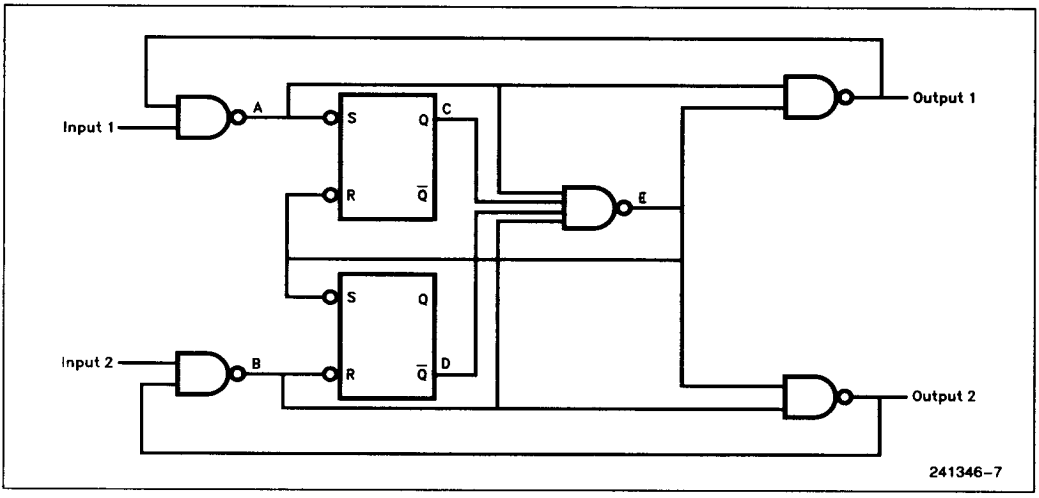


Figure 2-4. Phase Detector Diagram

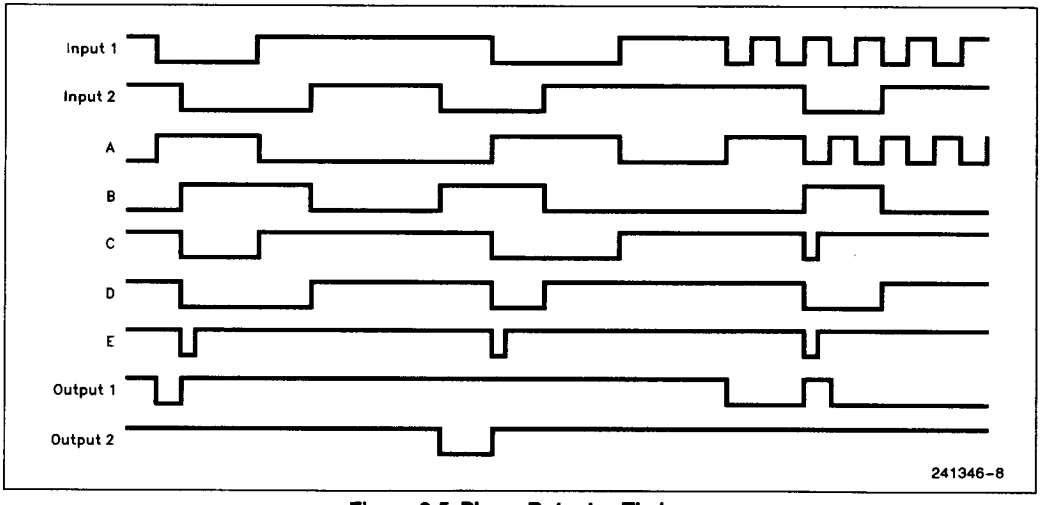


Figure 2-5. Phase Detector Timing

In Figure 2-4 Inputs 1 and 2 are the outputs of the ÷M and ÷N Counters. Assume that initially all inputs and outputs are high. This determines the state of all the internal locations (A through E) in the diagram. If Input 1 goes low first, this causes Output 1 to go low and stay low until Input 2 goes low, at which time signal E goes low briefly resetting both outputs to their high state. When Inputs 1 and 2 go high, the circuit returns to its initial state. Similarly, in the timing diagram, when Input 2 goes low first, Output 2 goes low and stays low until Input 1 goes low. In summary, the appropriate output will be asserted (low) depending on which input goes low first and the pulse width will be proportional to the time difference in the input negative-going edges. In the last section of the timing diagram, Input 1 is at a higher frequency than Input 2. In this case Output 1 stays asserted most of the time, showing that this Phase Detector has a high sensitivity for input frequency offsets (in contrast with an exclusive-or type phase detector).

In order to provide some flexibility in the use of the Phase Detector, the output configuration can be selected under software control. One option is the one shown in Figure 2-4. Another provides positive-going output pulses (non-inverted). A third uses each asserted output as the enable for a tri-stated gate whose output is driven to a high level. In the final configuration the two Phase Detector inputs appear at the output, permitting the use of an external Phase Detector.

The remaining loop components, consisting of a loop filter and a VCO, are located external to the chip.

2.2.5 PB AND DB CLOCK MUXES

The clocks used to operate the PB and DB Processors are individually selectable from the choice shown in Figure 2-2. The 25 MHz system clock is a typical choice for PB while the VCO output is usually used for DB. The VCO÷2 output allows the use of a lower clock frequency than the VCO can provide.

2.2.6 KEYING LOGIC

KAGA determines the source of the system output video using connections to the Video Feature Bus, DB, the Black Detect Circuit and the Video Mux. There are several ways in which this choice can be made. The gate array can externally select DVI, VGA or External RGB as the sole output video. A second option is to make VGA video the default selection, replacing it with DVI Video only when a digital VGA pixel value equal to a previously stored value is detected. A third option is the same as the second but additionally requires a DB Keying Signal to be asserted for DVI to be selected. The final option is to make External RGB Video the default selection, replacing it with DVI Video only when the Black Detect Circuit determines that the RGB value is near black. In this last case the gate array controls the mode of operation and the keying signal is provided externally.

2.2.7 REGISTER CONFIGURATION

The Keying and Genlock Registers are located in the range from FA0008H to FA0015H on the DVI Bus which conforms to the subsystem having a DVI Device ID of 5. Each register can be addressed with either byte, word or long word operations.

Table 2-2. Keying and Genlock Registers

Register	DVI Address	DVI R/W	Register Length	Register Description
NMOD	FA0008H	R/W	16 Bits	N Modulus
MMOD	FA000AH	R/W	16 Bits	M Modulus
NCTR	FA000CH	R	16 Bits	N Counter
MCTR	FA000EH	R	16 Bits	M Counter
GCSR	FA0010H	R/W	32 Bits	Genlock Command and Status
CKVAL	FA0014H	R/W	8 Bits	Chroma Keying Value
KMSEL	FA0015H	R/W	8 Bits	Keying Mode Select

2.2.8 MODULUS AND COUNTER REGISTERS

The 16-bit read-write N Modulus (NMOD) and M Modulus (MMOD) Registers are used to determine the values to which the 12-bit ÷N and ÷M Counters respectively divide their input clock frequency. The Counters will count to a number two greater than the values in NMOD and MMOD. When the chip is reset, these registers are each loaded with the value 200H.

The 16-bit read-only N Counter (NCTR) and M Counter (MCTR) Registers permit a DVI Device to instantaneously read the respective Counter values. This feature is primarily used for diagnostic purposes.

2.2.9 GENLOCK COMMAND AND STATUS REGISTER

This 32-bit read-write register, GCSR is used to control and monitor the following parameters involved in genlocking the DVI Video to external video sources: (1) The selection of the PB and DB clocks; (2) the mode of the phase detector; and (3) the choice of horizontal and vertical syncs for the various muxes.

2.2.10 CHROMA KEYING VALUE REGISTER

This 8-bit read-write register, CKVAL, is used select and monitor the stored digital VGA pixel value which causes VGA keying to occur when that mode is selected.

2.2.11 KEYING MODE SELECT REGISTER

This 8-bit read-write register, KMSEL, is used to select and monitor the choice of keying mode as described in Section 2.2.6.

3.0 HARDWARE INTERFACE

3.1 DVI Bus Register Access

The KAGA gate array recognizes a DVI Bus access to one of its registers whenever the upper VRAM Address bits match the KAGA DVI Device ID (VA19–VA17) = 5 and the Device Strobe line (DSTRB#) is asserted indicating that (VA23–VA20) = F Hex. Therefore, combining the two conditions, an access is made whenever the address lies anywhere in the FA0000H to FBFFFFH range. Within this range only the four locations shown in Table 2-1 are used for audio. This selection is made using (VA4–VA2) and the Byte Enables (BE#3–BE#0). Read and write cycles are differentiated by the state of the VRAM Write Enable signal (VWE#). This is demonstrated in Figure 3-1.

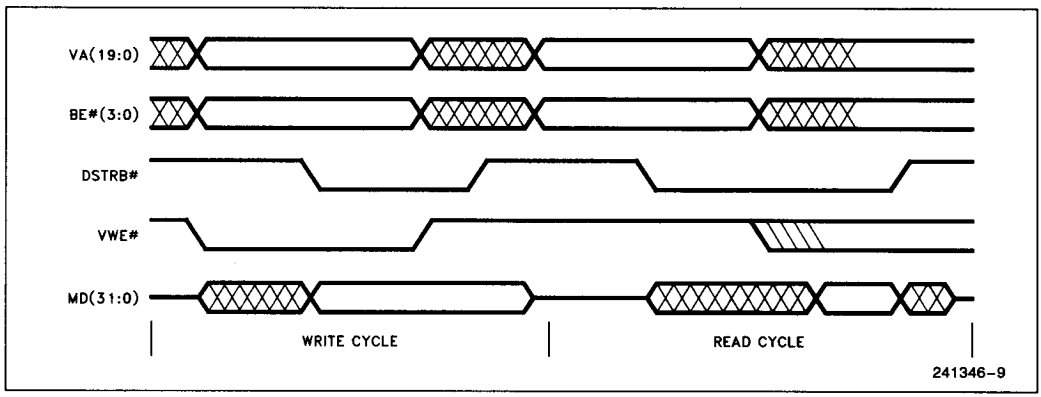


Figure 3-1. DVI Bus Register Access

3.2 Audio

A diagram of the KAGA gate array interconnections relating to the audio subsystem is shown in Figure 3-2. These signals will be described in conjunction with various operations performed by the audio subsystem. In order to fully appreciate the operation of the audio system hardware, refer to the Analog Devices ADSP-2105 data sheet and ADSP-2101 User's Manual.

3.2.1 ADSP BUS REGISTER ACCESS

The KAGA gate array recognizes an ADSP Bus Access to any one of its registers whenever the Data Memory Strobe (DMS#) and either the Data Read (DRD#) or the Data Write (DWR#) signals are asserted. The ADSP Address Bus (A3–A0) is decoded to determine which register is being addressed. As shown in Table 2-1 byte addresses from 0H to BH correspond to the audio registers. Read and Write Cycles are differentiated by whether the DWR# or the DRD# signal is asserted as shown in Figure 3-3.

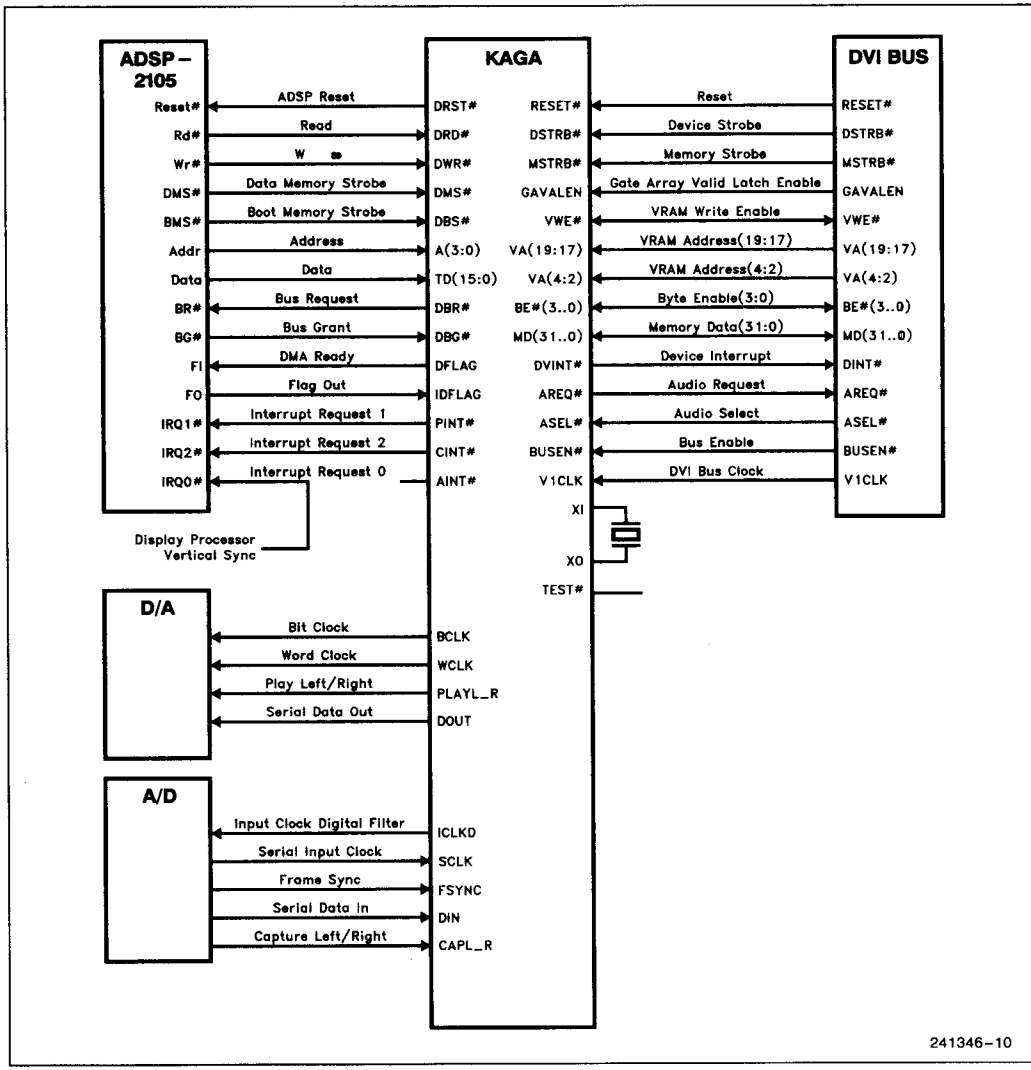


Figure 3-2. KAGA Audio Interconnections

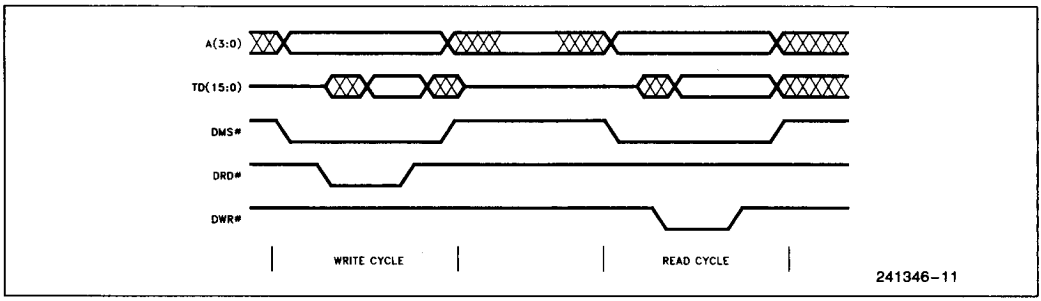


Figure 3-3. ADSP Bus Register Access

3.2.2 RESET AND BOOT LOAD

Upon power-up the audio digital signal processor has random data in its program memory and is held in a reset state. The reset is caused by the DVI Bus RESET# input pin on KAGA being asserted, in turn asserting the DRST# output to the ADSP, halting that processor. The output remains asserted until the DRST bit in the DCS register is set to a 0 by a DVI Device. Since this action will immediately initiate a boot load of program memory in the ADSP, this should not be done before some preparation is made.

During the booting process the DVI Bus acts as a Boot ROM for the ADSP. Since the interaction with the DVI BUS is slow due to the low priority of the audio system, it is not possible to allow the ADSP to run at its normal speed. KAGA contains circuitry which allows the DVI Device to provide one byte of data at a time to the ADSP program boot by interrupting the processor after each data transfer until the next byte can be supplied. The procedure, described in Figure 3-4, is as follows:

While the ADSP is still reset, the 8-bit BOOT Register is loaded from the DVI Bus. Writing of this register sets the Bus Ready (BRDY) status bit in the DCS Register to a 0. The hardware reset is then removed by setting the DRST# bit in the DCS register to a 0. The ADSP then reads the BOOT Register and after the leading edge of the DRD# signal, the gate array automatically asserts the Bus Request signal (DBR#) to the ADSP, halting the processor after the completion of the read cycle. At the trailing edge of the Boot Memory Strobe (DBS#) the gate array reasserts BRDY, at which time the DVI Device can load the succeeding byte. The trailing edge of the DSTRB# signal from that load qualified with (DVI Device = 5) indicates that new data is in the Boot Register and automatically releases the DBR# line to the ADSP, allowing that processor access to this data. This process continues one byte at a time, until the entire boot program is loaded. After the last byte is loaded, the DVI device must set the DBR# bit to 0 to allow the ADSP to begin executing the boot software. Note that the ADSP Address lines, (A3–A0), are not used since the BOOT Register responds to all DBS# cycles and the Host "knows" the order in which to supply the boot program. Refer to the ADSP User's Manual for a description of the sequence of bytes which must be loaded in the boot process.

In practice, the boot program contains only the software to allow the loading of the remaining program code using the MDSP Register. This second loading mechanism permits transfers of 16 bits and is therefore more efficient.

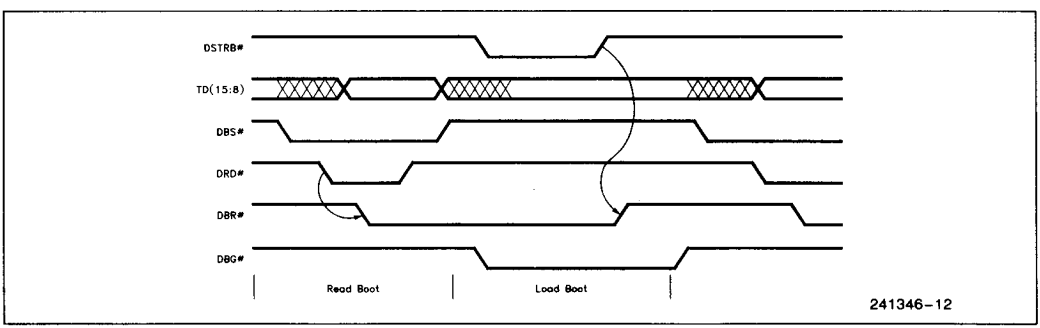


Figure 3-4. Boot Process

3.2.3 PROGRAM LOAD

Once the boot program is loaded it is possible to load the remainder of internal ADSP program memory with 16-bit transfers by using the Message to DSP Register (MDSP) and the Message to DVI Register (MDVI). ADSP data requests are made by writing to the MDVI Register. This creates an audio interrupt by asserting DVINT# on the DVI Bus if the DVI Device Interrupt Enable (DVIE) bit is set to a 1 in the DVI Device Command and Status Register (DCS). If the interrupt is not enabled, the DVINT bit in the DCS register can be polled by the DVI Device. In either case the DVI Device sets the DVINT bit to 0 (and resets the interrupt) by reading the MDVI Register and returns program data by writing to the MDSP Register. This causes the AINT bit in the Audio Command and Status Register to be set to a 1. It also causes the MINT# pin of the gate array to be asserted, but this pin is not presently used in the system. When the ADSP polls the ACS Register and finds the AINT bit set to a 1, it can set that bit to a 0 by reading the MDSP register and the whole process is repeated until the program transfer is complete.

3.2.4 VRAM DMA TRANSFERS

Whenever audio capture or playback takes place, data is transferred between the ADSP and VRAM using the KAGA DVI DMA interface. The timing for this transaction appears in Figure 3-5. As described in Section 2.1.3, the ADSP initiates a write access by first loading the VRAM destination into the write address registers and then loading the data into the WVR data registers, least significant word first. A read access is initiated by loading the VRAM access location into the read address registers, least significant word first. In either case, the gate array negates the DMA Ready (DFLAG) output and sets the DMARDY status bit in the DVI Control and Status Register (DCS) to a 0 at the trailing edge of the register load pulse to prevent further requests until the DMA cycle is complete. The trailing edge is used to insure that the data or address is stable before it appears on the DVI Bus. The gate array also asserts the Audio Request (AREQ#) signal to request control of the DVI Bus. When the assertion of both the Audio Select (ASEL#) and the Bus Enable (BUSEN#) signals are detected by KAGA, this indicates that the audio bus cycle is beginning and that AREQ# may be negated. It also enables KAGA to drive both the VRAM Write Enable (VWE#) line to indicate the type of cycle taking place and the DVI Data Bus (MD31–MD0) where address information is placed. Once the Gate Array Valid Latch Enable (GAVALEN) signal is detected and qualified by a positive transition on the V1CLK, the address is replaced by the data to be transferred on the (MD31–MD0) lines. During VRAM read cycles, the bus drivers are then tri-stated and, subsequently, the Memory Strobe (MSTRB#) signal, qualified by the V1CLK, is used to latch the read data into the RVR registers. For VRAM write cycles, the negation of the BUSEN# signal causes the bus drivers to be tri-stated and the DVI Data Bus relinquished. For both read and write cycles the negation of the BUSEN# signal causes the DFLAG pin and the DMARDY status bit in DCS to be asserted to allow new requests.

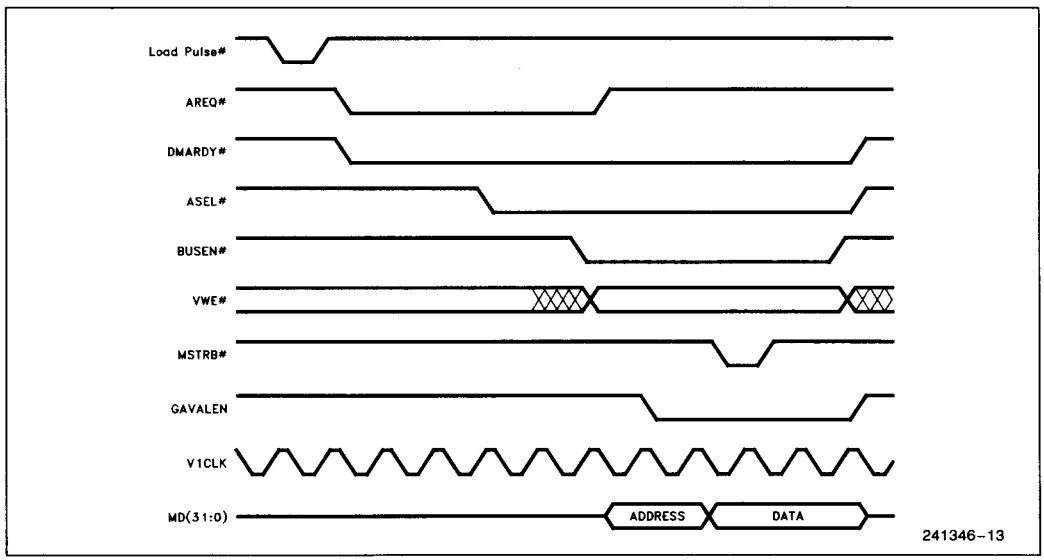


Figure 3-5. DMA Transfer Timing

3.2.5 AUDIO DATA CAPTURE

Data captured by the audio system in two's complement format is transferred serially to KAGA from a model CS5338 dual A/D Converter manufactured by Crystal Semiconductor. The source of all capture timing is a 16.9344 MHz crystal attached to pins XI and XO of the gate array. This oscillator is divided internally based on the (C5–C0) bits of the Sample Rate Command and Status Register (SRCS) and output to the converter as an input digital clock (ICLKD) which runs at 384 times the software-selected sample rate, F_S, of each channel. The Converter uses this frequency to operate a sharp cutoff digital filter which eliminates aliasing and to generate clocks, timing signals and data. Figure 3-2 shows the A/D interface signals. A timing diagram of these signals is shown in Figure 3-6. The Shift Clock (SCLK) is used to transfer serial data and runs at a frequency 64 × F_S. The Capture Left_Right signal is a 1 when right channel audio is being transferred. The Frame Sync (FSYNC) is a 1 when data on the Data In (DIN) line is active. The Capture Interrupt (CINT#) signal is asserted each time new data is available in the Capture Audio Registers (CAL/CAR). It is negated when the ADSP reads either register.

3.2.6 AUDIO DATA PLAYBACK

Data output by the audio system in two's complement format is transferred serially from KAGA to a model PCM66 dual D/A Converter manufactured by Burr Brown. The source of all Playback timing is the same 16.9344 MHz crystal used for audio capture. This oscillator is divided internally based on the (P5–P0) bits of the Sample Rate Command and Status Register (SRCS). It is then output to the Converter as a Bit Rate Clock (BCLK) which runs at 32 times the software-selected sample rate, F_S, of each channel and is used to transfer serial data. Figure 3-2 shows D/A interface signals. A timing diagram of these signals is shown in Figure 3-7. The gate array also generates Word Clock (WDCLK) and Play Left_Right (PLAYL_R) signals for the Converter in addition to the output data (DOUT). WDCLK is a square wave at frequency 2 × F_S, which is a 0 at the beginning of each output word. PLAYL_R is a square wave at frequency F_S and is a 1 when right channel audio is being transferred. A Playback Interrupt signal (PINT#) is asserted by KAGA each time new data may be transferred to the Playback Audio Registers (CPAR/CPAL). It is negated when the ADSP writes to either of these registers.

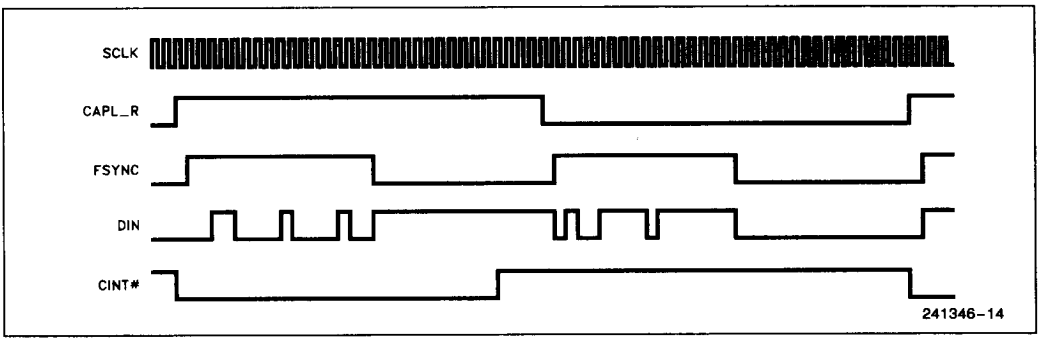


Figure 3-6. Audio Capture Timing

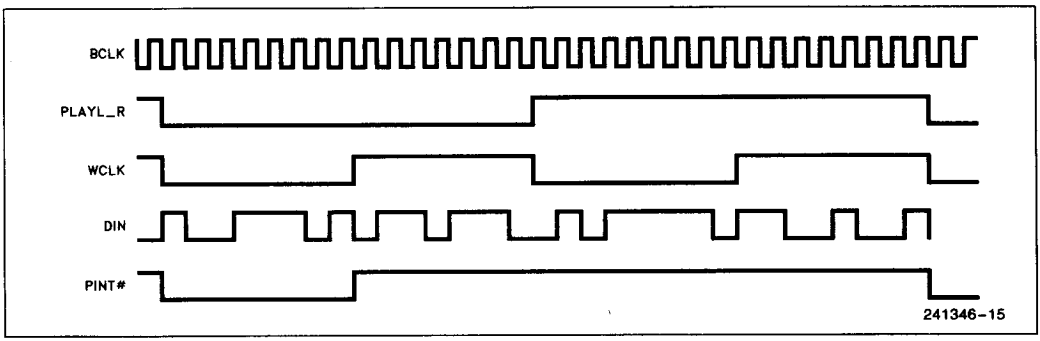


Figure 3-7. Audio Playback Timing

3.3 Keying and Genlock

A diagram of the KAGA interconnections relating to the Keying and Genlock Subsystems is shown in Figure 3-7. These signals will be described in conjunction with various operations performed by these subsystems.

3.3.1 VIDEO SYNC SELECTION

The gate array incorporates two Video Sync Muxes to develop a Horizontal (HSYNC) and Vertical (VSYNC) output which synchronize the output video to a monitor. The HSYNC output is selected under software control from DB Horizontal Sync (DB__HSYNC), DB Composite Sync (DB__CSYNC), VGA Horizontal Sync (VGA__HSYNC) and RGB Horizontal Sync (RGB__HSYNC). The VSYNC output is selected under software control from DB Vertical Sync (DB__VSYNC), VGA Vertical Sync (VGA__VSYNC) and RGB Vertical Sync (RGB__VSYNC). The outputs may be logically inverted within the array to simplify display device compatibility.

3.3.2 DISPLAY PROCESSOR SYNCHRONIZATION

The gate array produces a Horizontal (DB__HRST) and Vertical (DB__VRST) Reset signal to synchronize the Display Processor to a choice of input sources. DB__VRST is selected by a software-controlled multiplexer whose inputs are VGA__VSYNC, RGB__VSYNC, and Capture Vertical Sync (CAP__VSYNC). The DB__HRST output is the same as the Reference input to the Phase Detector in the Phaselock Loop. When the Loop is genlocked, this output is synchronous with the Horizontal Reference selected by the Phaselock Loop Reference Mux.

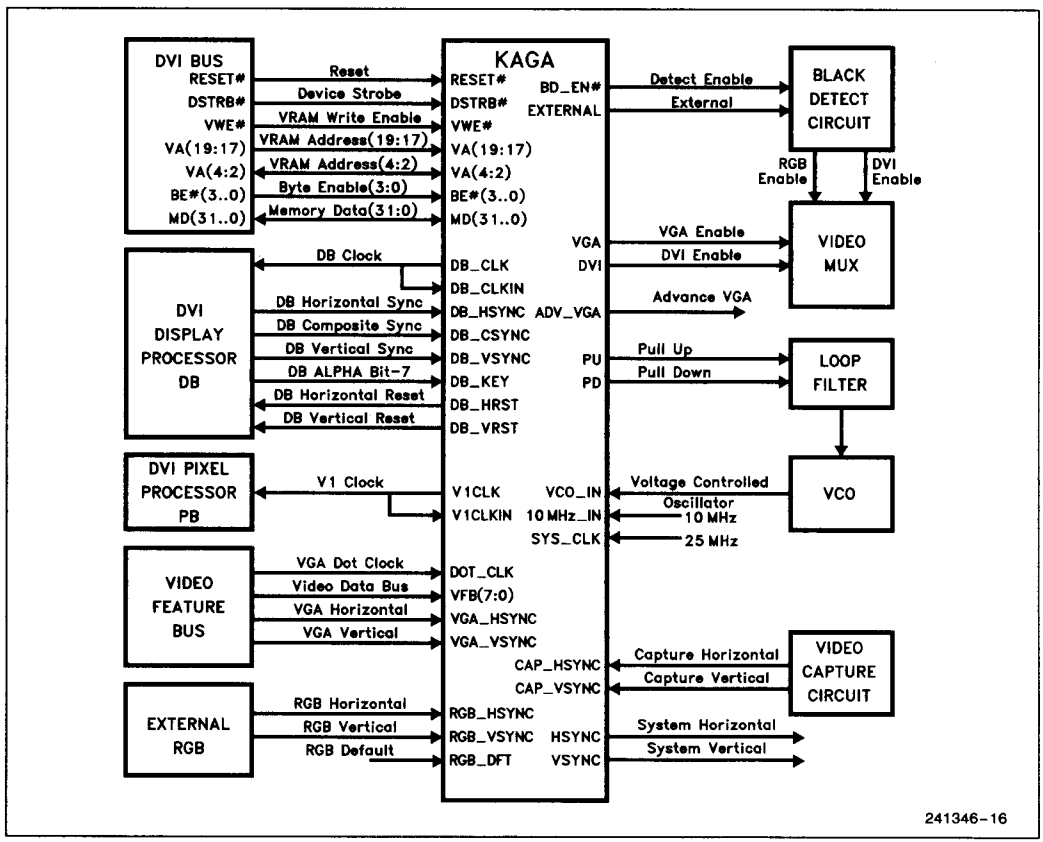


Figure 3-8. KAGA Keying and Genlock Interconnections

3.3.3 SYNCHRONIZING THE DISPLAY PROCESSOR

In order to genlock the DVI Video to another video source or to synchronize it to a crystal clock, the internal Phaselock Loop is used. Its Reference Frequency is selected by the Phaselock Loop Reference Mux from the following signals: VGA_HSYNC, RGB_HSYNC, Capture Horizontal Sync (CAP_HSYNC) and a divided down version of an input clock (10MHZ_IN). This is compared in the Phase Detector with a divided down version of the Voltage Controlled Oscillator Frequency (VCO_IN) to produce the phase error signals, Pull Up (PU1) and Pull Down (PD1). These outputs have several configurations described in Section 4.2.5.

3.3.4 PB AND DB CLOCK SELECTION

There are six clocks which can be independently selected to generate clocks for PB (PBCLK) and DB (DBCLK). These are VCO_IN, an internal clock at half the frequency of VCO_IN, 10MHZ_IN, the VGA Dot Clock (DOT_CLK), the internal audio clock at 16.9344 MHz and the 25 MHz System Clock (SYS_CLK). PBCLK and DBCLK are input back into the array on pins PBCLKIN and DBCLKIN for synchronization of DVI System and Display System signals.

3.3.5 VIDEO KEYING

The KAGA gate array interfaces with an external Video Multiplexer, DB, the Video Feature Bus and a Black Detect Circuit in order to implement Keying. The interconnections are shown in Figure 3-8. The Multiplexer is capable of instantaneously switching any one of its three inputs, DVI, VGA or RGB Video, to its output, depending on state of the control signals from KAGA and the Black Detect Circuit. The three control signals DVI, VGA and EXTERNAL are mutually exclusive and, when asserted, cause the Multiplexer to pass the DVI, VGA or External RGB Video respectively. In Keying Modes 0, 4 and 5 (see Section 4.2.7) only one of these signals is enabled and no video keying takes place. In Keying Modes 2 and 3 it is KAGA's responsibility to switch the DVI and VGA outputs to effect the video keying. The information used to make this decision is derived from the data lines of the Video Feature Bus, (VFB7–VFB0), the keying signal from the Display Processor (DB_Key) and the contents of the Chroma Key Value Register. In Keying Mode 6, the Black Detect Enable (BD_EN#) signal is asserted low by the gate array and the Black Detect Circuit has the responsibility of switching the DVI and RGB outputs to effect video keying. BD_EN# is asserted in Keying Mode 5, as well, simplifying the external logic. The control signal information is summarized in Figure 3-9.

Keying Mode	EXTERNAL	BD_EN#	VGA	DVI
0	0	1	0	1
1	Reserved for Future Use			
2	0	1	0 When VGA KEY = 1 1 When VGA KEY = 0	1 When VGA KEY = 1 0 When VGA KEY = 0
3	0	1	0 When VGA KEY & DB_KEY = 1 1 When VGA KEY & DB_KEY = 0	1 When VGA KEY & DB_KEY = 1 0 When VGA KEY & DB_KEY = 0
4	0	1	0	1
5	1	0	0	0
6	0	0	0	0
7	Reserved for Future Use			

Figure 3-9. Keying Control Signals

Two other signals are involved in the video keying. The first, Advance VGA (ADV__VGA), is an input which when grounded causes Keying Mode 0 to be the power-on default state. If the pin is tied to Vcc or left floating, then Keying Mode 5 is the power-on default state. The second, RGB Default (RGB__DFT), is an output which is a combination of the information found on the VGA and DVI pins, but slightly earlier in time. Using it as the D input to a flip-flop clocked by the rising edge of DOT__CLK will make the timing the same as the other two outputs. However, if DVI and VGA are used, this signal is unnecessary.

One further piece of information about the use of this chip is that the DVI and VGA control signals appear one cycle of DOT__CLK too early at the output pins to properly key the video. This can be corrected with two D flip-flops as shown in Figure 3-10.

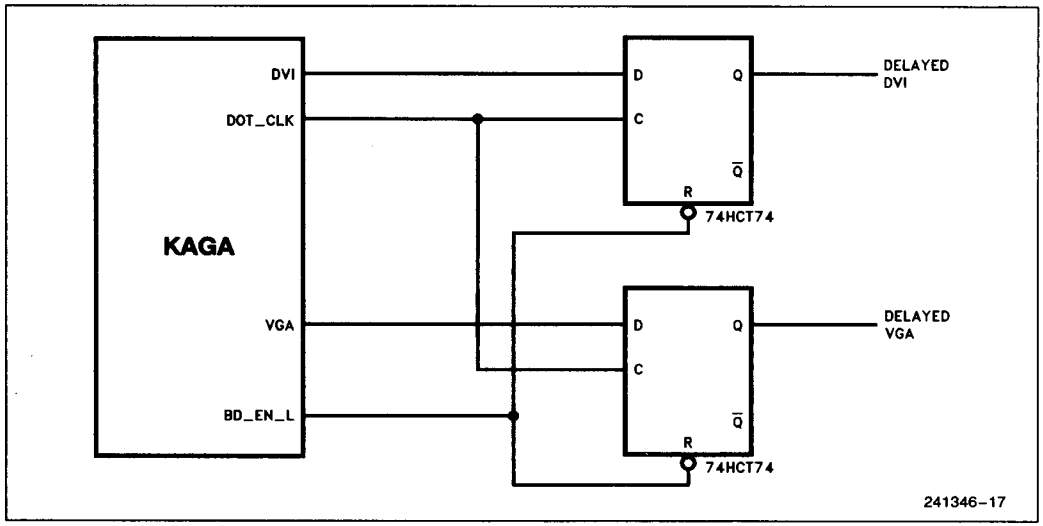


Figure 3-10. DVI and VGA Keying Delay Circuit

4.0 PROGRAMMING INFORMATION

4.1 Audio

This section describes the details of the 18 audio registers addressable from the DVI and the ADSP Buses.

4.1.1 AUDIO COMMAND AND STATUS REGISTER (ACS)

The Audio Command and Status Register is a 16-bit ADSP read-write register. Figure 4-1 identifies each bit of this register as well as its accessibility. Writing data to read-only locations has no effect.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AINT	DVINT	DMARDY	TEST	CINT	PINT	0	VSYNC	0	0/1	RAUTO	WAUTO	BE3	BE2	BE1	BE0
R	R	R	R/W	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 4-1. Audio Command and Status Register

AINT—Audio Interrupt (Bit 15)

This read-only bit, when set to a 1, indicates that a message has been sent to the MDSP Register from a DVI Device. The ADSP clears this bit by reading the MDSP register.

DVINT—DVI Device Interrupt (Bit 14)

This read-only bit, when set to a 1, indicates that the ADSP has written a message to the MDVI Register (causing an audio interrupt if the DVI Device Interrupt Enable (DVIE) bit is set to a 1 in the DVI Device Command and Status Register (DCS)). The bit is cleared and the audio interrupt disabled by a DVI Device reading the MDVI Register. This interrupt mechanism is primarily intended for use by the Host Computer but could be configured to be used by other DVI devices.

DMARDY—DMA Ready (Bit 13)

This read-only bit, when set to a 1, indicates that the ADSP may execute an audio DMA read or write operation.

TEST—Loop Test Mode (Bit 12)

This read-write bit, when set to a 1, indicates that the audio input/output circuitry is in the loop back mode. In this mode, serially shifted data intended for the output D/A converter is additionally routed within KAGA to the A/D input serial shift register. In the process, left and right channel data are transposed.

CINT—Audio Capture Interrupt (Bit 11)

This read-only bit, when set to a 1, indicates that audio data from the Audio A/D converter resides in the Capture/Playback Audio Registers (CPAL/CPAR) and the CINT# output pin of the gate array is asserted (generating an ADSP interrupt if enabled within the ADSP). The bit is cleared when the ADSP reads either the CPAL or CPAR.

PINT—Audio Playback Interrupt (Bit 10)

This read-only bit, when set to a 1, indicates that audio data to the Audio D/A converter can be sent to the Capture/Playback Audio Registers (CPAL/CPAR) and the PINT# output pin of the gate array is asserted (generating an ADSP interrupt if enabled within the ADSP). The bit is cleared when the ADSP writes to either the CPAL or CPAR.

VSYNC—Vertical Sync (Bit 8)

This read-only bit, when set to a 1, indicates that the DB Vertical Sync is asserted.

Bit 6

This bit is a general purpose read-write bit.

RAUTO—Read Address Auto-Increment Mode (Bit 5)

This read-write bit, when set to a 1, will increment the address pointer in the VRAM Read Address Register (RVRADD0 and RVRADD1) by 4 (a double word) at the end of each audio DMA read cycle. Another read cycle will be initiated when the Most Significant VRAM Data Register (VRDAT1) is read. If RAUTO is set to a 0 the pointer will be unaffected by data reads and a DMA read cycle will consist of an address write followed by a data read.

WAUTO—Write Address Auto-Increment Mode (Bit 4)

This read-write bit, when set to a 1, will increment the address pointer in the VRAM Write Address Register (WVRADD0 and WVRADD1) by 4 (a double word) at the end of each audio DMA write cycle. Another write cycle will be initiated when the Most Significant VRAM Data Register (WVR1) is written. If WAUTO is set to a 0 the pointer will be unaffected by address writes and a DMA write cycle will consist of a data write followed by an address write.

BE3–BE0—Byte Enables for VRAM and DVI Device Accesses (Bits 3:0)

These read-write bits determine which of the four bytes on the DVI bus are enabled during a bus transaction. Thus, they control whether the access involves a byte, word or long word.

4.1.2 MESSAGE TO DVI REGISTER (MDVI)

The MDVI Register is a 16-bit read-write ADSP register but is read-only by a DVI Device. When the register is written, the DVINT bit is set to a 1 in the Audio Command and Status Register (ACS) and the DVI Device Command and Status Register (DCS). This creates an audio interrupt if the DVI Device Interrupt Enable (DVIE) bit is set to a 1 in the DVI Device Command and Status Register (DCS). The DVINT bit is cleared and the audio interrupt disabled by a DVI Device reading the MDVI Register.

4.1.3 MESSAGE TO DSP REGISTER (MDSP)

The MDSP Register is a 16-bit read-write DVI register but is read-only by the ADSP. When the register is written, the AINT bit is set to a 1 in both the Audio Command and Status (ACS) Register and the DVI Device Command and Status Register (DCS). The AINT bit is cleared by the ADSP reading the MDSP Register.

4.1.4 SAMPLE RATE COMMAND AND STATUS REGISTER (SRCS)

This Sample Rate Command and Status Register is a 16-bit read-write ADSP register. Figure 4-2 identifies each bit of this register as well as its accessibility. Writing data to read-only locations has no effect.

C5–C0—Capture Sample Rate (Bits 13:8)

These bits control the rate at which audio samples are taken by the A/D converter. The sample rate (F_S) is determined by the formula:

$$F_S = \frac{44.1\ KHz}{C + 1}$$

where:

$0 \leq C \leq 63$

C is the value C5:C0

P5–P0—Capture Sample Rate (Bits 5:0)

These bits control the rate at which audio samples are output to the D/A converter. The sample rate (F_S) is determined by the formula:

$$F_S = \frac{529.2\ KHz}{P + 1}$$

where:

$1 \leq P \leq 63$

P is the value P5:P0

P = 0 turns off the playback sample rate clock.

4.1.5 VRAM DATA REGISTERS (VRDAT0, VRDAT1)

The Least and Most Significant VRAM Data Registers are each 16-bit ADSP read-write registers used together to transfer up to 32-bit data words between the ADSP and VRAM on the DVI Bus. Data is transferred to the DVI Bus at the address stored in the VRAM Write Address Registers (WVRADD0, WVRADD1) whenever data is written to VRDAT1.

4.1.6 CAPTURE/PLAYBACK AUDIO REGISTERS (CPAR, CPAL)

The Right and Left Capture/Playback Registers are each 16-bit ADSP read-write registers used to transfer data between the ADSP and the D/A or A/D converters. Each time the Audio Capture Rate Counter counts to completion, 32 bits of data are transferred from the Audio Capture Serial-to-Parallel Converters to the Left and Right Capture Audio Registers and the Capture Interrupt (CINT) bit is set to a 1 in the Audio Command and Status Register (ACS). Similarly, each time the Audio Playback Rate Counter counts to completion, 32 bits of data are transferred from the Left and Right Playback Audio Registers to the Audio Playback Parallel-to-Serial Converters and the Playback Interrupt (PINT) is set to a 1 in the ACS Register. Figure 4-3 shows a hardware block diagram of the A/D and D/A interface. Even though the Audio Capture and Playback Registers are distinct hardware entities, the first is read-only and the second write-only by the ADSP and it is convenient to group them together and assign them one bus address.

4.1.7 VRAM WRITE ADDRESS REGISTERS (WVRADD0, WVRADD1)

The Least and Most Significant VRAM Write Address Registers are each 16-bit ADSP read-write registers used together to create a 32-bit write address pointer into the DVI Device Bus space. Up to 32 bits of data in the VRAM Data Registers (VRDAT0, VRDAT1) is written to this pointer location when the ADSP writes to the VRDAT1 Register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	C5	C4	C3	C2	C1	C0	0	0	P5	P4	P3	P2	P1	P0
R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Figure 4-2. Sample Rate Command and Status Register

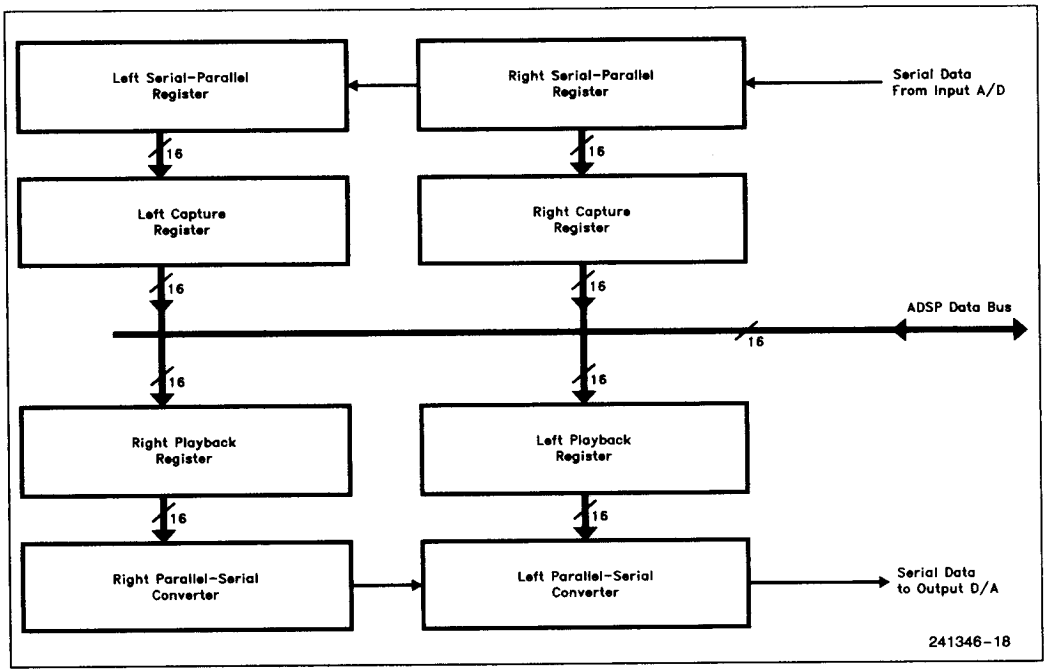


Figure 4-3. Audio A/D and D/A Interface Registers

4.1.8 VRAM READ ADDRESS REGISTERS (RVRADD0, RVRADD1)

The Least and Most Significant VRAM Read Address Registers are each 16-bit ADSP read-write registers used together to create a 32-bit read address pointer into the DVI Device Bus space. Up to 32 bits of data is loaded into the VRAM Data Registers (VRDAT0, VRDAT1) from this pointer location when the ADSP writes to the RVADD1 Register.

4.1.9 DVI COMMAND AND STATUS REGISTER (DCS)

The DVI Command and Status Register is a 16-bit DVI Bus read-write register. Figure 4-4 identifies each bit of this register as well as its accessibility. Writing data to read- only locations has no effect.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FO	HIE	DVINT	AINT	AREQ	BR	BG	ARST	0	0	0	0	0	0	0	BRDY
R	R/W	R	R	R	R/W	R	R/W	R	R	R	R	R	R	R	R

Figure 4-4. DVI Command and Status Register

FO—Flag Out (Bit 15)

This read-only bit indicates the status of the Flag Out pin of the ADSP. It is controllable in software by the audio processor and may be used to signal events to the DVI Device.

DVIE—Host Interrupt Enable (Bit 14)

This read-write bit controls whether the assertion of the DVI Device Interrupt (DVINT) bit will create an audio interrupt on the DVI Bus. DVIE = 1 enables the interrupt; DVIE = 0 disables it. The interrupt enable bit powers up in the 0 state.

DVINT—DVI Device Interrupt (Bit 13)

This read-only bit, when set to a 1, indicates that the ADSP has written a message to the MDVI Register (causing an audio interrupt if the DVI Device Interrupt Enable (DVIE) bit is set to a 1). The bit is cleared and the audio interrupt disabled by a DVI Device reading the MDVI Register. This interrupt mechanism is primarily intended for use by the Host Computer but could be configured to be used by other DVI devices.

AINT—Audio Device Interrupt (Bit 12)

This read-only bit, when set to a 1, indicates that a message has been sent to the MDSP Register from a DVI Device. The ADSP clears this bit by reading that register.

AREQ—Audio Request (Bit 11)

This read-only bit, when set to a 1, indicates that the AREQ# output pin on the gate array is asserted and there is a pending request by KAGA to perform an audio data transfer on the DVI Bus. When the transfer is completed, the bit is negated.

BR—Bus Request (Bit 10)

This read-write bit, when set to a 1 by any DVI Device, asserts the BR# pin of the gate array, requesting the ADSP to relinquish control of its bus. This is used primarily during the ADSP boot process where the Host serves as the boot ROM and loads ADSP program memory in single-step mode using this signal.

BG—Bus Grant (Bit 9)

This read-only bit, when set to a 1, indicates that the ADSP has asserted the DBG# pin of the gate array and has relinquished control of the audio bus.

ARST—ADSP Reset (Bit 8)

This read-write bit, when set to a 1, indicates that DRST# pin of the gate array has been asserted, resetting the ADSP.

BRDY—Bus Ready (Bit 0)

This read-only bit, when set to a 1, indicates that the DBS# pin of the gate array has been negated, signifying the end of a boot memory load cycle. At this time a new byte of data may be loaded into the BOOT Register by the DVI Device.

4.2 Keying and Genlock

This section describes the details of the 7 Keying and Genlock registers addressable from the DVI Bus and how they are used in the system.

4.2.1 N MODULUS REGISTER (NMOD)

The N Modulus Register is a 16-bit DVI Bus read-write register. Figure 4-5 identifies each bit of this register as well as its accessibility. The ÷N Counter divides the 10 MHz reference frequency by the quantity (NMOD + 2) so long as the register contents are 8 or greater. (The N0 bit is always interpreted by the counting circuitry as a 0 regardless of the state of stored value. This results in the modulus always being even.) If the contents of NMOD are less than 8, the output of the N Counter will be non-oscillatory. Writing to read-only locations has no effect. This register is set to 200H upon reset.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 4-5. N Modulus Register

4.2.2 M MODULUS REGISTER (MMOD)

The M Modulus Register is a 16-bit DVI Bus read-write register. Figure 4-6 identifies each bit of this register as well as its accessibility. The ÷M Counter divides the Voltage Controlled Oscillator (VCO) frequency by the quantity (MMOD + 2) so long as the register contents are 8 or greater. (The M0 bit is always interpreted by the counting circuitry as a 0 regardless of the state of stored value. This results in the modulus always being even.) If the contents of MMOD are less than 8, the output of the M Counter will be non-oscillatory. Writing to read-only locations has no effect. This register is set to 200H upon reset.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 4-6. M Modulus Register

4.2.3 N COUNTER REGISTER (NCTR)

The N Counter Register is a 16-bit DVI Bus read-only register which contains the instantaneous value of the N Counter. Figure 4-7 identifies each bit of this register as well as its accessibility. Writing to this register has no effect.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Figure 4-7. N Counter Register

4.2.4 M Counter Register (MCTR)

The M Counter Register is a 16-bit DVI Bus read-only register which contains the instantaneous value of the M Counter. Figure 4-8 identifies each bit of this register as well as its accessibility. Writing to this register has no effect.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Figure 4-8. M Counter Register

4.2.5 GENLOCK COMMAND AND STATUS REGISTER (GCSR)

The Genlock Command and Status Register is a 32-bit DVI Bus read-write register use to control and monitor the parameters involved in synchronizing the DVI Display Processor (DB) to various sources of video timing. Figure 4-9 identifies each bit of these registers and its accessibility.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GSEL	IVS	IHS	SCMP	SDB	HREN	VREN	NEVS	UPBC	PBC2	PBC1	PBC0	UDBC	DBC2	DBC1	DBC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	IDMC	IDNC	PDM1	PDM0	SCAP	SEXT	IVRS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 4-9. Genlock Command and Status Register

IDMC—Invert Divider M Counter (Bit 22)

This read-write bit selects the edge of the Voltage Controlled Oscillator waveform that is used to increment the ÷M Counter. The default for this bit is 0 which selects the rising edge. If the bit is set to a 1, the falling edge is selected.

IDNC—Invert Divider N Counter (Bit 21)

This read-write bit selects the edge of the 10 MHz Reference Oscillator Waveform that is used to increment the ÷N Counter. The default for this bit is 0 which selects the rising edge. If the bit is set to a 1, the falling edge is selected.

PDM1–PDM0—Phase Detector Mode (Bits 20:19)

These read-write bits control the Phase Detector mode of operation. There are four modes of operation:

Mode 0 is the default mode. In this mode, if the two Phase Detector inputs are coincident, the output pins are tri-stated. If the VCO input lags the Reference, the PU1 output pin will go active high during the lag time. If the VCO input leads the Reference, the PD1 output pin will go active high during the lead time.

Mode 1 bypasses the internal Phase Detector, bringing the VCO input to the PD1 output pin and the Reference to the PU1 output pin. This allows the use of an external phase detector.

In Modes 2 and 3 the outputs of the internal Phase Detector always drive the output pins. In Mode 2 if the two Phase Detector inputs are coincident, the output pins are both low. If the VCO input lags the Reference, the PU1 output pin will go high during the lag time. If the VCO input leads the Reference, the PD1 output pin will go high during the lead time. In Mode 3 the outputs are inverted from Mode 2.

SCAP—Select Capture (Bit 18)

This read-write bit together with bits SEXT and GSEL determines the Reference input to the Phase Detector and the signal selected for Vertical Reset of the DB as shown in Figure 4-10. The default for this bit is 0.

SEXT—Select External RGB (Bit 17)

This read-write bit together with bits SCAP and GSEL determines the Reference input to the Phase Detector and the signal selected for Vertical Reset of the DB as shown in Figure 4-10. Additionally, together with bits SCMP and SDB, it determines the horizontal and vertical inputs selected for the Video Sync Outputs as shown in Figure 4-11. The default for this bit is 0.

IVRS—Invert Reference Source (Bit 16)

When this read-write bit is set to a 1 the Reference Input to the Phase Detector is inverted. When the bit is set to a 0 no inversion takes place. The default for this bit is 0.

GSEL—Genlock Select (Bit 15)

This read-write bit together with bits SCAP and SEXT determines the Reference input to the Phase Detector and the signal selected for Vertical Reset of the DB as shown in Figure 4-10.

IVS—Invert Vertical Sync (Bit 14)

When this read-write bit is set to a 1 the Vertical Sync output (VSYNC) is inverted. When the bit is set to a 0 no inversion takes place. The default for this bit is 0.

IHS—Invert Horizontal Sync (Bit 13)

When this read-write bit is set to a 1 the Horizontal Sync output (HSYNC) is inverted. When the bit is set to a 0 no inversion takes place. The default for this bit is 0.

SCMP—Select Composite (Bit 12)

This read-write bit together with bits SEXT and SDB determines the horizontal and vertical inputs selected for the Video Sync Outputs as shown in Figure 4-11. The default for this bit is 0.

SDB—Select Display Processor (DB) (Bit 11)

This read-write bit together with bits SEXT and SCMP determines the horizontal and vertical inputs selected for the Video Sync Outputs as shown in Figure 4-11. The default for this bit is 0.

SCAP (18)	SEXT (17)	GSEL (16)	Reference	DB_VRST
0	0	0	I0MHZ_N	VGA_VSYNC
0	0	1	VGA_HSYNC	VGA_VSYNC
0	1	X	RGB_HSYNC	RGB_VSYNC
1	X	X	CAP_HSYNC	CAP_VSYNC

Figure 4-10. Phase Detector Reference and Vertical Reset Select

SCMP (12)	SEXT (17)	SDB (11)	HSYNC	VSYNC
0	0	0	VGA_HSYNC	VGA_VSYNC
0	X	1	DB_HSYNC	DB_VSYNC
0	1	0	RGB_HSYNC	RGB_VSYNC
1	0	0	DB_CSYNC	VGA_VSYNC
1	X	1	DB_CSYNC	DB_VSYNC
1	1	0	DB_CSYNC	RGB_VSYNC

Figure 4-11. Horizontal and Vertical System Sync Select

HREN—Horizontal Reset Enable (Bit 10)

When this read-write bit is set to a 1 the Horizontal Reset to the DB is enabled. The reset is used to align the lines of video produced by the DB with various video sources. When the bit is set to a 0 the output is disabled. The default for this bit is 0.

VREN—Vertical Reset Enable (Bit 9)

When this read-write bit is set to a 1 the Vertical Reset to the DB is enabled. The reset is used to align the fields of video produced by the DB with various video sources. When the bit is set to a 0 the output is disabled. The default for this bit is 0.

NEVS—Negative Edge of Vertical Sync (Bit 8)

This read-write bit selects the edge of the selected Vertical Sync input waveform that is used to assert the Vertical Sync Reset to the DB. The default for this bit is 0, which selects the rising edge. If the bit is set to a 1, the falling edge is selected.

UPBC—Update PB Clock (Bit 7)

When a 1 is written to this read-write bit, the selection of the PB clock source (PBC2–PBC0) is updated. The bit immediately returns to the 0 state.

PBC2–PBC0—PB Clock Select (Bits 6:4)

This three-bit field selects the PB clock source when the UPBC input makes a positive transition as shown in Figure 4-12. The default for this field is 0.

PBC2 (6)	PBC1 (5)	PBC0 (4)	PB Clock Source
0	0	0	10MHZ_IN
0	0	1	VCO_IN
0	1	0	10MHZ_IN
0	1	1	16.9344 MHz
1	0	0	VCO_IN + 2
1	0	1	10MHZ_IN
1	1	0	DOT_CLK
I	1	1	SYS_CLK

Figure 4-12. PB Clock Source Selection

UDBC—Update DB Clock (Bit 3)

When a 1 is written to this read-write bit, the selection of the DB clock source (DBC2–DBC0) is updated. The bit immediately returns to the 0 state.

DBC2–DBC0—DB Clock Select (Bits 2:0)

This three-bit field selects the DB clock source when the UDBC input makes a positive transition as shown in Figure 4-13. The default for this field is 0.

DBC2 (2)	DBC1 (1)	DBC0 (0)	DB Clock Source
0	0	0	10MHZ_IN
0	0	1	VCO_IN
0	1	0	10MHz_IN
0	1	1	16.9344 MHz
1	0	0	VCO_IN + 2
1	0	1	10MHZ_IN
1	1	0	DOT_CLK
1	1	1	SYS_CLK

Figure 4-13. DB Clock Source Selection

4.2.6 CHROMA KEYING VALUE REGISTER (CKVAL)

The Chroma Keying Value Register is an 8-bit DVI Bus read-write register which contains a value which is continuously compared with the pixel values on the Video Feature Bus. If VGA Keying is selected (see Section 4.2.7) and the values match, the output from the Display Processor is substituted for the VGA video for that pixel.

4.2.7 KEYING MODE SELECT REGISTER (KMSEL)

The Keying Mode Select Register is an 8-bit DVI Bus read-write register which determines whether a single video source or the keying of RGB or VGA with DVI video will make up the system video output. Figure 4-14 identifies each bit of this register as well as its accessibility.

7	6	5	4	3	2	1	0
0	0	0	0	XDFT	MS2	MS1	MS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 4-14. Keying Mode Select Register

XDFT—External RGB Default Mode (Bit 3)

This bit reflects the state of the RGB_DFT pin on the gate array. If this pin is tied to ground, the bit will display as a 0 and Keying Mode 0 (see below) is the power-on default state. If the pin is tied to V_{CC} or left floating, then Keying Mode 5 is the power-on default state.

MS2..MS0—Mode Selects (Bits 2:0)

This 3-bit field selects one of eight keying modes as shown in Figure 4-15 and described below.

Keying Mode	MS2	MS1	MS0	Video with Key = 0	Video with Key = 1	Keying Signal
0	0	0	0	VGA	—	N/A
1	0	0	1	Reserved for Future Use		
2	0	1	0	VGA	DVI	VGA Key
3	0	1	1	VGA	DVI	VGA Key and DB_Key
4	1	0	0	DVI	—	N/A
5	1	0	1	RGB	—	N/A
6	1	1	0	RGB	DVI	Black Detect
7	1	1	1	Reserved for Future Use		

Figure 4-15. Keying Modes

In Mode 0, VGA is the unconditional source of the video output. It is the default mode when the RGB__DFT pin on the gate array is tied to ground.

Mode 1 is reserved for future use and is not presently defined.

In Mode 2, VGA Video is selected unless the pixel value matches the byte in the Chroma Key Value Register (CKVAL) at which time DVI video is selected.

In Mode 3, VGA video is selected unless the pixel value matches the byte in the Chroma Key Value Register (CKVAL) and the DB__Key pin on the array is asserted at which time DVI video is selected.

In Mode 4, DVI is the unconditional source of the video output.

In Mode 5, RGB is the unconditional source of the video output. It is the default mode when the RGB__DFT pin on the gate array is tied to V_{CC} or left floating.

In Mode 6, RGB video is selected unless the external analog Black Detect circuit determines that the RGB value is near black, at which time DVI video is selected.

Mode 7 is reserved for future use and is not presently defined.

4.2.8 COMMON SYSTEM CONFIGURATIONS

Although the Genlock Command and Status Register provides many possibilities for signal selection, the following eight combinations shown in Figure 4-16 (ignoring some signal inversions) are the most logical alternatives:

Case A

This is a mode in which the Display Processor generates the entire image and is not overlaid with any other video. It is the source of the horizontal and vertical timing. The ÷N is selected as the genlock source and the VCO drives the DB clock without any restraints. (The ÷N should be chosen even if the VCO is not the source for the DB clock since it is the only phaselock loop reference guaranteed to be present.) The HREN and VREN bits are both set to 0 since the DB is not genlocked to a source. The IVS and IHS bits are set to provide inverted syncs to output monitors.

Case B

This is a mode where the Display Processor generates an image that is overlaid with VGA video. In this mode the DB clock source must originate from the VCO which is phaselocked to the VGA Horizontal Sync. The VGA Horizontal and Vertical Syncs are selected as the DB Resets as well as the system output synchronization. The HREN and VREN bits are set to 1 in order to allow those resets to synchronize the DB to the VGA frame. The IVS and IHS bits are set to 0 since both the Video Feature Bus input and the output monitors most likely use active low syncs.

Case C

This mode is identical to case B except that the output Horizontal and Vertical Syncs originate from the DB. Since the DB outputs positive-going sync pulses, it is necessary to set the IVS and IHS bits to a 1.

	GCSR (15:0)	SCAP	SEXT	GSEL	SCMP	SDB	VSYNC	HSYNC	Reference Source	DB__VRST	DB__HRST
A	68	0	0	0	0	1	DB__VSYNC	DB__HSYNC	÷N	OFF	OFF
B	86	0	0	1	0	0	VGA__VSYNC	VGA__HSYNC	VGA__HSYNC	VGA__VSYNC	÷M
C	EE	0	0	1	0	1	DB__VSYNC	DB__HSYNC	VGA__HSYNC	VGA__VSYNC	÷M
D	206	0	1	0	0	0	RGB__VSYNC	RGB__HSYNC	RGB__HSYNC	RGB__VSYNC	÷M
E	26E	0	1	0	0	1	DB__VSYNC	DB__HSYNC	DB__HSYNC	DB__VSYNC	÷M
F	27E	0	1	0	1	1	DB__VSYNC	DB__CSYNC	RGB__HSYNC	RGB__VSYNC	÷M
G	46E	1	0	0	1	1	DB__VSYNC	DB__HSYNC	CAP__HSYNC	CAP__VSYNC	÷M
H	47E	1	0	0	1	1	DB__VSYNC	DB__CSYNC	CAP__HSYNC	CAP__VSYNC	÷M

Figure 4-16. Common System Configurations

Case D

This is a mode where the Display Processor generates an image that is overlaid with RGB video. In this mode the DB clock source must originate from the VCO which is phaselocked to the RGB Horizontal Sync. The RGB Horizontal and Vertical Syncs are selected as the DB Resets as well as the system output synchronization. The HREN and VREN bits are set to 1 in order to allow those resets to synchronize the DB to the RGB frame. The IVS and IHS bits would probably be set to 0 since RGB syncs are likely to be the correct polarity.

Case E

This mode is identical to case D except that the output Horizontal and Vertical Syncs originate from the DB. Since the DB outputs positive-going sync pulses, it is necessary to set the IVS and IHS bits to a 1.

Case F

This mode is identical to case E except that Composite Horizontal Sync is selected from the DB.

Case G

This is a mode in which the DB generates the entire image but is still genlocked to an external source, Capture Horizontal and Video. The Capture Horizontal is the genlock reference and the Vertical is used to reset the DB. However, the DB Horizontal and Vertical Syncs are used as the system output.

Case H

This mode is identical to case G except that Composite Horizontal Sync is selected from the DB.

5.0 ELECTRICAL SPECIFICATIONS

5.1 DC Characteristics

Table 5-1 contains stress ratings only, and functional operation at the maximums is not guaranteed. Exposure to Maximum Ratings may affect device reliability. Furthermore, although the 82750LA contains protective circuitry to resist damage from static electrical discharge, this device is sensitive to ESD levels above 1000V. Always take precautions to avoid high static voltages or electric fields.

Table 5-1. Maximum Ratings

Condition	Maximum Requirement
Maximum Operating Junction Temperature	100°C
Storage Temperature	−65°C to ÷150°C
Voltage on Any Pin with Respect to Ground	−0.5V to 7V
Supply Voltage with Respect to V_{SS}	−0.5V to 7V
Input Current Clamp ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output Current Clamp ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous Output Current Low	20 mA
Continuous Output Current High	20 mA

Table 5-2. Recommended Operating Conditions

Parameter	Recommended Condition		
	Min	Nom	Max
Supply Voltage (V_{CC})	4.50V	5.00V	5.50V
Operating Temperature Range	0°C		70°C

Table 5-3. DC Characteristics V_{CC} = 5V, T_{CASE} = 25°C

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input LOW Voltage			0.8	V	V_{CC} = 4.5V
V_{IH}	Input HIGH Voltage	2.0			V	V_{CC} = 5.5V
V_{OL}	Output LOW Voltage			0.5	V	V_I = 0.1 V_{CC}, I_{OL} = 4 mA
V_{OH}	Output HIGH Voltage	3.7			V	V_I = 0.9 V_{CC}, I_{OH} = 4 mA
I_{IL}	Input Leakage Current		−70		μA	V_{IL} = 0V
I_{OL}	Output Low Current			4	mA	
I_{CC}	Power Supply Current		35		mA	
C_{IN}	Input Capacitance			7	pF	
C_{OUT}	Output Capacitance			34	pF	
V_T(1)	Input Threshold Voltage		1.3		V	
V_T(2)	Input Threshold Voltage		V_{CC}/2		V	

NOTES:
1. Specified for all input pins except MD31–MD0, VWE#, BE#3–BE#0.
2. Specified for MD31–MD0, VWE#, BE#–BE#0.

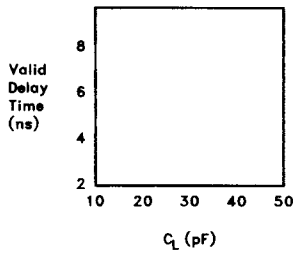
Table 5-4. CLK DC Characteristics V_{CC} = 5V, T_{CASE} = 25°C

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IL}	Input LOW Voltage			0.9	V	V_{CC} = 4.5V
V_{IH}	Input HIGH Voltage	3.85			V	V_{CC} = 5.5V
I_{IL}	Input LOW Leakage			±1	μA	V_{IH} = V_{CC}
I_{IH}	Input HIGH Leakage			±1	μA	V_{IL} = 0V
V_T	Input Threshold Voltage		2.5		V	
C_{IN}	Input Capacitance			7	pF	

1

Output Delay and Rise Time vs Load Capacitance

Typical Output Valid Delay vs Load Capacitance



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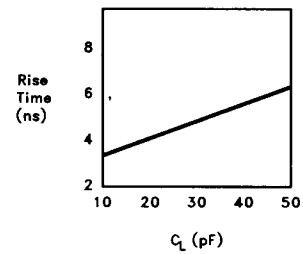
Typical Output Rise Time vs Load Capacitance



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5.2 AC Characteristics

NOTE:
Industry standard gate array test methodologies do not include full AC characterization. The AC characteristics below were determined through simulation and are provided as design guidelines only. These parameters are not fully tested in production. As per TI's standard gate array test methodology, two AC parametric measurements are made during production to guarantee the speed of the device. These measurements are indicated by an * in the table below.

Table 5-5. AC Characteristics V_{CC} = 5V ±10%, T_A = 0°C to +70°C, C_L = 45 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t1	VA19–VA0 Setup before DSTRB# Low	10		ns	5-1	
t2	VA19–VA0 Hold after DSTRB# Low	2		ns	5-1	
t3	BE#3–BE#0 Setup before DSTRB# Low	0		ns	5-1	
t4	BE#3–BE#0 Hold after DSTRB# Low	10		ns	5-1	
t5	DSTRB# Low Pulse Width	20		ns	5-1	
t6	VWE# Setup before DSTRB# Low	7		ns	5-1	
t7	VWE# Hold after DSTRB# Low	5		ns	5-1	
t8	MD31–MD0 Write Data Valid before VWE# High	5		ns	5-1	
t9	MD31–MD0 Write Data Valid after VWE# High	20		ns	5-1	
t10	DSTRB# Low to MD31–MD0 Read Data Enabled	5		ns	5-1	2
t11	DSTRB# Low to MD31–MD0 Read Data Valid		50	ns	5-1	2
t12	DSTRB# High to MD31–MD0 Read Data Invalid	4		ns	5-1	2
t13	DSTRB# High to MD31–MD0 Read Data Disabled		20	ns	5-1	2

NOTES:
1. All timing measured at the 1.3V TTL threshold.
2. For MD31–MD0 lines, C_L = 100 pF.

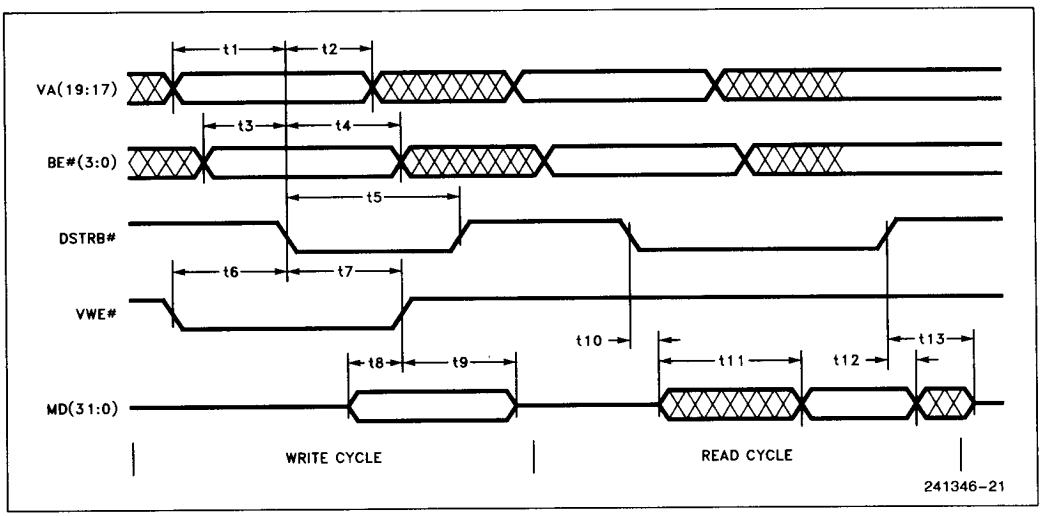


Figure 5-1. DVI Device Read and Write Cycle

Table 5-6. AC Characteristics V_{CC} = 5V ±10%, T_A = 0°C to +70°C, C_L = 45 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t14	DMS#, DRD#, and DWR# Low to AREQ# Low		42	ns	5-2	
t15	AREQ# Low to DMARDY# Low		6	ns	5-2	
t16	ASEL# Low to AREQ# High		32	ns	5-2	
t17	BUSEN# Low to AREQ# High		31	ns	5-2	
t18	BUSEN High to DMARDY# High		36	ns	5-2	
t19	ASEL# High to DMARDY# High		37	ns	5-2	
t20	ASEL# High to VWE# Disabled		28	ns	5-2	
t21	ASEL# Low to VWE# Enabled and Valid		28	ns	5-2	
t22	BUSEN# Low to VWE# Enabled and Valid		27	ns	5-2	
t23	BUSEN# High to VWE# Disabled		27	ns	5-2	
t24	MSTRB# Setup to V1CLK	10		ns	5-2	
t25	GAVALEN Setup to V1CLK	8		ns	5-2	
t26	ASEL# Low to MD31–MD0 Address Enabled and Valid		46	ns	5-2	2
t27	BUSEN# Low to MD31–MD0 Address Enabled and Valid		27	ns	5-2	2
t28	V1CLK High to MD31–MD0 Address Disabled		50	ns	5-2	
t29	WRITE: V1CLK High to MD31–MD0 Data Enabled and Valid		50	ns	5-2	2
t30	WRITE: V1CLK to MD31–MD0 Data Disabled		30	ns	5-2	2
t31	WRITE: ASEL# High to MD31–MD0 Data Disabled	3	43	ns	5-2	
t32	READ: MD31–MD0 Setup to V1CLK	10		ns	5-2	
t33	READ: MD31–MD0 Hold after V1CLK	10		ns	5-2	

NOTES:
1. All timing measured at the 1.3V TTL threshold.
2. For MD31–MD0 lines, C_L = 100 pF.

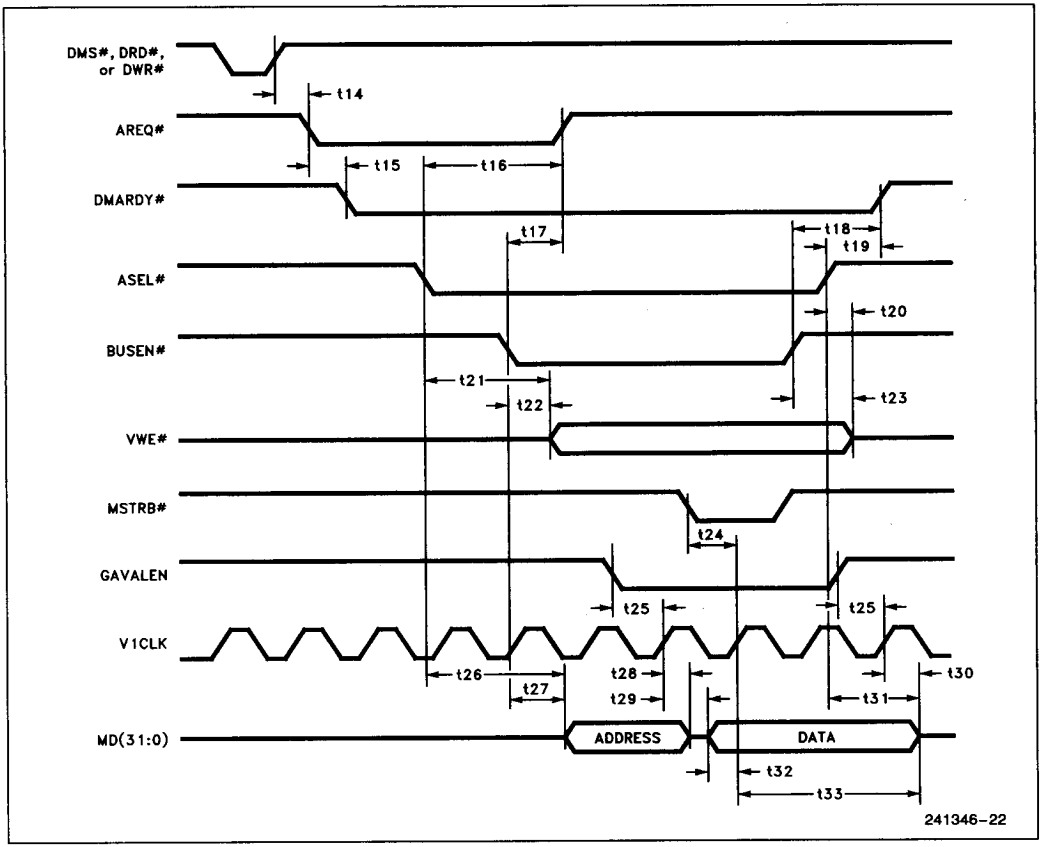


Figure 5-2. DVI DMA Transfer

Table 5-7. AC Characteristics V_{CC} = 5V ±10%, T_A = 0°C to +70°C, C_L = 45 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t34	A(3:0) Delay before TD15–TD0 Read Data Valid		48	ns	5-3	
t35	A(3:0) Delay before TD15–TD0 Read Data Invalid	3		ns	5-3	
t36	DRD# High to TD15–TD0 Read Data Invalid	3		ns	5-3	
t37	DMS# High to TD15–TD0 Read Data Invalid	3		ns	5-3	
t38	DMS# Low to TD15–TD0 Read Data Valid		57	ns	5-3	
t39	DMS# Low to TD15–TD0 Read Data Enabled	3		ns	5-3	
t40*	DRD# Low to TD15–TD0 Read Data Valid		57	ns	5-3	
t41	DMS# High to TD15–TD0 Read Data Disabled	3		ns	5-3	
t42	DRD# Low to TD15–TD0 Read Data Enabled	3		ns	5-3	
t43	DRD# High to TD15–TD0 Read Data Disabled	3		ns	5-3	
t44	A3–A0 Setup before DWR# Low	0		ns	5-3	
t45	A3–A0 Hold after DWR# High	5		ns	5-3	
t46	A3–A0 Hold after DMS# High	5		ns	5-3	
t47	A3–A0 Setup before DMS# Low	0		ns	5-3	
t48	TD15–TD0 Write Data Setup before DMS# High	5		ns	5-3	
t49	TD15–TD0 Write Data Hold after DMS# High	15		ns	5-3	
t50	TD15–TD0 Write Data Setup before DWR# High	5		ns	5-3	
t51	TD15–TD0 Write Data Hold after DWR# High	15		ns	5-3	
t52	DRD# Low to DBR# Low	5	32	ns	5-4	
t53	DSTRB# Low to DBR# High	5	28	ns	5-4	
t54	DIN Setup before SCLOCK High	0		ns	5-5	
t55	DIN Hold after SCLOCK High	9		ns	5-5	
t56	CAPL__R Setup before SCLOCK High	5		ns	5-5	
t57	CAPL__R High to CINT# Low		16	ns	5-5	
t58	BCLK Low to WCLK Delay		4	ns	5-6	
t59	BCLK Low to DOUT Delay		13	ns	5-6	
t60	BCLK Low to PLAYL__R Delay		3	ns	5-6	

NOTE:
1. All timing measured at the 1.3V TTL threshold.

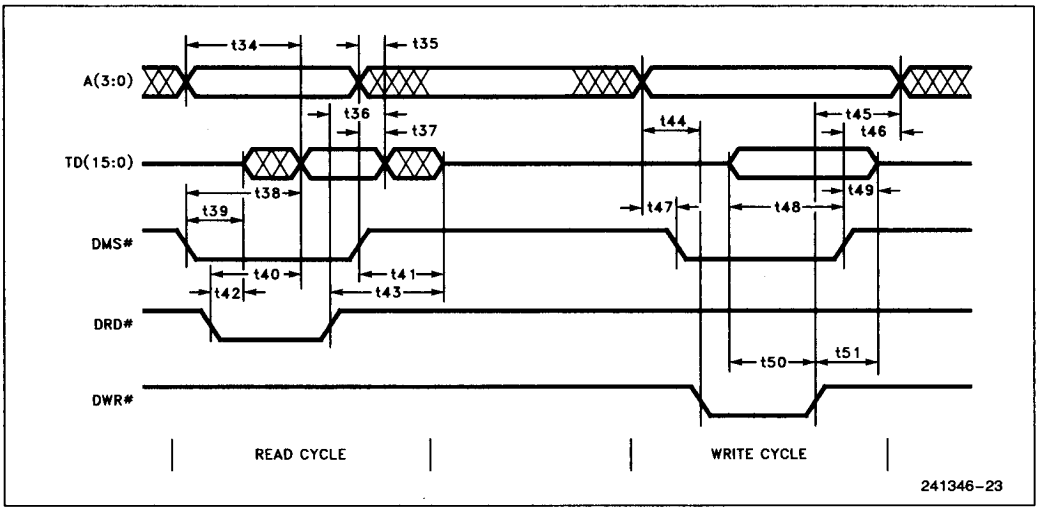


Figure 5-3. ADSP External Memory Read and Write Cycle

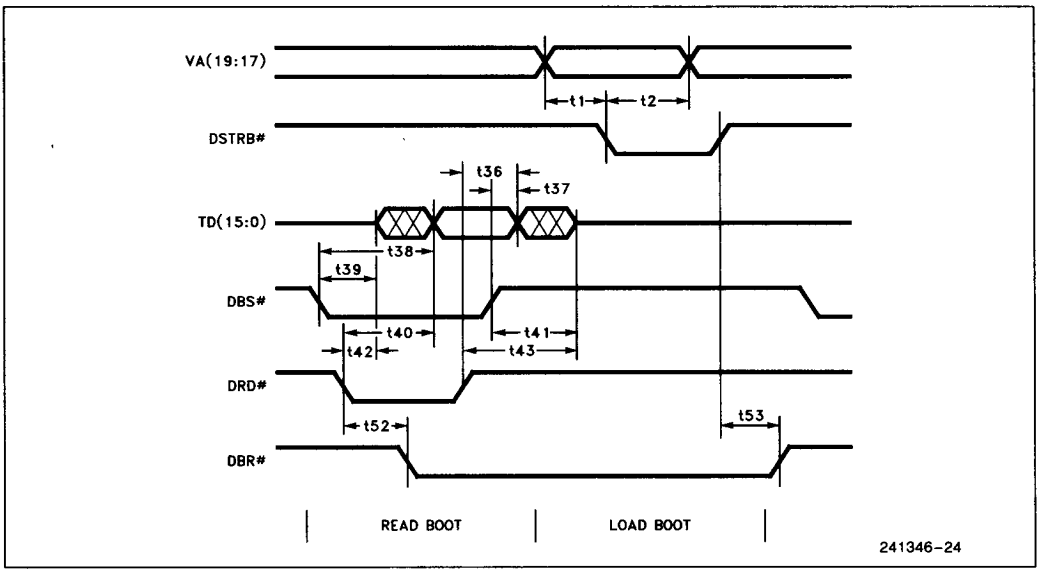


Figure 5-4. ADSP Boot Cycle

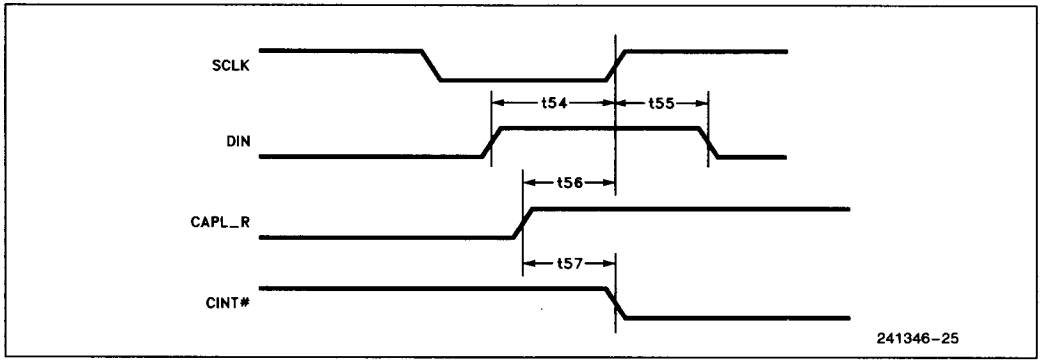


Figure 5-5. ADSP Capture Waveforms

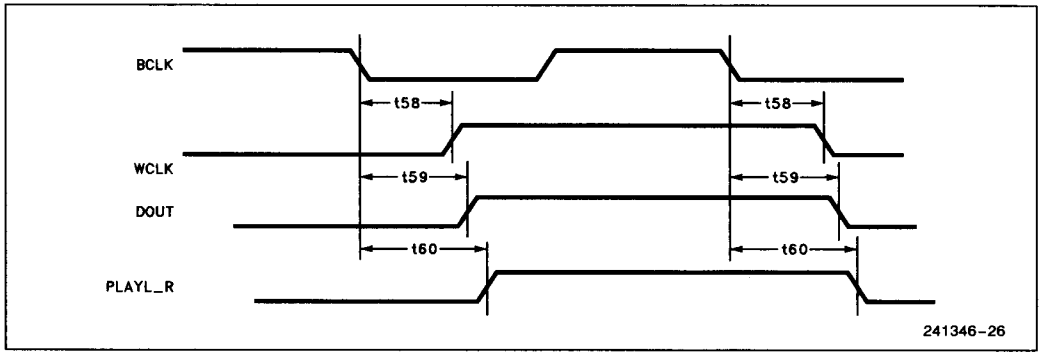


Figure 5-6. ADSP Playback Waveforms

Table 5-8. AC Characteristics V_{CC} = 5V ±10%, T_A = 0°C to +70°C, C_L = 45 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t61	RGB__HSYNC to HSYNC Delay		23	ns	5-7	
t61	DB__HSYNC to HSYNC Delay		23	ns	5-7	
t61	VGA__HSYNC to HSYNC Delay		23	ns	5-7	
t61	DB__CSYNC to HSYNC Delay		23	ns	5-7	
t61	RGB__VSYNC to VSYNC Delay		22	ns	5-7	
t61	DB__VSYNC to VSYNC Delay		22	ns	5-7	
t61	VGA__VSYNC to VSYNC Delay		22	ns	5-7	
t62	VCO__IN to PB__CLK, DB__CLK Delay		20	ns	5-8	
t62	DOT__CLK to PB__CLK, DB__CLK Delay		20	ns	5-8	
t62*	SYS__CLK to PB__CLK, DB__CLK Delay		20	ns	5-8	
t62	10MHZ__IN to PB__CLK, DB__CLK Delay		20	ns	5-8	
t62	XI to PB__CLK, DB__CLK Delay		20	ns	5-8	
t62	VCO__IN ÷ 2 to PB__CLK, DB__CLK Delay		26	ns	5-8	
t63	VFB7-VFB0 Setup before DOT__CLK	5		ns	5-9	
t63	DB__KEY Setup before DOT__CLK	6		ns	5-9	
t64	VFB7-VFB0 Hold after DOT__CLK	3		ns	5-9	
t64	DB__KEY Hold after DOT__CLK	3		ns	5-9	
t65	DOT__CLK to DVI, VGA Delay		8	ns	5-9	
t65	DB__CLK to DB__VRST Delay		25	ns	5-9	
t65	VCO__IN to DB__HRST Delay		29	ns	5-9	

NOTE:
1. All timing measured at the 1.3V TTL threshold.

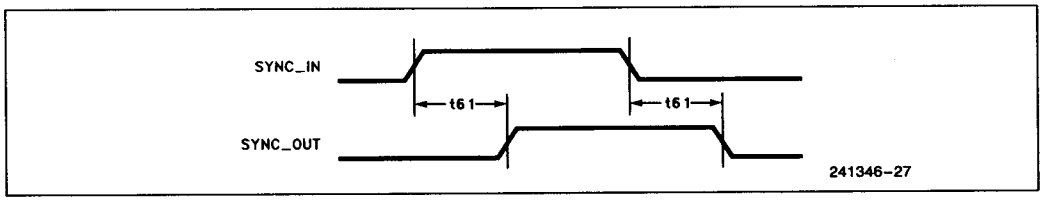


Figure 5-7. Sync Delays

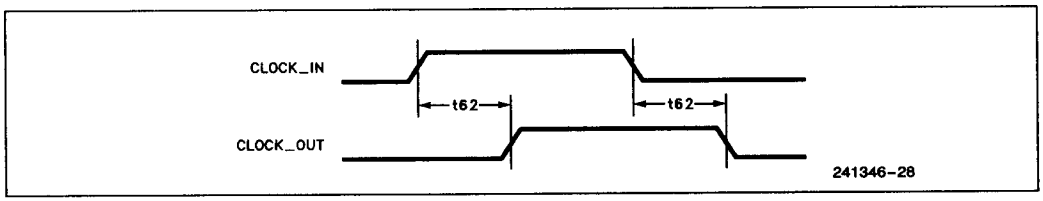


Figure 5-8. Clock Delays

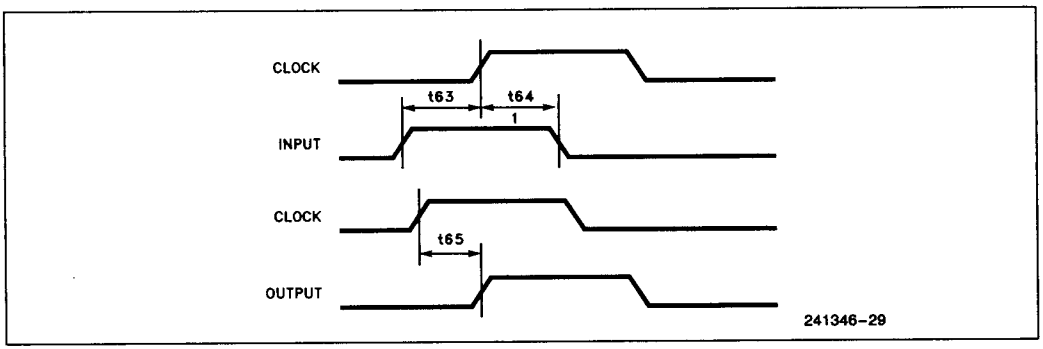
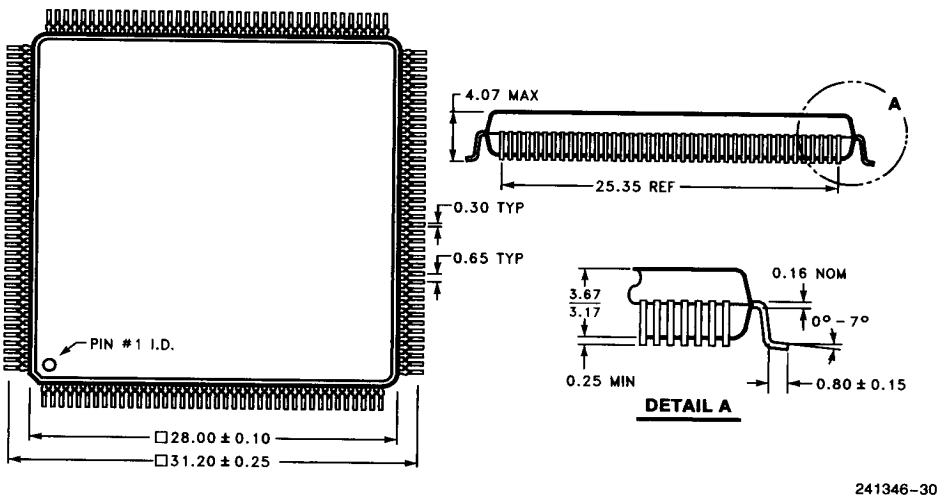


Figure 5-9. Miscellaneous Timing



NOTES:
1. All dimensions in millimeters.
2. Co-planarity within 0.10 mm.

6.0 PACKAGE THERMAL SPECIFICATIONS

Thermal impedance is defined as the ability to dissipate heat generated by an electronic device and is characterized by θ_{JA} and θ_{JC}. It is measured in degrees Celsius per Watt. θ_{JA} is the thermal impedance from the IC chip junction in still air ambient with the package mounted in a socket or directly mounted on a PC Board. θ_{JC} is the thermal impedance from the IC junction to the external package case. Measurements are typically taken using high air flow to simulate an infinite heat sink. The thermal characteristics of the 160-lead PQFP package are as follows:

$$\theta_{JA} = 60.0°C/W$$
$$\theta_{JC} = 18.0°C/W$$