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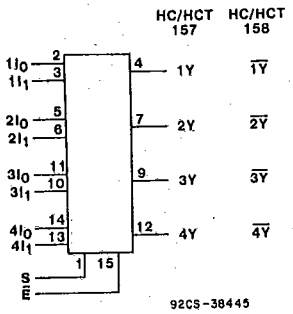
CD54/74HC157, CD54/74HCT157
CD54/74HC158, CD54/74HCT158

File Number **1642**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad 2-Input Multiplexers

HC/HCT157 Non-Inverting
HC/HCT158 Inverting

Type Features:

- *Buffered inputs*
- *Typical Propagation Delay (In to Output) = 10 ns (HC157) @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC157, 158 and CD54/74HCT157, 158 are quad 2-input multiplexers which select four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active LOW. When ($\overline{E}$) is HIGH, all of the outputs in the 158, the inverting type, (1Y-4Y) are forced HIGH and in the 157, the non-inverting type, all of the outputs ($\overline{1Y}$-$\overline{4Y}$) are forced LOW, regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of these devices. The state of the Select input determines the particular register from which the data comes. They can also be used as function generators.

The CD54HC157, 158 and CD54HCT157, 158 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC157, 158 and CD74HCT157, 158 are supplied in 16-lead dual-in-line plastic packages (E suffix). The CD74HC157, 158 and CD74HCT157, 158 are supplied in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

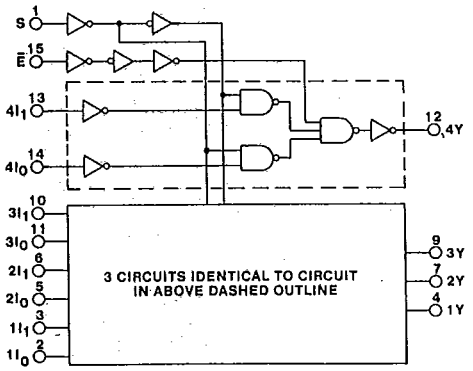


Fig. 1 - Logic Diagram for HC/HCT157.

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

FUNCTION TABLE

Enable	Select Input	Data Inputs		Output	
				157	158
$\overline{E}$	S	I_0	I_1	Y	$\overline{Y}$
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

L = LOW voltage level.
H = HIGH voltage level.
X = Don't care.

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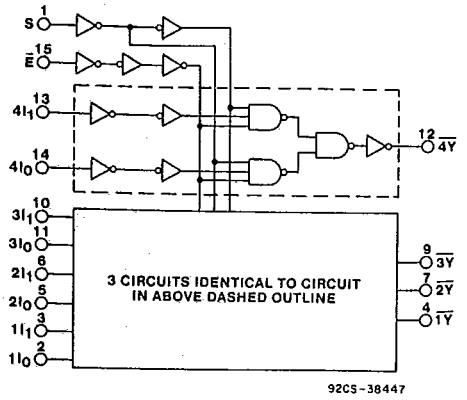
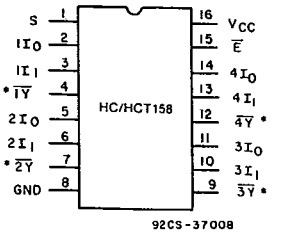


Fig. 2 - Logic Diagram for HC/HCT158.



* For HC/HCT157 these outputs are 1Y, 2Y, 3Y, 4Y.

TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} +0.5$ V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}): ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 In. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{in}, V_{out}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC157/158/CD54HC157/158										CD74HCT157/158/CD54HCT157/158									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage CMOS Loads V_{OH}	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage CMOS Loads V_{OL}	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

INPUT LOADING TABLE

INPUT	UNIT LOADS *	
	HCT 157	HCT 158
I (ALL)	0.95	0.4
$\overline{E}$	0.6	0.6
S	3	2.8

* Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L pF	SYMBOL	TYPICAL VALUES				UNITS
			HC157	HCT157	HC158	HCT158	
Data to Output	15	t_{PHL} t_{PLH}	10	12	11	13	ns
Enable to Output	15	t_{PHL} t_{PLH}	11	12	13	15	ns
Select to Output	15	t_{PHL} t_{PLH}	12	15	12	14	ns
Power Dissipation Capacitance*		C_{PD}	62	70	35	35	pF

* C_{PD} is used to determine the dynamic power consumption, per multiplexer.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where: f_i = input frequency. f_o = output frequency. C_L = output load capacitance. V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	125	—	—	—	155	—	—	—	190	—	—	
Data to Output	t_{PHL}	4.5	—	25	—	30	—	31	—	38	—	38	—	45	ns
(Figure 3) HC/HCT157		6	—	21	—	—	—	26	—	—	—	32	—	—	
Propagation Delay	t_{PLH}	2	—	135	—	—	—	170	—	—	—	205	—	—	
Enable to Output	t_{PHL}	4.5	—	27	—	30	—	34	—	38	—	41	—	45	ns
(Figure 4) HC/HCT157		6	—	23	—	—	—	29	—	—	—	35	—	—	
Propagation Delay	t_{PLH}	2	—	145	—	—	—	180	—	—	—	220	—	—	
Select to Output	t_{PHL}	4.5	—	29	—	37	—	36	—	46	—	44	—	56	ns
(Figure 3) HC/HCT157		6	—	25	—	—	—	31	—	—	—	38	—	—	
Propagation Delay	t_{PLH}	2	—	140	—	—	—	175	—	—	—	210	—	—	
Data to Output	t_{PHL}	4.5	—	28	—	32	—	35	—	40	—	42	—	48	ns
(Figure 3) HC/HCT158		6	—	24	—	—	—	30	—	—	—	36	—	—	
Propagation Delay	t_{PLH}	2	—	160	—	—	—	200	—	—	—	240	—	—	
Enable to Output	t_{PHL}	4.5	—	32	—	37	—	40	—	46	—	48	—	56	ns
(Figure 4) HC/HCT158		6	—	27	—	—	—	34	—	—	—	41	—	—	
Propagation Delay	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Select to Output	t_{PHL}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
(Figure 3) HC/HCT158		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
(Figure 3 or 4)		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_{in}		—	10	—	10	—	10	—	10	—	10	—	10	pF

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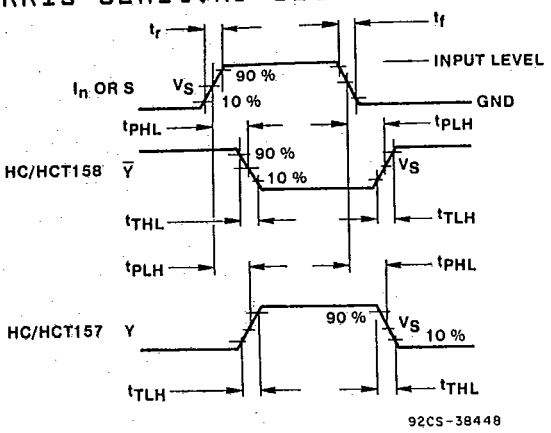

Fig. 3 - Inputs or select to output propagation delays and output transition times.

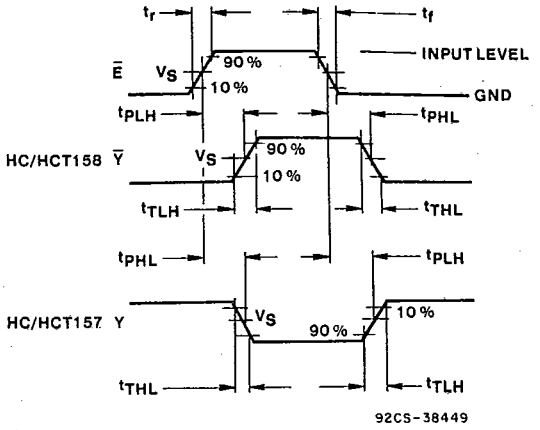

Fig. 4 - Enable to output propagation delays and output transition times.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V