National Semiconductor

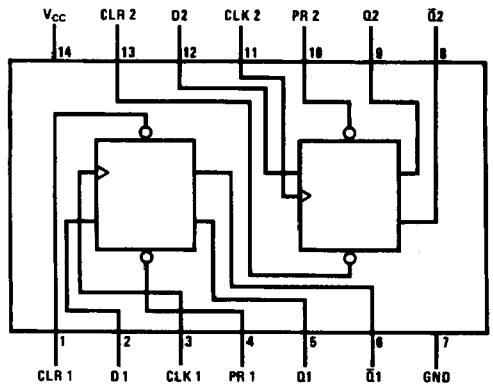
DM54L74 Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6631–1

Order Number DM54L74J or DM54L74W
See NS Package Number J14A or W14B

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_O	$\overline{Q}_O$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↑ = Positive-going transition.

Q_O = The output logic level of Q before the indicated input conditions were established.

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs returned to their inactive (high) level.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54L74			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.7	V
I_{OH}	High Level Output Current				−0.2	mA
I_{OL}	Low Level Output Current				2	mA
f_{CLK}	Clock Frequency (Note 2)		0		6	MHz
t_W	Pulse Width (Note 2)	Clock High	75			ns
		Clock Low	75			
		Preset Low	75			
		Clear Low	75			
t_{SU}	Input Setup Time (Notes 1 & 2)		50 ↑			ns
t_H	Input Hold Time (Notes 1 & 2)		15 ↑			ns
T_A	Free Air Operating Temperature		−55		125	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.15	0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 5.5V	D			100	μA
			Clear			300	
			Preset			200	
			Clock			200	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	D			10	μA
			Clear			30	
			Preset			20	
			Clock			20	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	D			−0.18	mA
			Clear			−0.36	
			Preset			−0.18	
			Clock			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max		−3		−15	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			1.6	3	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 4 kΩ, C_L = 50 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		6		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		120	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		120	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$	10	90	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$	10	120	ns