

Octal D-Type Latch with 3-State Outputs With 5V-Tolerant Inputs

The MC74LVX573 is an advanced high speed CMOS octal latch with 3-state outputs. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

This 8-bit D-type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

- High Speed: $t_{PD} = 6.4ns$ (Typ) at $V_{CC} = 3.3V$
- Low Power Dissipation: $I_{CC} = 4\mu A$ (Max) at $T_A = 25^\circ C$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP} = 0.8V$ (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

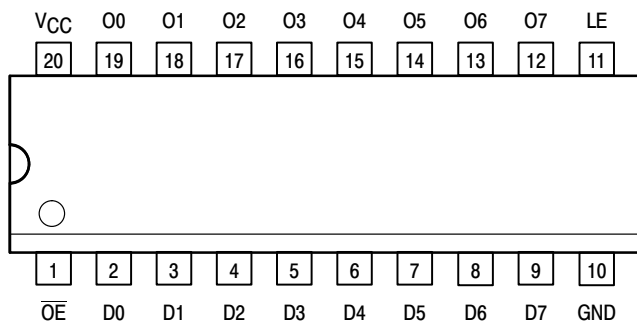
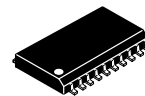


Figure 1. 20-Lead Pinout (Top View)

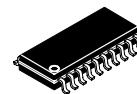
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DW SUFFIX
20-LEAD SOIC PACKAGE
CASE 751D-04



DT SUFFIX
20-LEAD TSSOP PACKAGE
CASE 948E-02



M SUFFIX
20-LEAD SOIC EIAJ PACKAGE
CASE 967-01

PIN NAMES

Pins	Function
\overline{OE}	Output Enable Input
LE	Latch Enable Input
D0-D7	Data Inputs
O0-O7	3-State Latch Outputs

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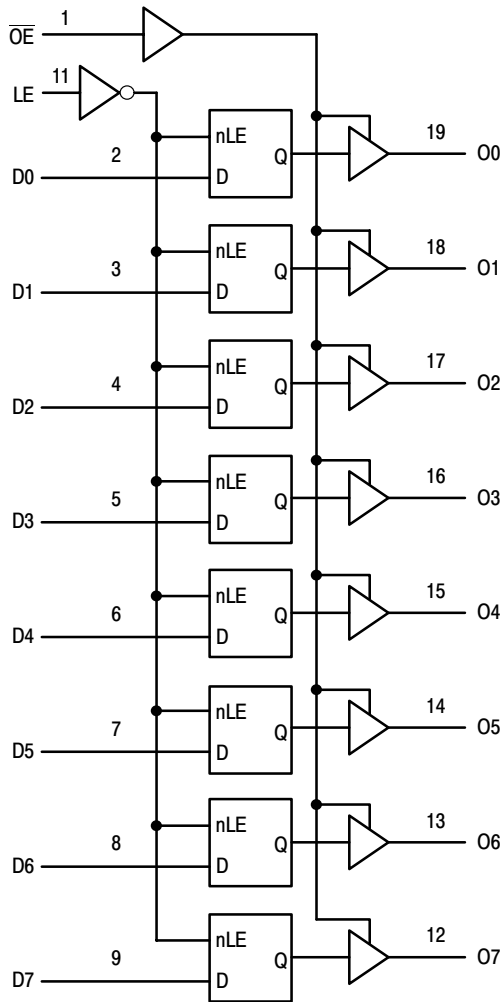


Figure 2. Logic Diagram

INPUTS			OUTPUTS	OPERATING MODE
\overline{OE}	LE	Dn	On	
L	H	H	H	Transparent (Latch Disabled); Read Latch
L	H	L	L	
L	L	h	H	Latched (Latch Enabled) Read Latch
L	L	l	L	
L	L	X	NC	Hold; Read Latch
H	L	X	Z	Hold; Disabled Outputs
H	H	H	Z	Transparent (Latch Disabled); Disabled Outputs
H	H	L	Z	
H	L	h	Z	Latched (Latch Enabled); Disabled Outputs
H	L	l	Z	

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition; NC = No Change, State Prior to the Latch Enable High-to-Low Transition; X = High or Low Voltage Level or Transitions are Acceptable; Z = High Impedance State; For I_{CC} Reasons DO NOT FLOAT Inputs

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{in}	DC Input Voltage	-0.5 to +7.0	V
V _{out}	DC Output Voltage	-0.5 to V _{CC} +0.5	V
I _{IK}	Input Diode Current	-20	mA
I _{OK}	Output Diode Current	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation	180	mW
T _{stg}	Storage Temperature	-65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	3.6	V
V _{in}	DC Input Voltage	0	5.5	V
V _{out}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-40	+85	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A = -40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.0	1.5			1.5		V
			3.0	2.0			2.0		
			3.6	2.4			2.4		
V _{IL}	Low-Level Input Voltage		2.0			0.5		0.5	V
			3.0			0.8		0.8	
			3.6			0.8		0.8	
V _{OH}	High-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	I _{OH} = -50μA I _{OH} = -50μA I _{OH} = -4mA	2.0	1.9	2.0		1.9		V
			3.0	2.9	3.0		2.9		
			3.0	2.58			2.48		
V _{OL}	Low-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	I _{OL} = 50μA I _{OL} = 50μA I _{OL} = 4mA	2.0		0.0	0.1		0.1	V
			3.0		0.0	0.1		0.1	
			3.0			0.36		0.44	
I _{in}	Input Leakage Current	V _{in} = 5.5V or GND	3.6			±0.1		±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	3.6			±0.25		±2.5	μA
I _{CC}	Quiescent Supply Current	V _{in} = V _{CC} or GND	3.6			4.0		40.0	μA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
t_{PLH} , t_{PHL}	Propagation Delay LE to O	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$		8.2	15.6	1.0	18.5	ns
		$C_L = 50\text{pF}$		10.7	19.1	1.0	22.0	
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$		6.4	10.1	1.0	12.0	
		$C_L = 50\text{pF}$		8.9	13.6	1.0	15.5	
t_{PLH} , t_{PHL}	Propagation Delay D to O	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$		7.6	14.5	1.0	17.5	ns
		$C_L = 50\text{pF}$		10.1	18.0	1.0	21.0	
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$		5.9	9.3	1.0	11.0	
		$C_L = 50\text{pF}$		8.4	12.8	1.0	14.5	
t_{PZL} , t_{PZH}	Output Enable Time $\overline{\text{OE}}$ to O	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$		7.8	15.0	1.0	18.5	ns
		$R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		10.3	18.5	1.0	22.0	
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$		6.1	9.7	1.0	12.0	
		$R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		8.6	13.2	1.0	15.5	
t_{PLZ} , t_{PHZ}	Output Disable Time $\overline{\text{OE}}$ to O	$V_{CC} = 2.7\text{V}$ $C_L = 50\text{pF}$		12.1	19.1	1.0	22.0	ns
		$R_L = 1\text{k}\Omega$						
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$		10.1	13.6	1.0	15.5	
t_{OSHL} , t_{OSLH}	Output-to-Output Skew (Note 1.)	$V_{CC} = 2.7\text{V}$ $C_L = 50\text{pF}$			1.5		1.5	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
		Min	Typ	Max	Min	Max	
C_{in}	Input Capacitance		4	10		10	pF
C_{out}	Maximum Three-State Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		29				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/8$ (per latch). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$, $C_L = 50\text{pF}$, $V_{CC} = 3.3\text{V}$, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.5	-0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

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TIMING REQUIREMENTS (Input $t_r = t_f = 3.0\text{ns}$)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40$ to 85°C	Unit
			Typ	Limit	Limit	
$t_{w(h)}$	Minimum Pulse Width, LE	$V_{CC} = 2.7\text{V}$ $V_{CC} = 3.3 \pm 0.3\text{V}$		6.5 5.0	7.5 5.0	ns
t_{su}	Minimum Setup Time, D to LE	$V_{CC} = 2.7\text{V}$ $V_{CC} = 3.3 \pm 0.3\text{V}$		5.0 3.5	5.0 3.5	ns
t_h	Minimum Hold Time, D to LE	$V_{CC} = 2.7\text{V}$ $V_{CC} = 3.3 \pm 0.3\text{V}$		1.5 1.5	1.5 1.5	ns

SWITCHING WAVEFORMS

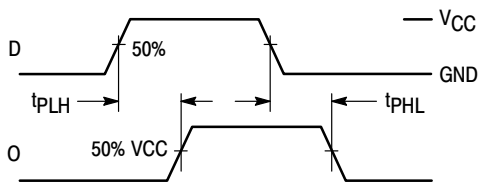


Figure 3.

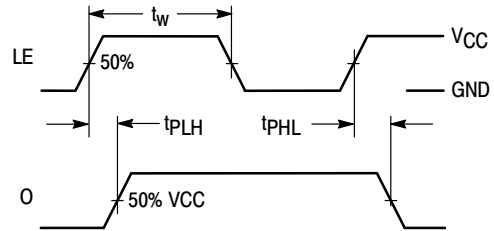


Figure 4.

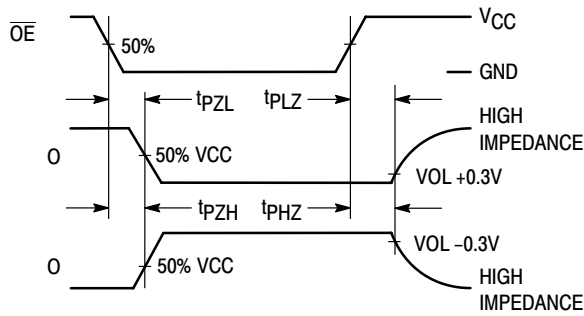


Figure 5.

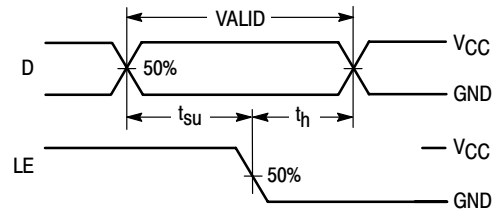
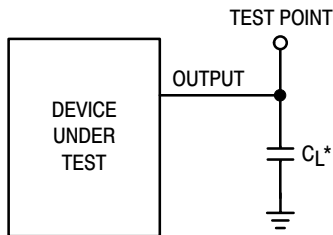


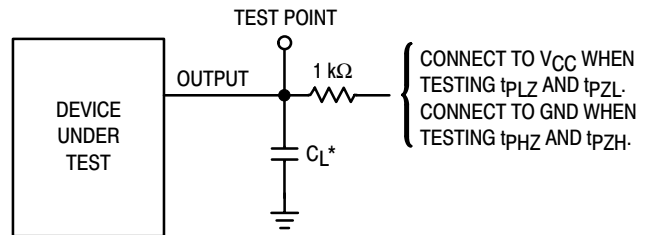
Figure 6.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 7. Propagation Delay Test Circuit



*Includes all probe and jig capacitance

Figure 8. Three-State Test Circuit