

## CMOS Ripple-Carry Binary Counter/Dividers

High-Voltage Types (20-Volt Rating)

CD4020B — 14 Stage

CD4024B — 7 Stage

CD4040B — 12 Stage

■ CD4020B, CD4024B, and CD4040B are ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros state. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times. All inputs and outputs are buffered.

The CD4020B and CD4040B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD4024B types are supplied in 14 lead hermetic dual-in-line ceramic package (D or F suffix), 14 lead dual-in-line plastic package (E suffix), 14 lead small-outline plastic package (M suffix) and in chip form (H suffix).

### MAXIMUM RATINGS, Absolute-Maximum Values:

#### DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal) ..... -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to  $V_{DD}$  +0.5V

DC INPUT CURRENT, ANY ONE INPUT .....  $\pm 10\text{mA}$

#### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  ..... 500mW

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  ..... Derate Linearly at 12mW/°C to 200mW

#### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR  $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$  ..... 100mW

OPERATING-TEMPERATURE RANGE ( $T_A$ ) .....  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE ( $T_{STG}$ ) .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

#### LEAD TEMPERATURE (DURING SOLDERING):

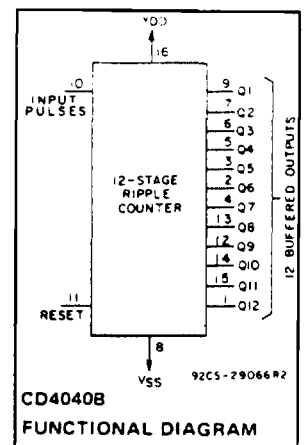
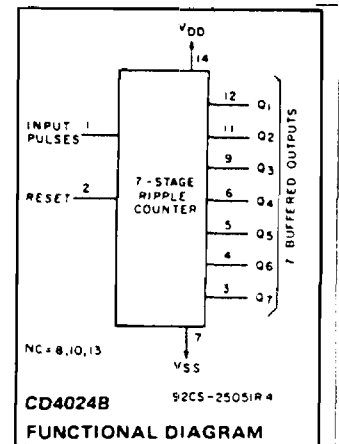
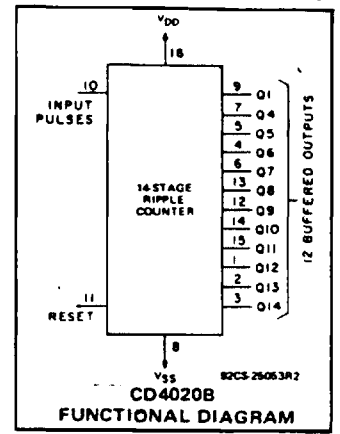
At distance 1/16  $\pm$  1/32 inch (1.59  $\pm$  0.79mm) from case for 10s max .....  $+265^\circ\text{C}$

### Features:

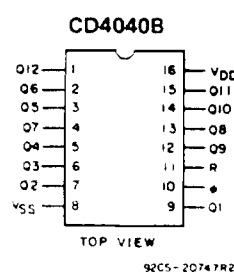
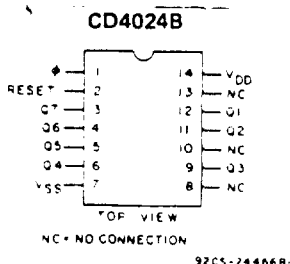
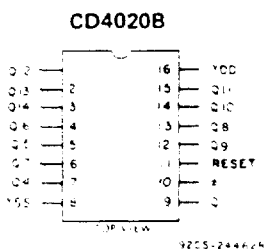
- Medium-speed operation
- Fully static operation
- Buffered inputs and outputs
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- Fully static operation
- Common reset
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1  $\mu\text{A}$  at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  - 1 V at  $V_{DD} = 5\text{ V}$
  - 2 V at  $V_{DD} = 10\text{ V}$
  - 2.5 V at  $V_{DD} = 15\text{ V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

- Control counters
- Frequency dividers
- Timers
- Time-delay circuits



### TERMINAL ASSIGNMENTS



\*HR15503\*

# CD4020B, CD4024B, CD4040B Types

**RECOMMENDED OPERATING CONDITIONS** at  $T_A = 25^\circ\text{C}$ . Unless Otherwise Specified  
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	$V_{DD}$	Min.	Max.	UNITS
Supply Voltage Range (at $T_A = \text{Full Package Temperature Range}$ )		3	18	V
Input-Pulse Frequency, $f_\phi$	5 10 15	—	3.5 8 12	MHz
Input-Pulse Width, $t_W$	5 10 15	140 60 40	— — —	ns
Input-Pulse Rise or Fall Time, $t_{r\phi}, t_{f\phi}$	5 10 15	Unlimited		$\mu\text{s}$
Reset Pulse Width, $t_W$	5 10 15	200 80 60	—	ns
Reset Removal Time, $t_{REM}$	5 10 15	350 150 100	—	ns

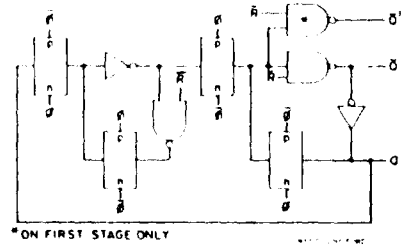


Fig. 4 - Detail of typical flip-flop stage.

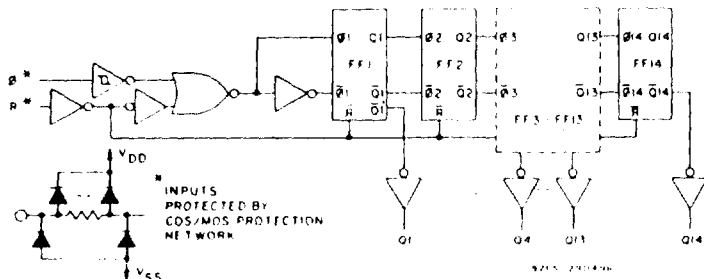


Fig. 1 - Logic diagram for CD4020B.

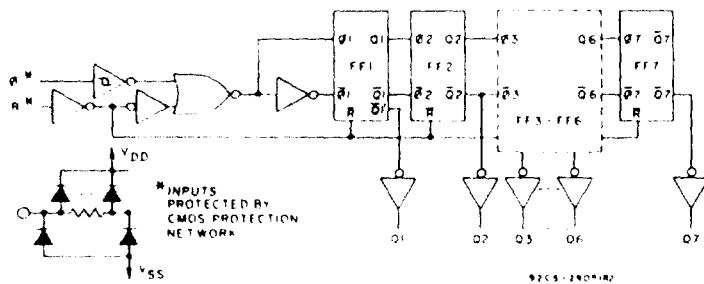


Fig. 2 - Logic diagram for CD4024B

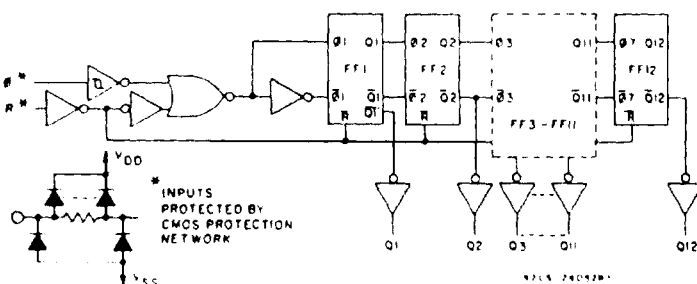


Fig. 3 - Logic diagram for CD4040B

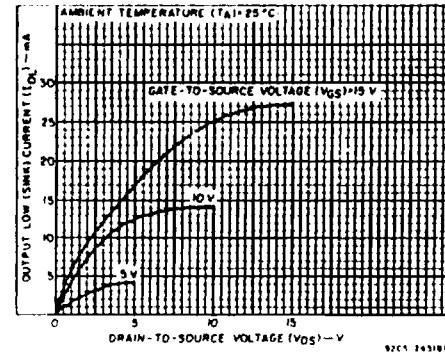


Fig. 5 - Typical output low (sink) current characteristics.

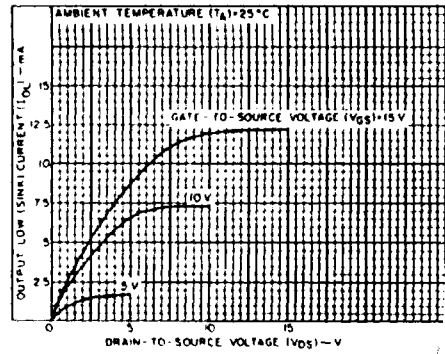


Fig. 6 - Minimum output low (sink) current characteristics.

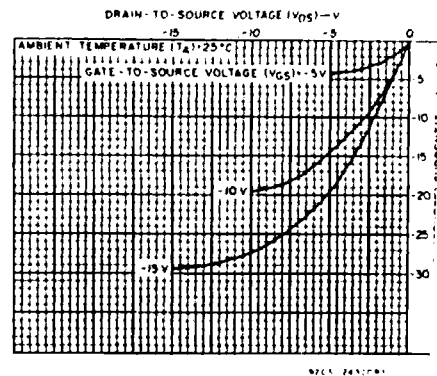


Fig. 7 - Typical output high (source) current characteristics.

# CD4020B, CD4024B, CD4040B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	+25							
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max	-	0,5	5	5	5	150	150	-	0,04	5	μA
	-	0,10	10	10	10	300	300	-	0,04	10	
	-	0,15	15	20	20	600	600	-	0,04	20	
	-	0,20	20	100	100	3000	3000	-	0,08	100	
Output Low (Sink) Current I <sub>OL</sub> Min	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-	
Output High (Source) Current, I <sub>OH</sub> Min	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-	
Output Voltage Low Level, V <sub>OL</sub> Max	-	0,5	5	0,05				-	0	0,05	V
	-	0,10	10	0,05				-	0	0,05	
	-	0,15	15	0,05				-	0	0,05	
Output Voltage High Level, V <sub>OH</sub> Min	-	0,5	5	4,95				4,95	5	-	V
	-	0,10	10	9,95				9,95	10	-	
	-	0,15	15	14,95				14,95	15	-	
Input Low Voltage, V <sub>IL</sub> Max	0,5, 4,5	-	5	1,5				-	-	1,5	V
	1,9	-	10	3				-	-	3	
	1,5, 13,5	-	15	4				-	-	4	
Input High Voltage, V <sub>IH</sub> Min	0,5, 4,5	-	5	3,5				3,5	-	-	V
	1,9	-	10	7				7	-	-	
	1,5, 13,5	-	15	11				11	-	-	
Input Current I <sub>IN</sub> Max		0,18	18	±0,1	±0,1	±1	±1	-	±10 <sup>-5</sup>	±0,1	μA

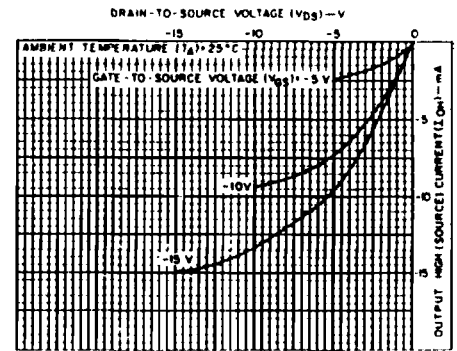


Fig. 8 - Minimum output high (source) current characteristics.

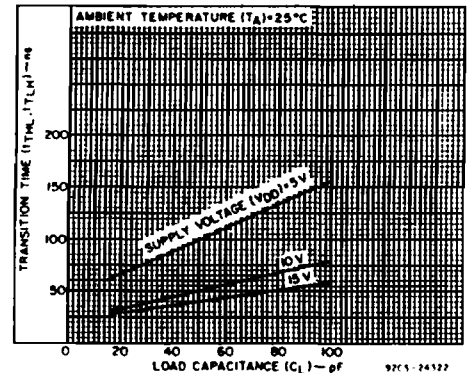
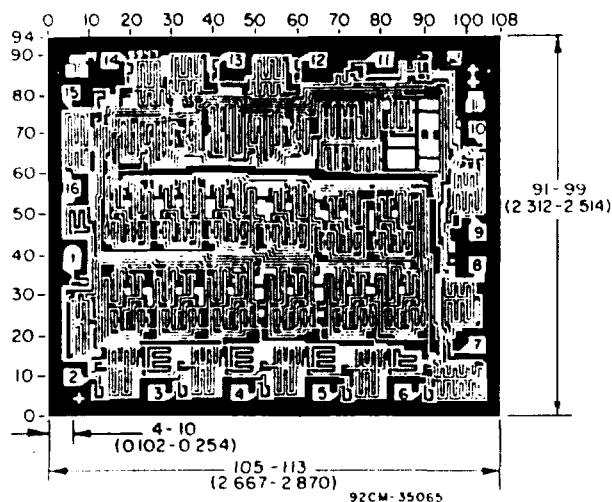
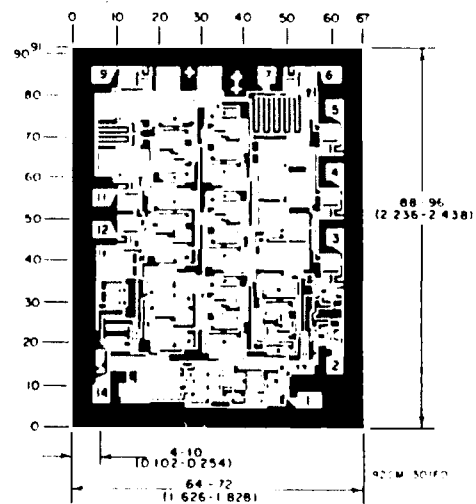


Fig. 9 - Typical transition time as a function of load capacitance.



Dimensions and Pad Layout for CD4020BH. Dimensions and pad layout for CD4040BH are identical.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10<sup>-3</sup> inch).



Dimensions and Pad Layout for CD4024BH.

# CD4020B, CD4024B, CD4040B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20\text{ ns}$ ,  
 $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	$V_{DD}$ (V)	LIMITS			UNITS
			Min.	Typ.	Max.	
<b>Input-Pulse Operation</b>						
Propagation Delay Time, $\phi$ to $Q_1$ Out: $t_{PHL}, t_{PLH}$		5	—	180	360	ns
		10	—	80	160	
		15	—	65	130	
$Q_n$ to $Q_{n+1}$ : $t_{PHL}, t_{PLH}$		5	—	100	330	ns
		10	—	40	80	
		15	—	30	60	
Transition Time, $t_{THL}, t_{TLH}$		5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Minimum Input-Pulse Width, $t_W$		5	—	70	140	ns
		10	—	30	60	
		15	—	20	40	
Input-Pulse Rise or Fall Time, $t_r, t_f$		5	Unlimited			$\mu\text{s}$
		10				
		15				
Maximum Input-Pulse Frequency, $f_\phi$		5	3.5	7	—	MHz
		10	8	16	—	
		15	12	24	—	
Input Capacitance, $C_i$	Any Input		—	5	7.5	pF
<b>Reset Operation</b>						
Propagation Delay Time, $t_{PHL}$		5	—	140	280	ns
		10	—	60	120	
		15	—	50	100	
Minimum Reset Pulse Width, $t_W$		5	—	100	200	ns
		10	—	40	80	
		15	—	30	60	
Reset Removal Time, $t_{REM}$		5	—	175	350	ns
		10	—	75	150	
		15	—	50	100	

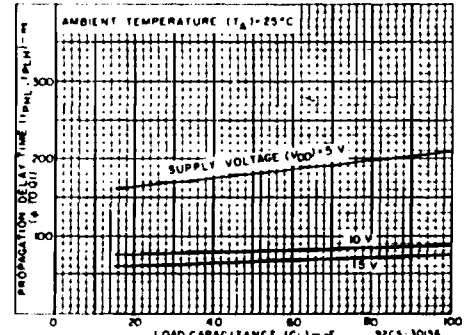


Fig. 10 - Typical propagation delay time as a function of load capacitance ( $\phi$  to  $Q_1$ ).

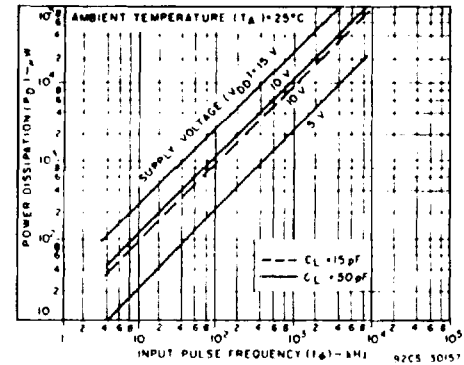


Fig. 11 - Typical dynamic power dissipation as a function of input pulse frequency for CD4020B.

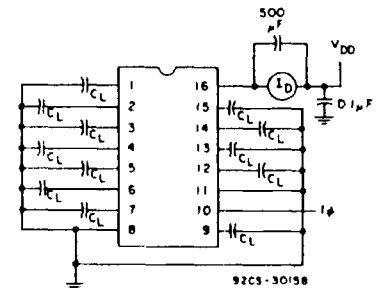


Fig. 12 - Dynamic power dissipation test circuit for CD4020B.

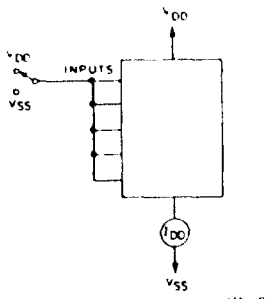


Fig. 13 - Quiescent device current test circuit.

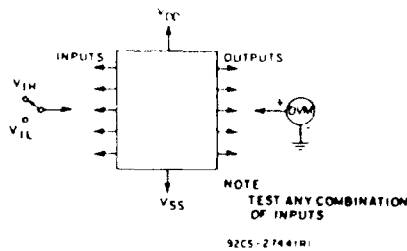


Fig. 14 - Input voltage test circuits.

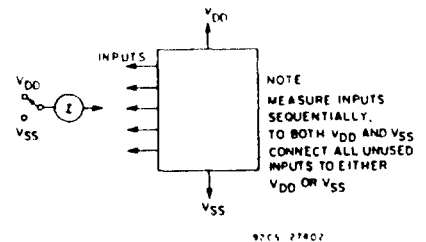


Fig. 15 - Input current test circuit.