



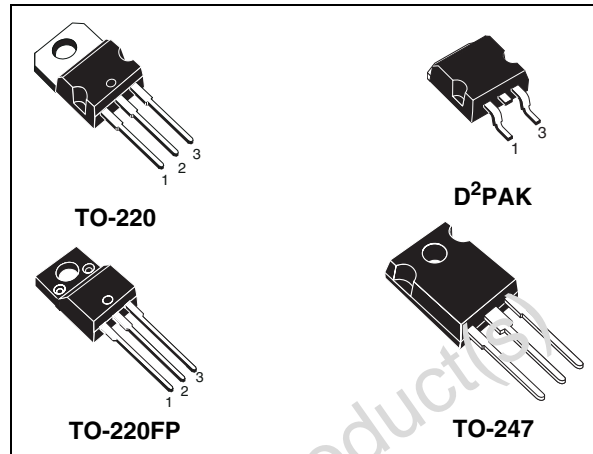
# STP40N20 - STF40N20 STB40N20 - STW40N20

N-channel 200V - 0.038Ω -40A- D<sup>2</sup>PAK/TO-220/TO-220FP/TO-247  
Low gate charge STripFET™ Power MOSFET

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>W</sub>
STB40N20	200V	<0.045Ω	40A	160W
STP40N20	200V	<0.045Ω	40A	160W
STP40N20FP	200V	<0.045Ω	40A	160W
STW40N20	200V	<0.045Ω	40A	40W

- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability
- Excellent figure of merit (R<sub>DS</sub>\*Q<sub>g</sub>)
- 100% avalanche tested



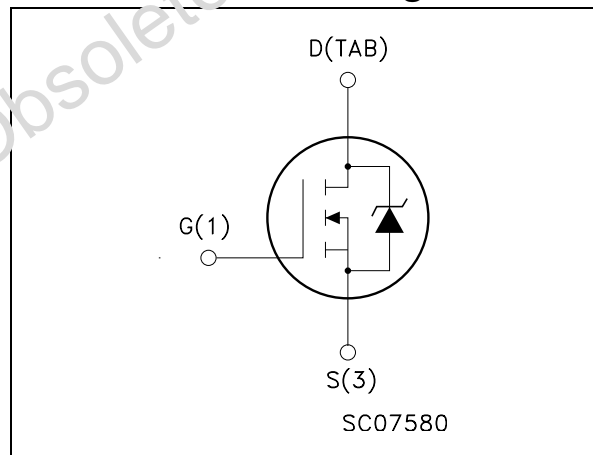
## Description

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters.

## Applications

- Switching application

## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STB40N20	B40N20	D <sup>2</sup> PAK	Tape & reel
STP40N20	P40N20	TO-220	Tube
STP40N20FP	P40N20	TO-220FP	Tube
STW40N20	W40N20	TO-247	Tube

# Contents

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Obsolete Product(s) - Obsolete Product(s)

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220 D <sup>2</sup> PAK TO-247	TO-220FP	
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	200		V
V <sub>GS</sub>	Gate- source voltage	± 20		V
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 25°C	40		A
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 100°C	25		A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	160		A
P <sub>tot</sub>	Total dissipation at T <sub>C</sub> = 25°C	160	40	W
	Derating Factor	1.28	0.32	
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	12		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1s; T <sub>c</sub> = 25°C)	--	2500	V
T <sub>stg</sub>	Storage temperature	-55 to 150		°C
T <sub>j</sub>	Max. operating junction temperature			

- Value limited by wire bonding
- Pulse width limited by safe operating area.
- I<sub>SD</sub> ≤ 40A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>

**Table 2. Thermal data**

		TO-220 D <sup>2</sup> PAK	TO-247	TO-220FP	
R <sub>thj-case</sub>	Thermal resistance junction-case max	0.78		3.1	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max	62.5	50	62.5	°C/W
T <sub>J</sub>	Maximum lead temperature for soldering purpose <sup>(1)</sup>	300			°C

- for 10 sec. 1.6mm from case

**Table 3. Avalanche characteristics**

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	40	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	230	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1mA, V_{GS} = 0$	200			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max ratings}$ $V_{DS} = \text{max ratings},$ $T_C = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 20A$		0.038	0.045	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 20A$		30		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1MHz,$ $V_{GS} = 0$		2500 510 78		pF pF pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 100V, I_D = 20A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see <a href="#">Figure 16</a> )		20 44 74 22		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 160V, I_D = 40A,$ $V_{GS} = 10V$ (see <a href="#">Figure 17</a> )		75 13.2 35.5		nC nC nC

1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				40 160	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20A, V_{GS} = 0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 20A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 25V$ (see <a href="#">Figure 18</a> )		192 922 9.6		ns nC A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 20A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 25V, T_j = 150^\circ C$ (see <a href="#">Figure 18</a> )		242 1440 11.9		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220/D<sup>2</sup>PAK

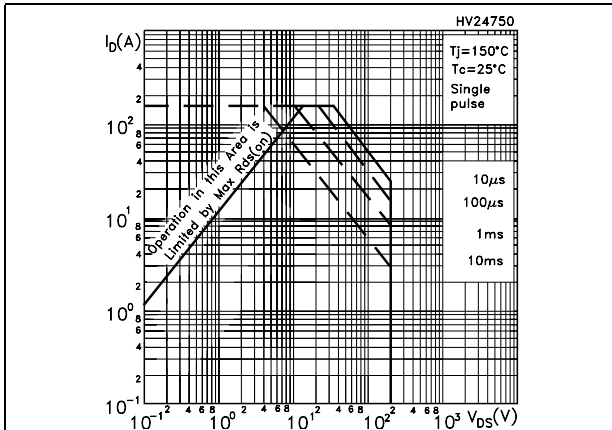


Figure 2. Thermal impedance area for TO-220/D<sup>2</sup>PAK

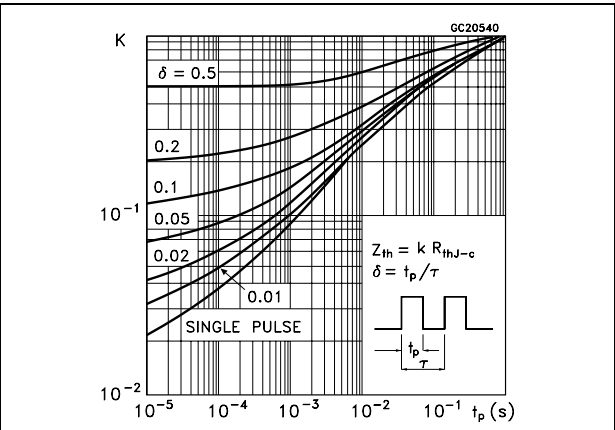


Figure 3. Safe operating area for TO-247

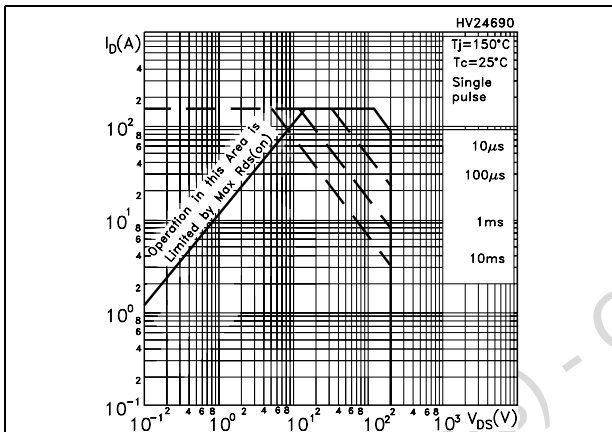


Figure 4. Thermal impedance for TO-247

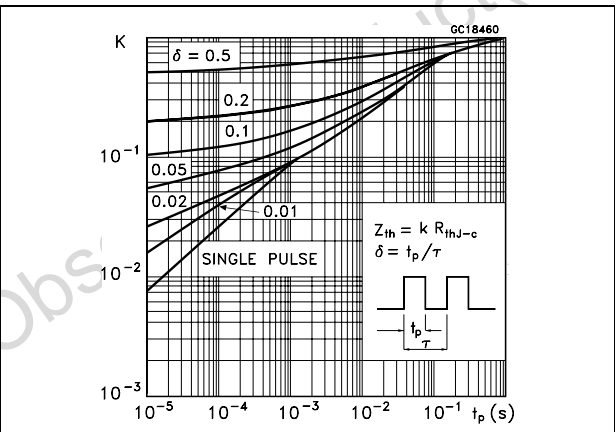


Figure 5. Safe operating area for TO-220FP

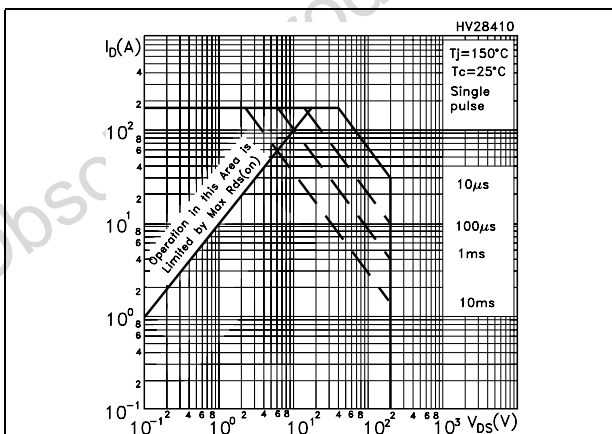


Figure 6. Thermal impedance for TO-220FP

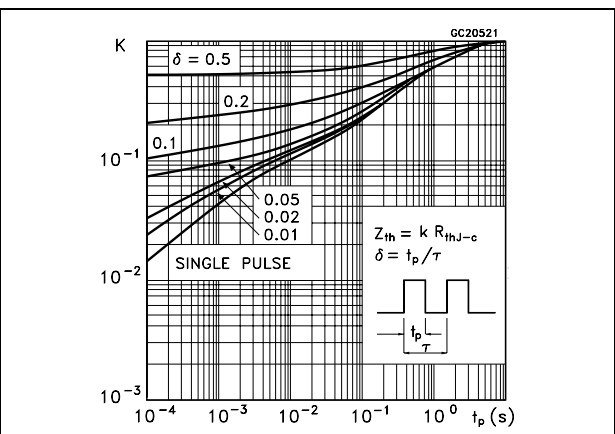


Figure 7. Output characteristics

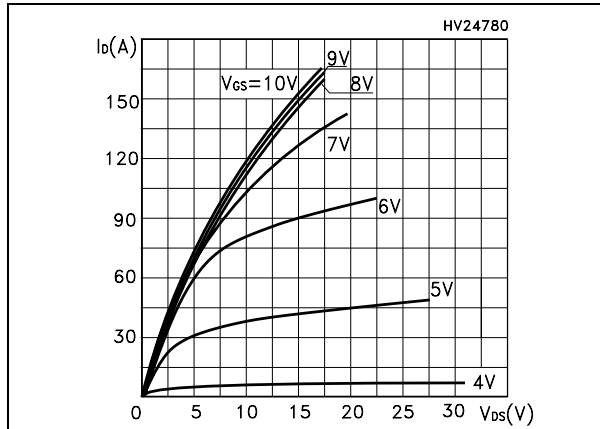


Figure 8. Transfer characteristics

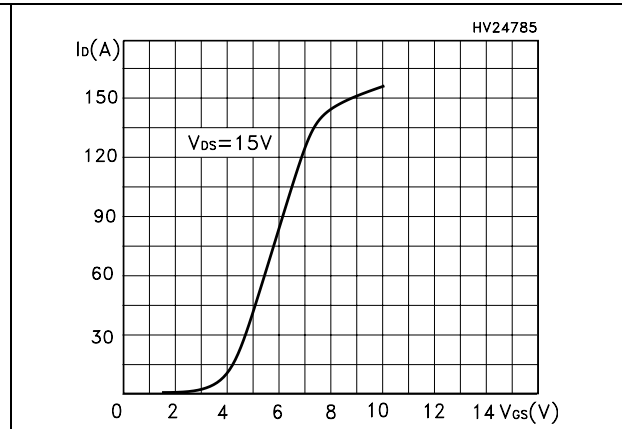


Figure 9. Transconductance

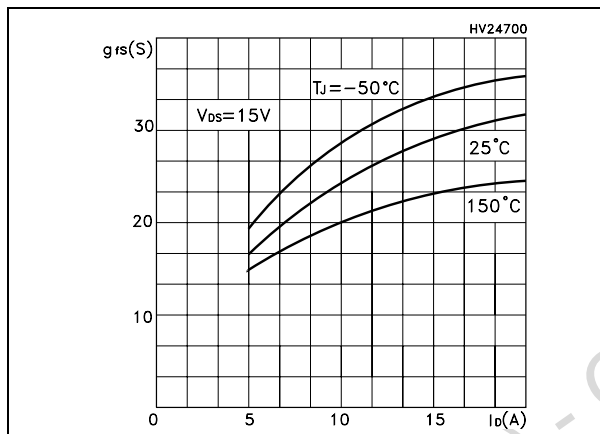


Figure 10. Static drain-source on resistance

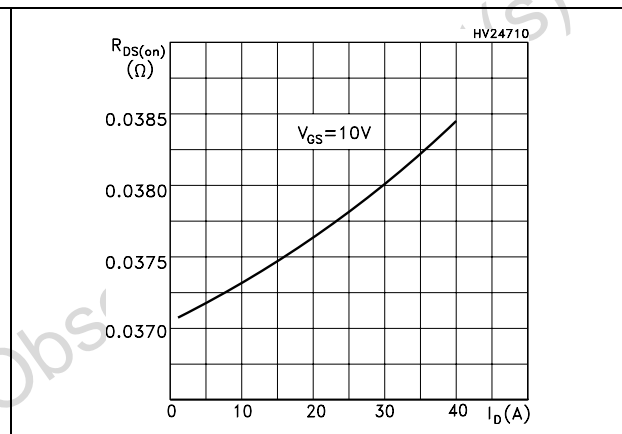


Figure 11. Gate charge vs gate-source voltage Figure 12. Capacitance variations

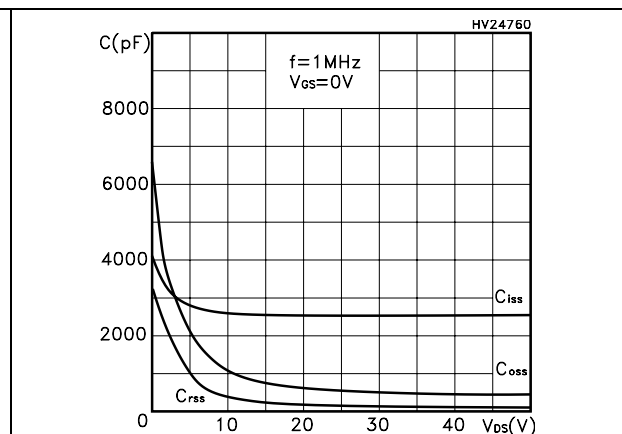
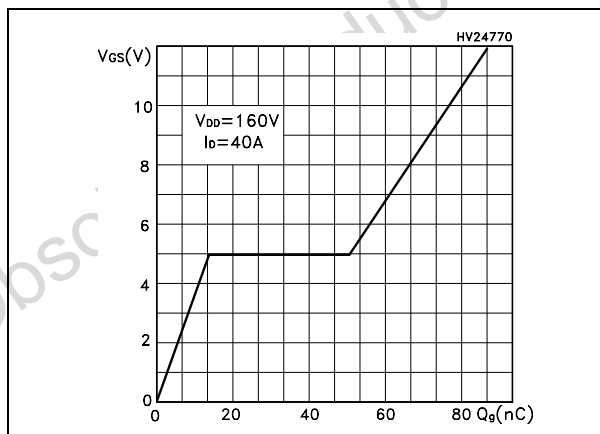


Figure 13. Normalized gate threshold voltage vs temperature

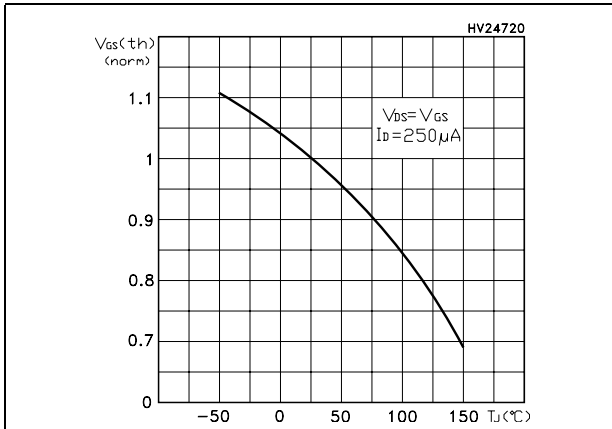


Figure 14. Normalized on resistance vs temperature

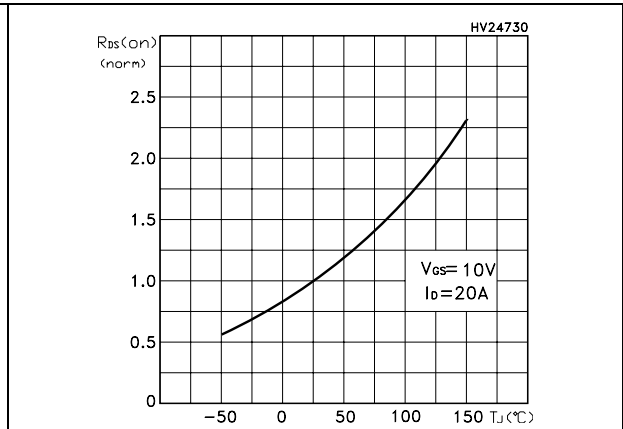
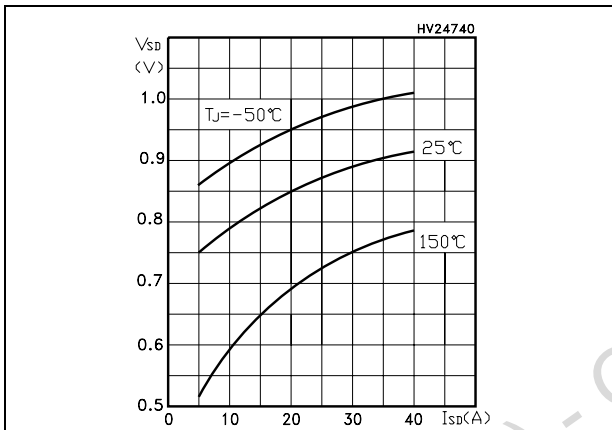


Figure 15. Source-drain diode forward characteristics





### 3 Test circuit

Figure 16. Switching times test circuit for resistive load



Figure 17. Gate charge test circuit

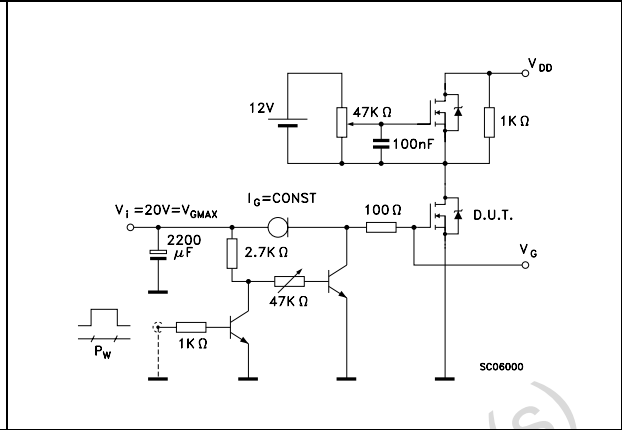


Figure 18. Test circuit for inductive load switching and diode recovery times

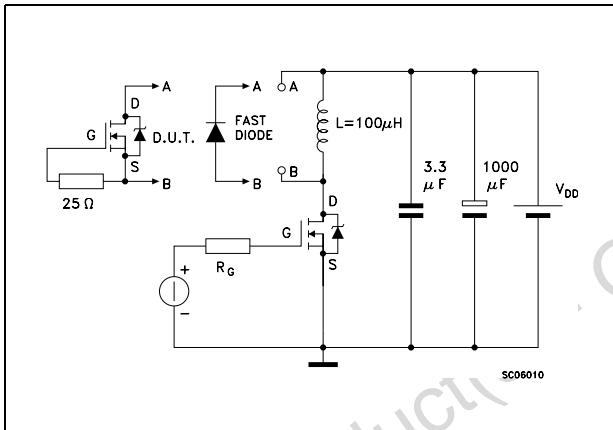


Figure 19. Unclamped Inductive load test circuit

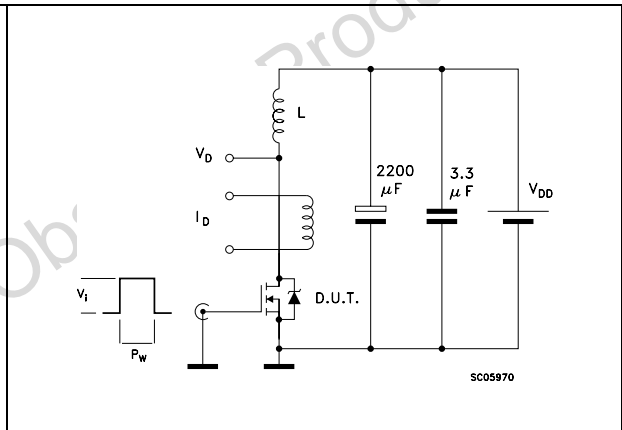


Figure 20. Unclamped inductive waveform

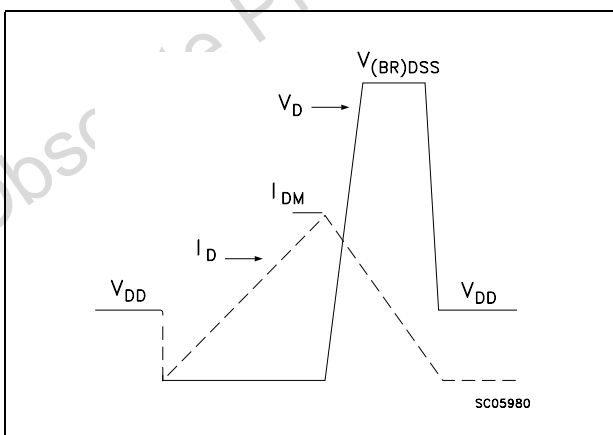
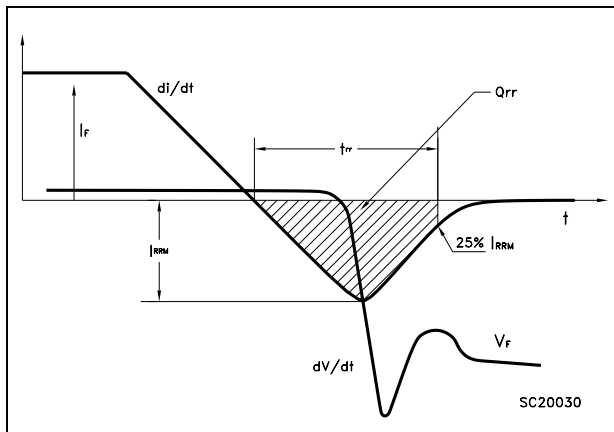


Figure 21. Switching time waveform



Figure 22. Diode recovery times waveform



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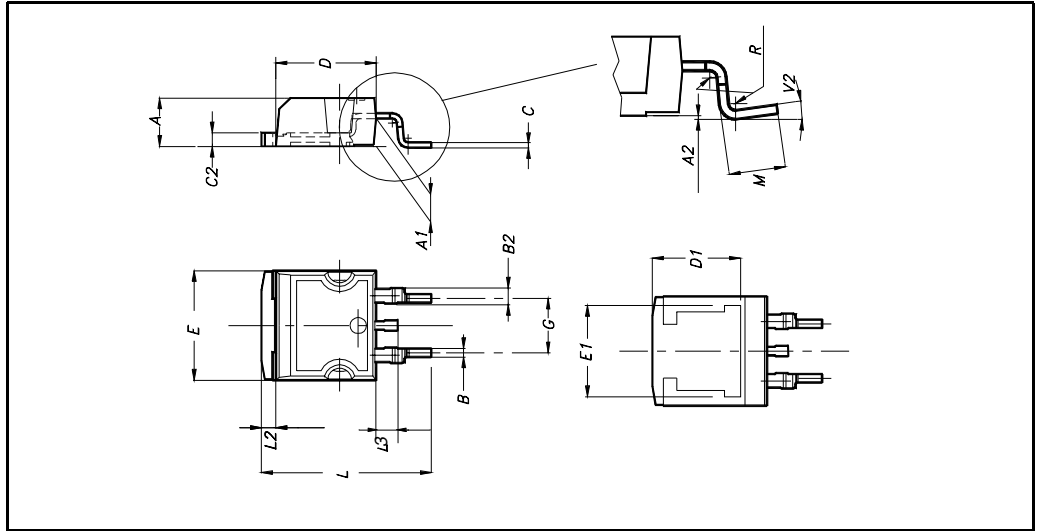
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

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**D<sup>2</sup>PAK MECHANICAL DATA**

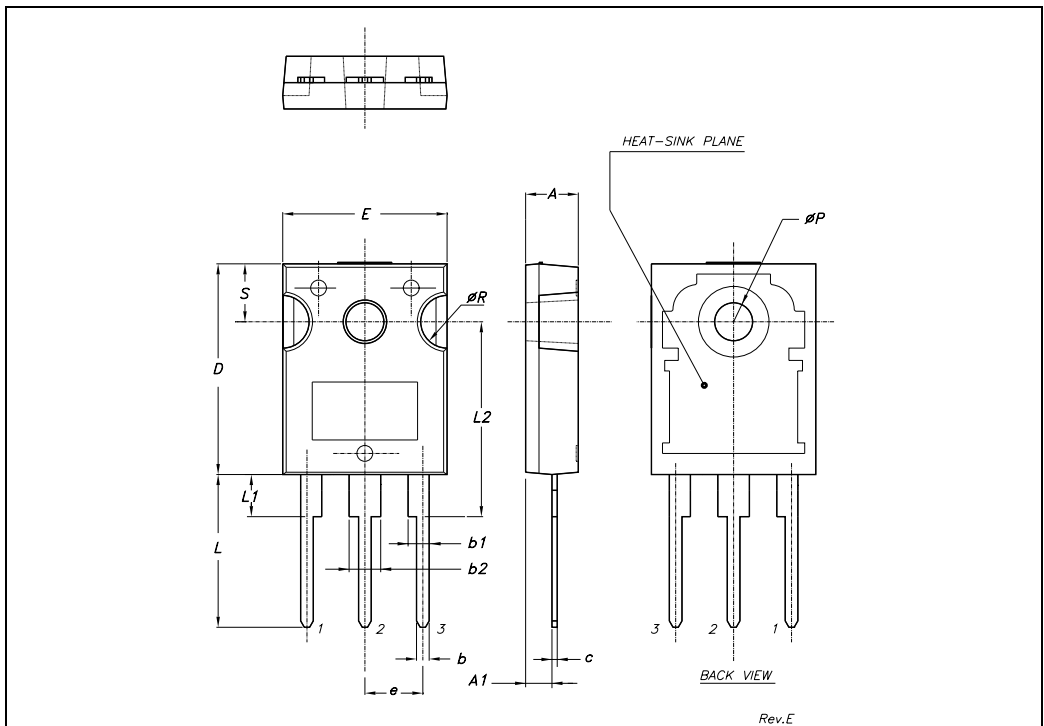
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



Obsole

**TO-247 MECHANICAL DATA**

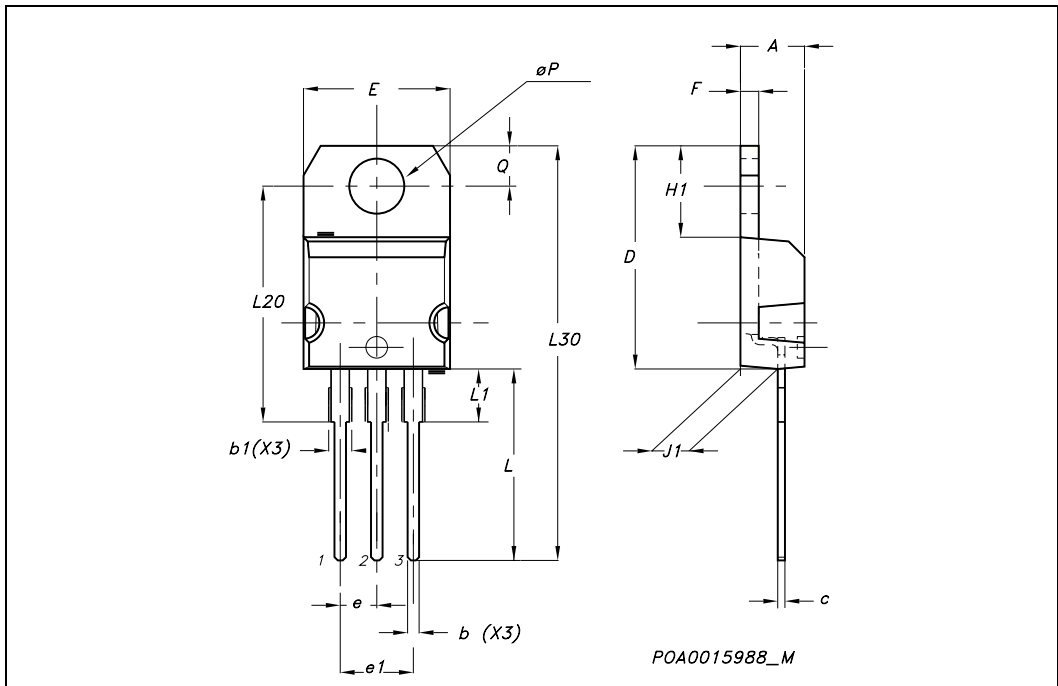
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



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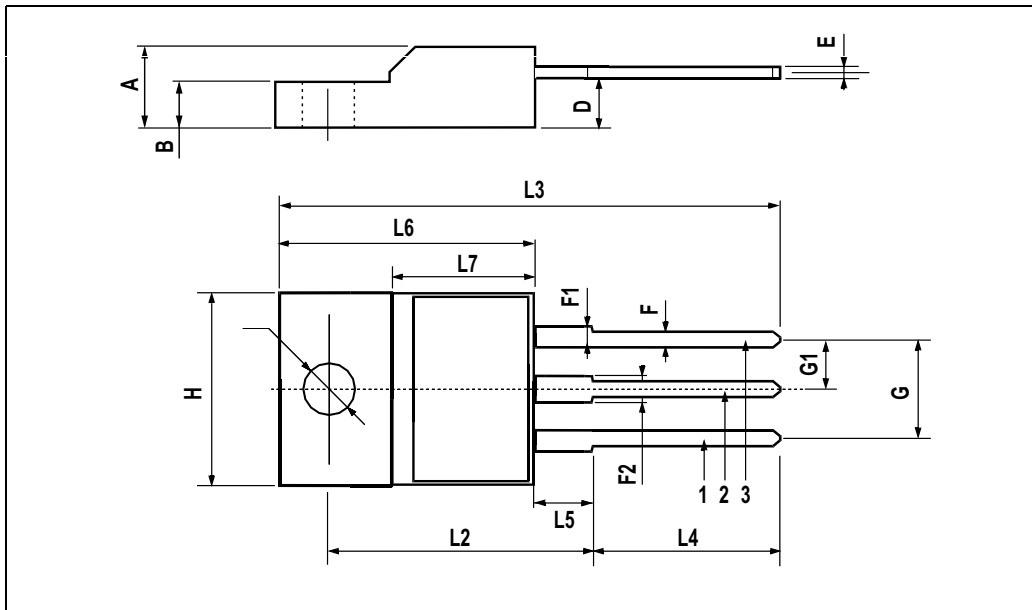
**TO-220 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



**TO-220FP MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



Obsole

# 5 Packaging mechanical data

## D<sup>2</sup>PAK FOOTPRINT



## TAPE AND REEL SHIPMENT

**TAPE MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

**REEL MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

\* on sales type



## 6 Revision history

Table 7. Revision history

Date	Revision	Changes
09-Feb-2005	1	First version
09-Jun-2005	2	Complete version with curves
09-Nov-2005	3	Inserted D <sup>2</sup> PAK package
15-Mar-2006	4	Inserted TO-220FP package
16-Aug-2006	5	New template, no content change

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