8961725 0077217 8

NOVEMBER 1985 — REVISED APRIL 1988

*This Data Sheet is Applicable to All TMS27C512s and TMS27PC512s Symbolized with Code "A" as Described on Page 12.*

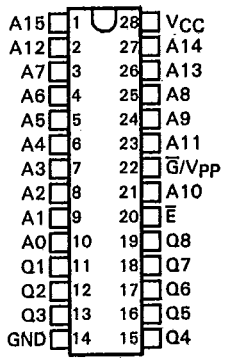
- **Organization . . . 64K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible with Existing 512K MOS ROMs, PROMs, and EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**

| $V_{CC}$ ±5% | $V_{CC}$ ±10% | |
|---|---|---|
| '27C512-1 | '27C512-17 | 170 ns |
| '27C/PC512-2 | '27C/PC512-20 | 200 ns |
| '27C/PC512 | '27C/PC512-25 | 250 ns |
| '27C/PC512-3 | '27C/PC512-30 | 300 ns |

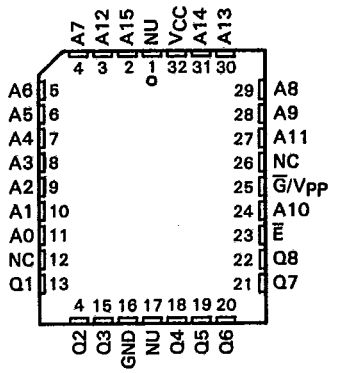
- **Power Saving CMOS Technology**
- **Very High-Speed SNAP! Pulse Programming or Fast Programming Algorithms**
- **3-State Output Buffers**
- **400 mV Guaranteed DC Noise Immunity with Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation ($V_{CC}$ = 5.25 V)**
  - **Active . . . 158 mW Worst Case**
  - **Standby . . . 1.4 mW Worst Case (CMOS Input Levels)**
- **PEP4 Version Available with 168 Hour Burn-In, and also Guaranteed Operating Temperature Ranges**
- **512K EPROM Available with MIL-STD-883C Class B High Reliability Processing (SMJ27C512)**

**J AND N PACKAGE**
**(TOP VIEW)**

T-46-13-25
T-46-13-29




**FM PACKAGE**
**(TOP VIEW)**




EPROMs/PROMs/EEPROMs

6

TEXAS INSTR (ASIC/MEMORY) 25E D

## description

The TMS27C512 series are 524,288-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC512 series are 524, 288-bit, one-time, electrically programmable read-only memories.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by

| PIN NOMENCLATURE | |
|---|---|
| A0-A15 | Address Inputs |
| $\overline{E}$ | Chip Enable/Power Down |
| $\overline{G}/V_{PP}$ | 12-13 V Programming Power Supply |
| GND | Ground |
| NC | No Connection |
| NU | Make No External Connection |
| Q1-Q8 | Outputs |
| $V_{CC}$ | 5-V Power Supply |





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Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C512 and the TMS27PC512 are pin compatible with 28-pin 512K MOS ROMs, PROMs, and EPROMs.

The TMS27C512 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C512 is available with two guaranteed temperature ranges of 0°C to 70°C and −40°C to 85°C (TMS27C512-_ _JL and TMS27C512-_ _JE, respectively). The TMS27C512 is also offered with 168 hour burn-in on both temperature ranges (TMS27C512-_ _JL4 and TMS27C512-_ _JE4, respectively). (See table below.)

The TMS27PC512 PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC512 is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix). The TMS27PC512 is guaranteed for operation from 0°C to 70°C.

All package styles conform to JEDEC standards.



| EPROM | SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN | | SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES | |
|---|---|---|---|---|
| | 0°C TO 70°C | −40°C TO 85°C | 0°C TO 70° | −40°C TO 85°C |
| TMS27C512-XXX | JL | JE | JL4 | JE4 |

These EPROMs and PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 12-13 V supply is needed for programming. All programming signals are TTL level. These devices are programmable by either Fast or SNAP! Pulse programming algorithms. Fast programming uses a $V_{PP}$ of 12.5 V and a $V_{CC}$ of 6.0 V for a nominal programming time of two minutes. SNAP! Pulse programming uses a $V_{PP}$ of 13.0 V and a $V_{CC}$ of 6.5 V for a nominal programming time of four seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

## operation

There are seven modes of operation listed in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for $V_{PP}$ during programming (12.5 V for Fast or 13.0 V for SNAP! Pulse) and 12 V on A9 for signature mode.

| FUNCTION | MODE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Read | Output Disable | Standby | Programming | Verify | Program Inhibit | Signature Mode | |
| $\overline{E}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | |
| $\overline{G}/V_{PP}$ | $V_{IL}$ | $V_{IH}$ | X† | $V_{PP}$ | $V_{IL}$ | $V_{PP}$ | $V_{IL}$ | |
| $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | |
| A9 | X | X | X | X | X | X | $V_H$‡ | $V_H$‡ |
| A0 | X | X | X | X | X | X | $V_{IL}$ | $V_{IH}$ |
| Q1-Q8 | $D_{OUT}$ | HI-Z | HI-Z | $D_{IN}$ | $D_{OUT}$ | HI-Z | CODE | |
| | | | | | | | MFG | DEVICE |
| | | | | | | | 97 | 85 |

†X Can be $V_{IL}$ or $V_{IH}$.
‡$V_H$ = 12 V ± 0.5 V.



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**read/output disable**

When outputs of two or more TMS27C512s or TMS27PC512s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$/$V_{PP}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 through Q8.

**latchup immunity**

Latchup immunity on the TMS27C512 and TMS27PC512 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001; *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family,"* available through TI Field Sales Offices.

**power down**

Active $I_{CC}$ current can be reduced from 30 mA to 500 $\mu$A (TTL-level inputs) or 250 $\mu$A (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

**erasure (TMS27C512)**

Before programming, the TMS27C512 EPROM is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). EPROM erasure before programming is necessary to assure that all bits are in the logic 1 (high) state. Logic 0s are programmed into the desired locations. A programmed logic 0 can be erased only by ultraviolet light. The recommended minimum ultraviolet light exposure dose (UV intensity × exposure time) is 15 watt-seconds per square centimeter. A typical 12-milliwatt-per-square-centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C512, the window should be covered with an opaque label.

**initializing (TMS27PC512)**

The one-time programmable TMS27PC512 PROM is provided with all bits in the logic 1 state, then logic 0s are programmed into the desired locations. Logic 0s programmed into a PROM cannot be erased.

**SNAP! Pulse programming**

The 512K EPROM and PROM can be programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which can reduce programming time to a nominal of four seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds ($\mu$s) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-$\mu$s pulses per byte are provided before a failure is recognized.

The programming mode is achieved when $\overline{G}$/$V_{PP}$ = 13.0 V, $V_{CC}$ = 6.5 V, and $\overline{E}$ = $V_{IL}$. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified when $V_{CC}$ = 5 V, $\overline{G}$/$V_{PP}$ = $V_{IL}$, and $\overline{E}$ = $V_{IL}$.

**Fast programming**

The 512K EPROM and PROM can be programmed using the Fast programming algorithm illustrated by the flowchart in Figure 2. During Fast programming, data is presented in parallel (eight bits) on pins Q1 through Q8. Once addresses and data are stable, $\overline{E}$ is pulsed. The programming mode is achieved when $\overline{G}/V_{PP}$ = 12.5 V, $V_{CC}$ = 6.0 V, and $\overline{E} = V_{IL}$. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Fast programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at $V_{CC}$ = 6.0 V and $\overline{G}/V_{PP}$ = 12.5 V. When the full Fast programming routine is complete, all bits are verified when $V_{CC}$ = 5 V and $\overline{G}/V_{PP} = V_{IL}$.

**program inhibit**

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

**program verify**

Programmed bits may be verified when $\overline{G}/V_{PP}$ and $\overline{E} = V_{IL}$.

**signature mode**

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., A0 = $V_{IL}$ accesses the manufacturer code, which is output on Q1-Q8; A0 = $V_{IH}$ accesses the device code, which is output on Q1-Q8. All other addresses must be held at $V_{IL}$. Each byte possesses odd parity on bit Q8. The manufacturer code for these devices is 97, and the device code is 85.



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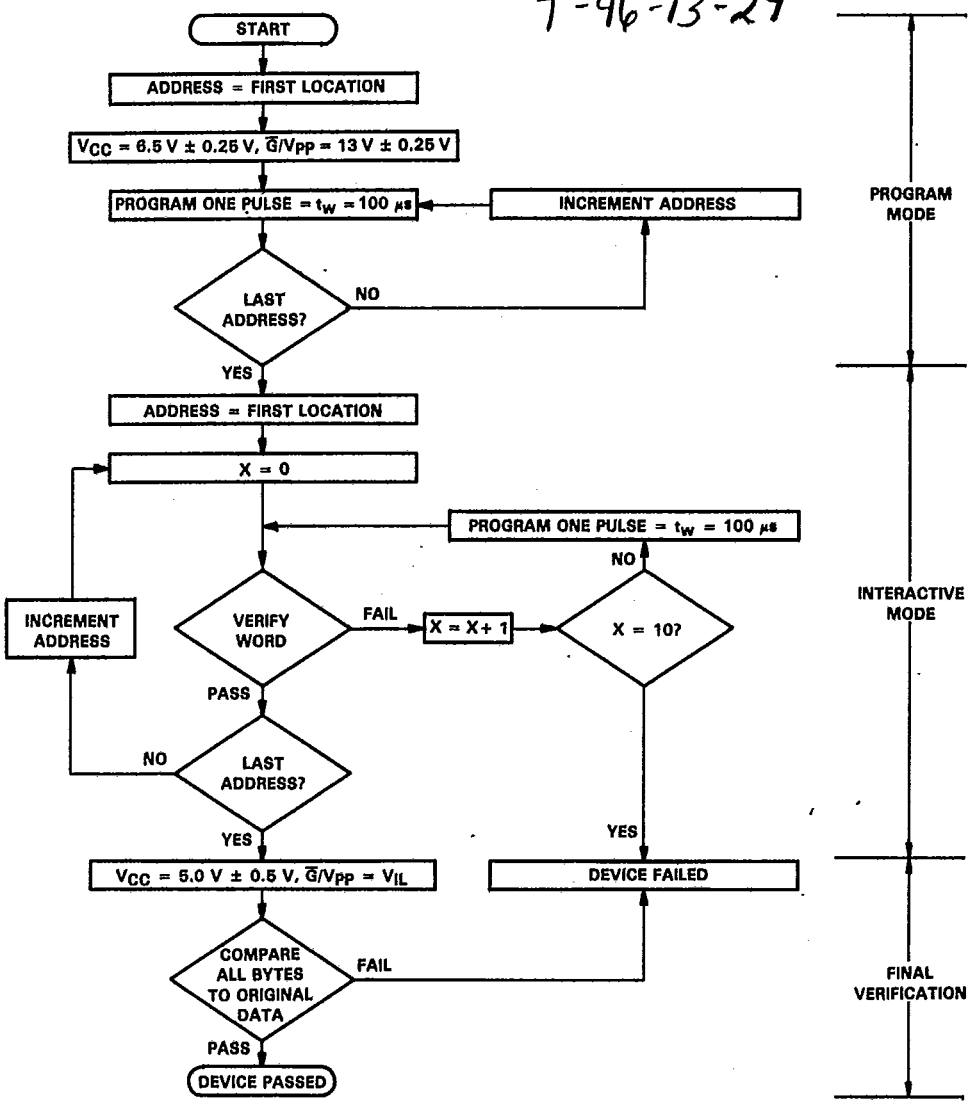


FIGURE 1. SNAP! PULSE PROGRAMMING FLOWCHART

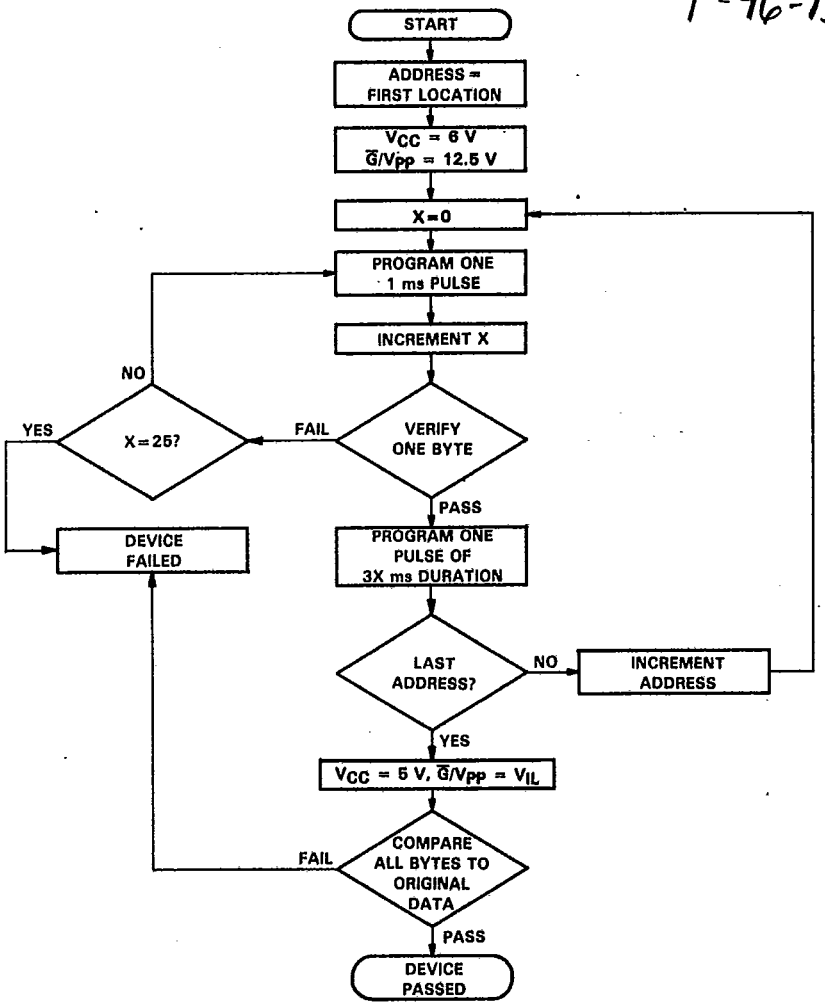


FIGURE 2. FAST PROGRAMMING FLOWCHART



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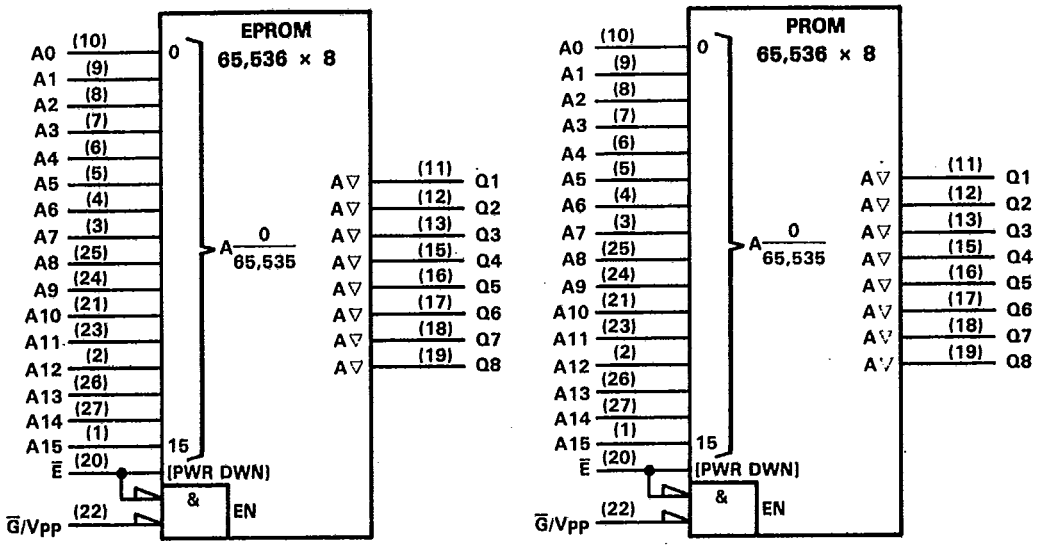
**logic symbols†**




†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, $V_{PP}$ (see Note 1) . . . . . −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 . . . . . −0.6 V to 6.5 V
A9 . . . . . −0.6 V to 13.5 V
Output voltage range (see Note 1) . . . . . −0.6 V to $V_{CC}$ + 1 V
Operating free-air temperature range ('27C512-_ _JL and JL4; '27PC512-_ _NL and FML) . . . . . 0°C to 70°C
Operating free-air temperature range ('27C512-_ _JE and JE4) . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

### recommended operating conditions

| | | | '27C512-1 '27C/PC512-2 '27C/PC512 '27C/PC512-3 | | | '27C512-17 '27C/PC512-20 '27C/PC512-25 '27C/PC512-30 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | Read mode (see Note 2) | 4.75 | 5 | 5.25 | 4.5 | 5 | 5.5 | V |
| | | Fast programming algorithm | 5.75 | 6 | 6.25 | 5.75 | 6 | 6.25 | V |
| | | SNAP! Pulse programming algorithm | 6.25 | 6.5 | 6.75 | 6.25 | 6.5 | 6.75 | V |
| $\overline{G}/V_{PP}$ | Supply voltage | Fast programming algorithm | 12 | 12.5 | 13 | 12 | 12.5 | 13 | V |
| | | SNAP! Pulse programming algorithm | 12.75 | 13.0 | 13.25 | 12.75 | 13.0 | 13.25 | V |
| $V_{IH}$ | High-level input voltage | TTL | 2 | | $V_{CC}+1$ | 2 | | $V_{CC}+1$ | V |
| | | CMOS | $V_{CC}-0.2$ | | $V_{CC}+1$ | $V_{CC}-0.2$ | | $V_{CC}+1$ | V |
| $V_{IL}$ | Low-level input voltage | TTL | −0.5 | | 0.8 | −0.5 | | 0.8 | V |
| | | CMOS | −0.5 | | 0.2 | −0.5 | | 0.2 | V |
| $T_A$ | Operating free-air temperature (See table, page 2) | | (See table, page 2) | | | (See table, page 2) | | | °C |

NOTE 2: $V_{CC}$ must be applied before or at the same time as $\overline{G}/V_{PP}$ and removed after or at the same time as $\overline{G}/V_{PP}$. The device must not be inserted into or removed from the board when $V_{PP}$ or $V_{CC}$ is applied.

### electrical characteristics over full ranges of recommended operating conditions

| PARAMETER | | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | | $I_{OH} = -2.5$ mA | 3.5 | | | V |
| | | | $I_{OH} = -20\ \mu$A | $V_{CC}-0.1$ | | | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL} = 2.1$ mA | | | 0.4 | V |
| | | | $I_{OL} = 20\ \mu$A | | | 0.1 | V |
| $I_I$ | Input current (leakage) | | $V_I = 0$ V to 5.5 V | | | ±1 | μA |
| $I_O$ | Output current (leakage) | | $V_O = 0$ V to $V_{CC}$ | | | ±1 | μA |
| $I_{PP}$ | $\overline{G}/V_{PP}$ supply current (during program pulse) | | $\overline{G}/V_{PP} = 13$ V | | 35 | 50 | mA |
| $I_{CC1}$ | $V_{CC}$ supply current (standby) | TTL-input level | $V_{CC} = 5.5$ V, $\overline{E} = V_{IH}$ | | 250 | 500 | μA |
| | | CMOS-input level | $V_{CC} = 5.5$ V, $\overline{E} = V_{CC}$ | | 100 | 250 | μA |
| $I_{CC2}$ | $V_{CC}$ supply current (active) | | $V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, $t_{cycle}$ = minimum cycle time, outputs open | | 15 | 30 | mA |

†Typical values are at $T_A = 25$°C and nominal voltages.

### capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz‡

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_i$ | Input capacitance | $V_I = 0$ V, f = 1 MHz | | 6 | 10 | pF |
| $C_o$ | Output capacitance | $V_O = 0$ V, f = 1 MHz | | 10 | 14 | pF |
| $C_{G/VPP}$ | $\overline{G}/V_{PP}$ input capacitance | $\overline{G}/V_{PP} = 0$ V, f = 1 MHz | | 20 | 25 | pF |

†Typical values are at $T_A = 25$°C and nominal voltages.
‡Capacitance measurements are made on sample basis only.



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**switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)**

| PARAMETER | | TEST CONDITIONS (SEE NOTES 3 AND 4) | '27C512-1 '27C512-17 | | '27C/PC512-2 '27C/PC512-20 | | '27C/PC512 '27C/PC512-25 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{a(A)}$ | Access time from address | $C_L$ = 100 pf, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns | | 170 | | 200 | | 250 | ns |
| $t_{a(E)}$ | Access time from chip enable | | | 170 | | 200 | | 250 | ns |
| $t_{en(G)}$ | Output enable time from $\overline{G}/V_{PP}$ | | | 75 | | 75 | | 100 | ns |
| $t_{dis}$ | Output disable time from $\overline{G}/V_{PP}$ or $\overline{E}$, whichever occurs first† | | 0 | 60 | 0 | 60 | 0 | 60 | ns |
| $t_{v(A)}$ | Output data valid time after change of address, $\overline{E}$, or $\overline{G}/V_{PP}$, whichever occurs first† | | 0 | | 0 | | 0 | | ns |



| PARAMETER | | TEST CONDITIONS (SEE NOTES 3 AND 4) | '27C/PC512-3 '27C/PC512-30 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{a(A)}$ | Access time from address | $C_L$ = 100 pf, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns Input $t_f \leq 20$ ns | | 300 | ns |
| $t_{a(E)}$ | Access time from chip enable | | | 300 | ns |
| $t_{en(G)}$ | Output enable time from $\overline{G}/V_{PP}$ | | | 120 | ns |
| $t_{dis}$ | Output disable time from $\overline{G}/V_{PP}$ or $\overline{E}$, whichever occurs first† | | 0 | 105 | ns |
| $t_{v(A)}$ | Output data valid time after change of address, $\overline{E}$, or $\overline{G}/V_{PP}$, whichever occurs first† | | 0 | | ns |

†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

**switching characteristics for programming: $V_{CC}$ = 6 V and $\overline{G}/V_{PP}$ = 12.5 V (Fast) or $V_{CC}$ = 6.50 V and $\overline{G}/V_{PP}$ = 13.0 V (SNAP! Pulse), $T_A$ = 25°C (see Note 3)**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{dis(G)}$ | Output disable time from $\overline{G}/V_{PP}$ | 0 | | 130 | ns |

NOTES: 3. For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0. (Reference page 11.)
4. Common test conditions apply for $t_{dis}$ except during programming.

**recommended timing requirements for programming: $V_{CC}$ = 6 V and $\overline{G}/V_{PP}$ = 12.5 V (Fast) or $V_{CC}$ = 6.50 V and $\overline{G}/V_{PP}$ = 13.0 V (SNAP! Pulse), $T_A$ = 25°C (see Note 3)**

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{w(IPGM)}$ | Initial program pulse duration | Fast programming algorithm | 0.95 | 1 | 1.05 | ms |
| | | SNAP! Pulse programming algorithm | 95 | 100 | 105 | µs |
| $t_{w(FPGM)}$ | Final pulse duration | Fast programming only | 2.85 | | 78.75 | ms |
| $t_{su(A)}$ | Address setup time | | 2 | | | µs |
| $t_{su(D)}$ | Data setup time | | 2 | | | µs |
| $t_{su(VPP)}$ | $\overline{G}/V_{PP}$ setup time | | 2 | | | µs |
| $t_{su(VCC)}$ | $V_{CC}$ setup time | | 2 | | | µs |
| $t_{h(A)}$ | Address hold time | | 0 | | | µs |
| $t_{h(D)}$ | Data hold time | | 2 | | | µs |
| $t_{h(VPP)}$ | $\overline{G}/V_{PP}$ hold time | | 2 | | | µs |
| $t_{rec(PG)}$ | $\overline{G}/V_{PP}$ recovery time | | 2 | | | µs |
| $t_{EHD}$ | Data valid from $\overline{E}$ low | | | | 1 | µs |
| $t_{r(PG)G}$ | $\overline{G}/V_{PP}$ rise time | | 50 | | | ns |

NOTE 3. For all switching characteristics the input pulse levels are 0.40 V to 2.4 V. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0. (Reference page 11.)



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## PARAMETER MEASUREMENT INFORMATION

T-46-13-29

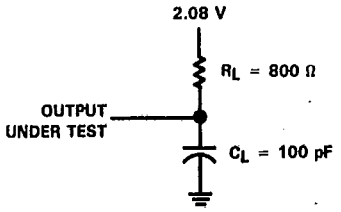
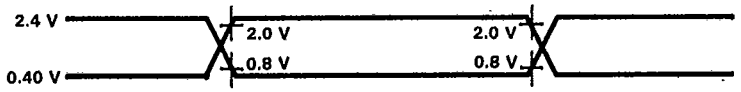


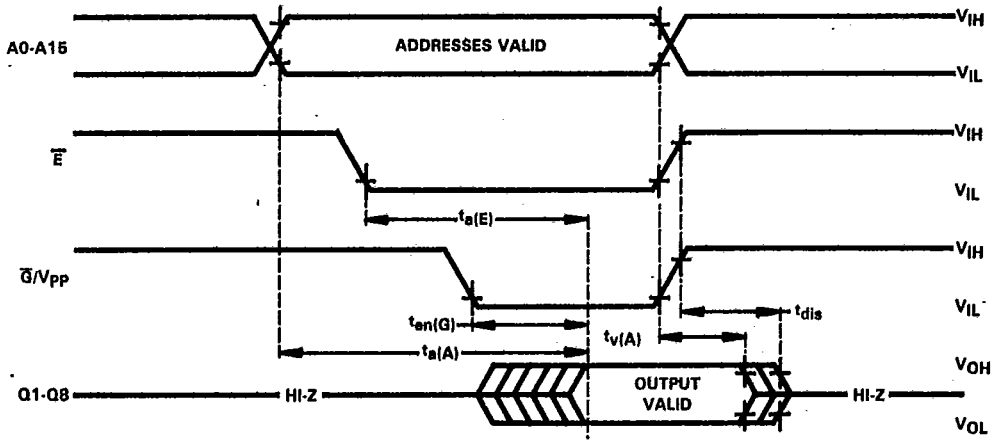

FIGURE 3. OUTPUT LOAD CIRCUIT

### AC testing input/output wave forms

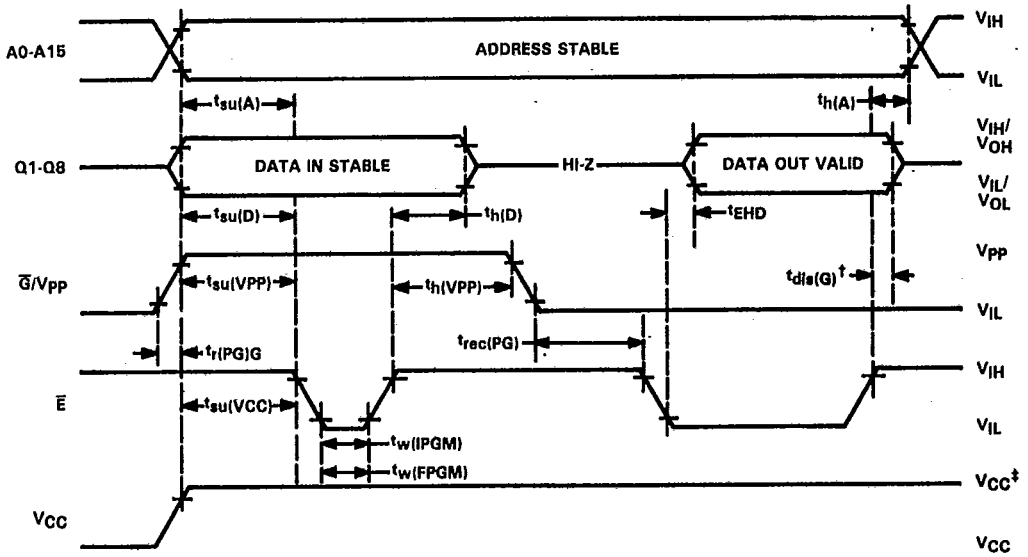



A.C. testing inputs are driven at 2.4 V for logic 1 and 0.4 V for logic 0. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 for both inputs and outputs.

### read cycle timing



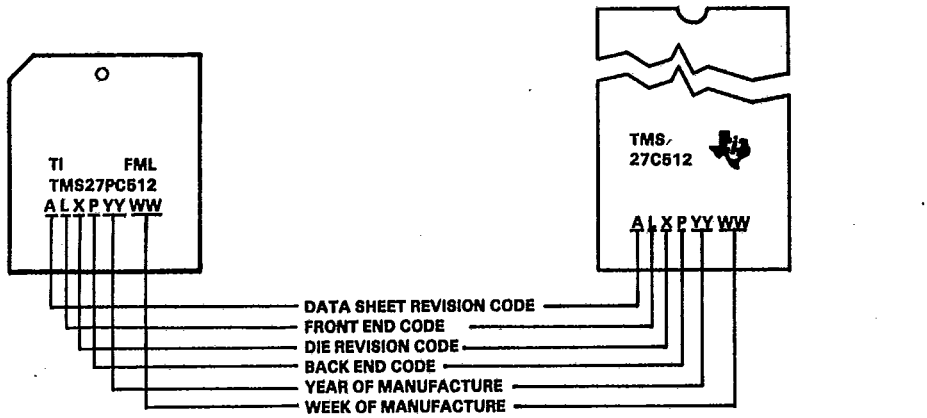
### program cycle timing




†$t_{dis(G)}$ is a characteristic of the device but must be accommodated by the programmer.
‡12.5 V $\overline{G}/V_{PP}$ and 6.0 V $V_{CC}$ for Fast programming; 13.0 V $\overline{G}/V_{PP}$ and 6.50 V $V_{CC}$ for SNAP! Pulse programming.

### device symbolization

This data sheet is applicable to all TI TMS27C512 CMOS EPROMs and TMS27PC512 CMOS PROMs with the code "A" shown below:



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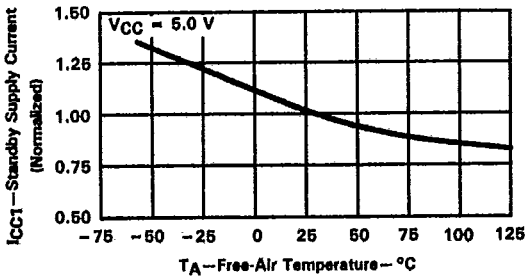
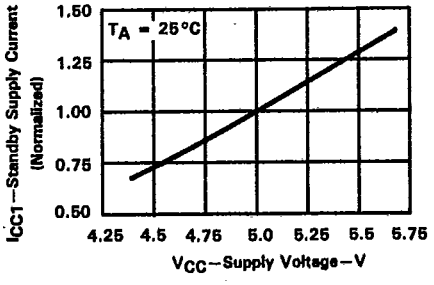
## TYPICAL TMS27C/PC512 CHARACTERISTICS



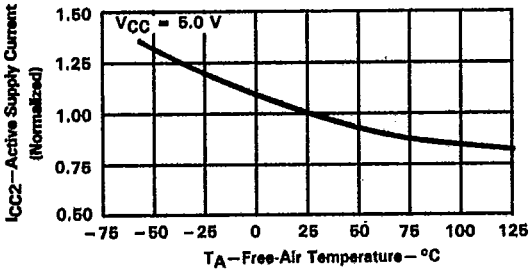
STANDBY SUPPLY CURRENT vs FREE-AIR TEMPERATURE



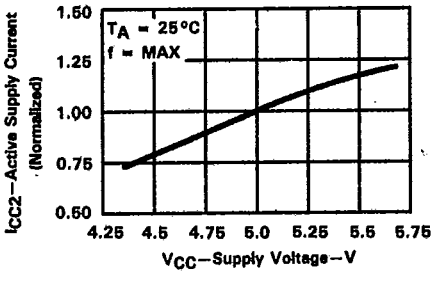

STANDBY SUPPLY CURRENT vs SUPPLY VOLTAGE



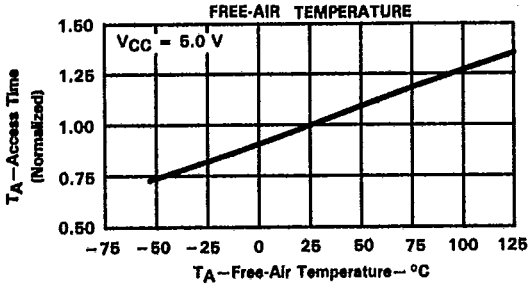

ACTIVE SUPPLY CURRENT vs FREE-AIR TEMPERATURE



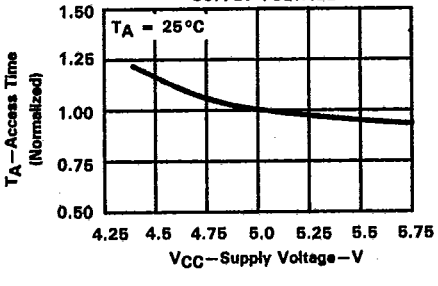

ACTIVE SUPPLY CURRENT vs SUPPLY VOLTAGE




ACCESS TIME vs FREE-AIR TEMPERATURE




ACCESS TIME vs SUPPLY VOLTAGE



# Designing and Manufacturing Surface Mount Assemblies

T-90-20

**Elizabeth Gunther, Charles Hutchins, and Paul Peterson**

The competitive nature of the semiconductor industry has driven vendors to minimize the size of electronic components, so that more functions can be achieved in a given volume. In addition, improved electrical performance, decreased mass, and the potential for lower system cost are all by-products of compacted packaging and circuitry which hold interest to component manufacturers and users alike.

Surface Mount Technology (SMT) offers an excellent method of reducing component size. A typical memory array can be reduced to 50 percent of its original PWB size with single-sided mounting, and 25 to 30 percent with double-sided mounting. Logic designs cannot achieve the same dramatic reduction, but decreases up to 40 to 60 percent can be achieved for single-sided and double-sided assemblies respectively.

The key design and manufacturing process issues must be understood in order to fully reap the benefits of Surface Mount Technology. This article gives a general overview of the key aspects of design, process, and manufacturing of surface mounted assemblies, and offers surface mount as an opportunity to lower a system's cost without sacrificing reliability.

## Components

Most surface mount components are at least one-third the size of the comparable through-hole mounted device (Figure 1). The 68-pin chip carrier is approxmiately one square inch, while the 64-pin DIP is approximately three square inches. The 20-pin chip carrier is slightly larger than 0.1 square inch, while the 20-pin DIP is 0.3 square inch. Similarly, other IC packages are reduced to approximately one-third the size of comparable lead count packages. The passive components occupy approximately one-tenth the board area, and this is why they have been used in most small consumer products built in the last couple of years.

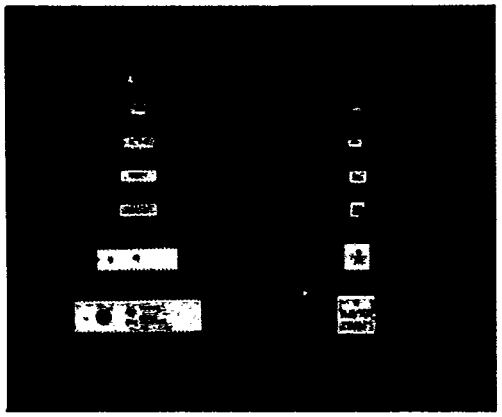


**Figure 1. Component Site Reduction**

There were many references in the recent past to problems with component availability, cost, and standardization. This area of SMT has probably received more attention than any other. Several recent magazine articles now state that significantly more components (particularly actives) are now available and that cost parity has been achieved on most of them. The effort by various industry committees on standardization has also been effective.

Thus, although more needs to be accomplished in these areas, a designer can begin a project with confidence that there will be no insurmountable barriers in this area. There are several consultants and subcontract assembly companies to assist in this effort. It is strongly recommended that all new designs utilize some form of SMT, particularly when space is an important consideration.

## Process

The process to manufacture a surface mount assembly (SMA) is very simple. It consists of four basic steps, as shown in Figure 2. First, the solder paste is screened on the PWB. Then the component is placed on the board, with due care to get it positioned correctly. Typical geometries require placement accuracy of less than plus/minus 4 mils. Next the solder is reflowed with either a vapor phase or infrared system. Finally, the assembly is cleaned and is now ready for test. This process, although simple in concept, relies on board and component planarity and solderability. These are easily achievable with the chip carriers and memory modules we will discuss later.

Texas Instruments has installed a Surface Mount Technology Center at its plant in Houston, Texas. At this center, we have a complete and flexible engineering line to assist our customers in converting to Surface Mount Technology.

The engineering line is equipped with a screen printer, pick and place system, vapor phase reflow, and clean-up station that will easily handle PWBs up to 9″ × 10″. Larger boards up to 14″ × 16″ can be processed with some additional care. TI uses this engineering line to produce its prototype and demo boards. It is also available to any of TI's customers, free of charge, for use in building test or prototype boards.

The effectiveness of the assembly process can be characterized by the number of unacceptable solder joints formed during the process. Unacceptable joints are defined by their electrical and mechanical (strength and reliability) characteristics. The major problem is open solder joints, followed by bridging and misregistration.

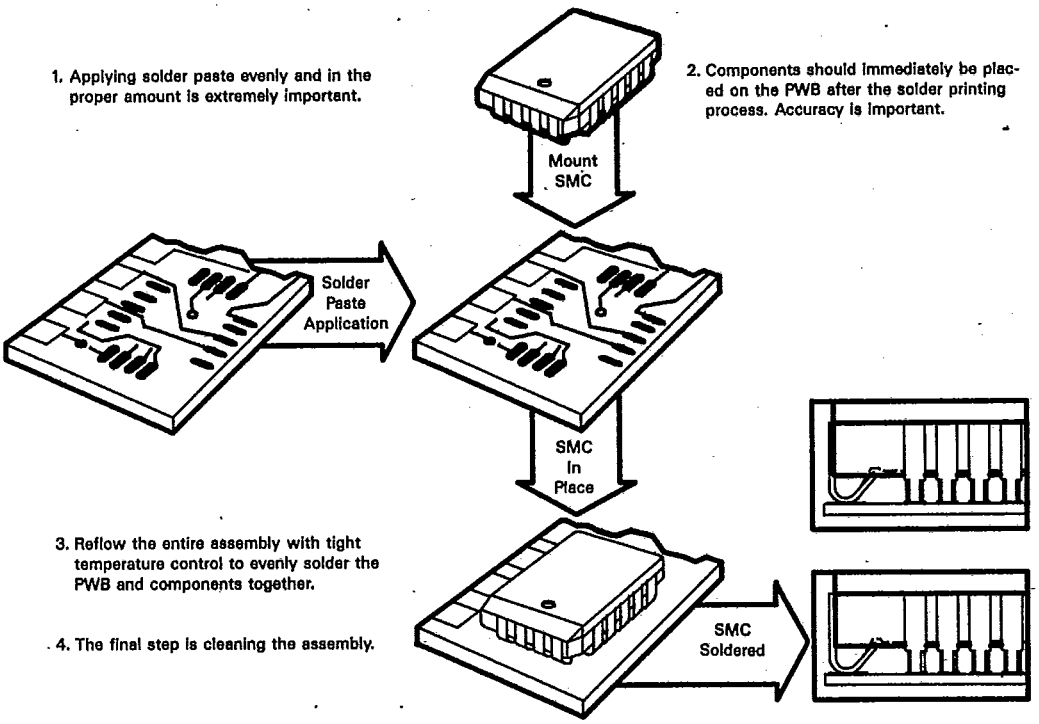



**Figure 2. Basic Process Steps**



Open circuits are detected at electrical test and are the first defects detected after soldering. At Texas Instruments, 10 PPM or less is the desirable defect level. Several factors that contribute to open solder joints were identified during production start-up. Lead tip planarity of the J-leaded plastic chip carriers is the most important factor in obtaining acceptable process yields. Lead position, lead finish, solder paste composition, and PWB solderability affect process yield as well.

Experiments in which lead tip planarity was confined to specific limits between 1 to 7 mils indicate that a 2 mil planarity requirement produces acceptable results with the process currently in use. Little gain in yield was noted at a 1 mil planarity requirement.

Another interesting result showed that silver in the process, either as a lead finish or in the solder paste, improves yields significantly. One explanation may have to do with the dynamics of the solder during the reflow process as they are affected by the different surface forces acting in the silver and non-silver process.

## Design

The design of the PWB, in addition to providing the component interconnections, will provide the proper amount and correct placement of solder paste for a strong fillet formation. The wave soldering process, by comparison, provides a semi-infinite amount of solder, whereas the SMT process will provide only a predetermined amount. Thus, the component connection pad must be correctly placed and be of the proper size.

Further, consideration must be given for inspection, testing, and rework. The density achievable can lead to severe problems at these points if understanding and due care are not exercised in the design. The project team should include members from manufacturing, testing, QA, and purchasing, in addition to the design engineers, from the start. The design and processing of test boards is strongly recommended to provide experience and direction for the major project.

A very practical set of design guidelines is given in Figure 3. These have been used on a number of SMT designs and have given good results. With proper manufacturing techniques as described later, a high yield can be achieved. Component spacings should be approximately equal to the height of the tallest component. This allows an angle of 45 degrees for visual inspection of test probes.

Figure 4 shows the standard footprint for all Small Outline (SO) packages. The larger and more important fillet of an SO package is on the inside of the gull-wing lead. The solder pad, or land, should therefore be designed to extend slightly under the body of the package in order to optimize this fillet. From Table 1 we can see all packages have 50 mil centers with 25 mil spacings between lands. This allows the designer enough space to put traces between pads, and also reduces the occurrence of solder bridging of adjacent lands. Table 1 also summarizes the suggested land lengths and placement, depending on the terminal count of the SO. While not an absolute solution, these land sizes offer a conservative design solution that will meet most vendors' specifications and provide a mechanically and electrically sound solder joint.

| | |
|---|---|
| ● Geometries | |
| • Trace Width/Space | 8/8 MIL Min., 10/10 MIL Typ. |
| • IC Lead Solder Pad Size | 25 ± 5 MIL × 70 ± 10 MIL |
| • Via Hole Size | 20 MIL DIA |
| • Via Pad Size | 40 MIL DIA |
| • Cap/Resistor Pad Size | W = MAX Dimensions of Component<br>L = 20 MIL Beyond Metallization<br>10 MIL Inside Metallization |
| • Solder Mask | 5 MIL Larger than IC/Component Pad |

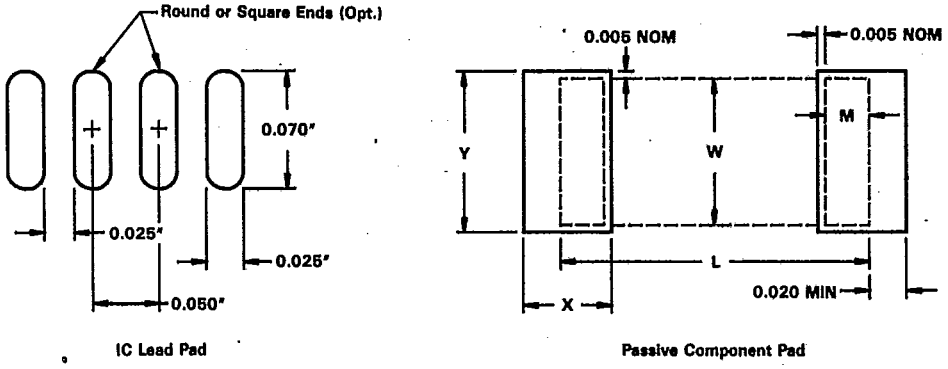



Figure 3. PWB Design Guidelines

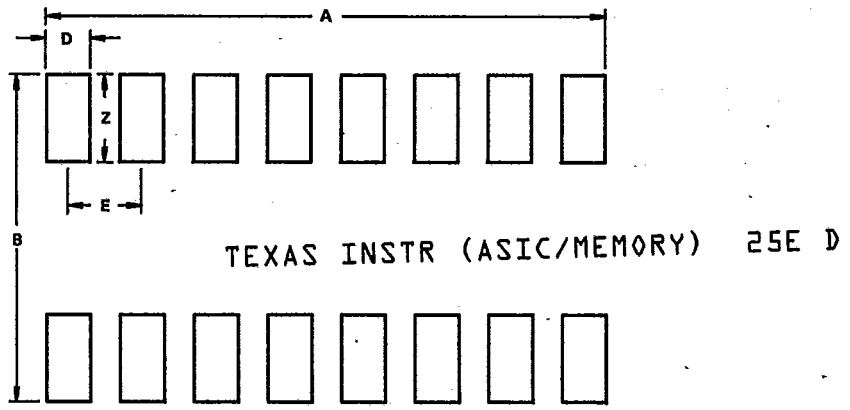



Figure 4. Standard SOIC Footprint

Table 1. SOIC Footprint Dimensions

| No. of Terminals | A | B | Z | D | E |
|---|---|---|---|---|---|
| 8 | .175 | .250 | .050 | .025 | .050 |
| 14 | .325 | .250 | .050 | .025 | .050 |
| 16 | .375 | .250 | .050 | .025 | .050 |
| 20 | .475 | .430 | .070 | .025 | .050 |
| 24 | .575 | .430 | .070 | .025 | .050 |



| Test | 4164A PLCC | 4164 DIP | Units |
|---|---|---|---|
| Life Test, 125°C | 42 | 64 | Fits*—60% UCL |
| 85°C/85% RH | 0.17 | 0.37 | %/1000 Hours |
| Autoclave | 0.17 | 0.96 | %/240 Hours |
| T/C—65/150 | 0.52 | 1.44 | %/1000 Cycles |
| T/C 0/125 | 0.0 | 0.0 | %/2000 Cycles |

*Derated to 55°C Assuming 0.5EV Activation Energy

Figure 5. Failure Rate Comparison 4164A PLCC VS DIP



## Manufacturing

The SMT manufacturing area must have the following basic equipment:

- Solder Paste Printer
- Component Pick and Place Machine
- Solder Paste Reflow Machine
- Clean-up System
- Inspection/Process Control Aids
- Electrical Test

The criteria for choosing the above is determined mainly by the size(s) and quantity of PWBs per month, the gross number of components per PWB, and the number of different components per PWB.

The size of the largest PWB is an important criterion in the choice of all of the major items. The printer, pick and place, reflow, and clean-up must all be able to handle it with no difficulty or process nonuniformity. The number and size of the various PWBs that may be produced will secondarily be considered for ease of set up and changeover in the printer and pick and place. The pick and place machine(s) will probably be the most expensive item in the list above and therefore, should get the most attention.

The gross number of components and PWBs will provide data for choosing the pick and place. Component per hour placement speed should be checked in actual operation, as the interrelationship may affect ultimate speed. The number of different components per board will determine how many feeders and what types of feeders will be required. This is a very key issue, as well as the accuracy of placement.

## Reflow

The solder reflow is easily achieved with any of the commercially available equipment. Subtle differences between vapor phase, either batch or in-line, and infrared are overshadowed by the choice of solder paste and the solderability/planarity issue. A batch vapor phase is extremely flexible for different sizes of boards with different component counts. The in-line vapor phase is a good choice for a more automated processing line with standard or similar sized boards. The infrared has the advantage of being less expensive to operate, but requires more alteration to set up the time-temperature profile for a different size PWB. This would be a minimal problem on a manufacturing line building high volumes of the same board.

## Clean-up

The most popular flux for SMT is the mildly activated rosin flux (RMA). This was developed in the days of vacuum tube assembly when clean-up was next to impossible. It is noncorrosive but provides sufficient fluxing action for good quality components and PWBs. Thus it is the preferred choice for SMAs with small spacings under most passives and SOICs, where complete cleaning is difficult. A mild solvent, such as Freon TMS, is generally sufficient to achieve a good visual cleanup, and there are several systems available that provide hot vapor, spray, or ultrasonic de-fluxing.

## Reliability

With the smaller surface mount packages, there is some concern about component reliability. Texas Instruments addressed the overall DRAM reliability issue several years ago. Through an extensive task force effort, the major problems of the life test, humidity performance, and temperature cycle were identified. The best solutions to these problems required several changes in the design and process of the silicon chip. In doing so, the reliability of the DRAM chip became independent of the package used. Thus, the 64K DRAM in the plastic chip carrier package performs equivalently to the same chip in a DIP as shown in Figure 5. Similar data is available on most semiconductor ICs.

An additional reliability concern originates in the surface mount solder reflow process, which submits components to higher reflow temperatures more suddenly than the wave-soldering methods of DIP components, with oftentimes repeated reflow cycles for rework and repair.

The best method for resolving this issue involves comparing the temperature-time differential of the vapor phase or infrared solder reflow process to the standard temperature

cycling reliability tests to which surface mount components are routinely submitted. Figures 6 and 7 show temperature profiles of the vapor phase and infrared solder reflow processes. In the vapor phase process, the maximum temperature change with time is:

$$\frac{215°C - 25°C}{45 \text{ sec}} = \frac{190°C}{45 \text{ sec}}$$

equaling approximately 4°C/sec. The infrared solder reflow method submits the ICs to a similar, yet less severe temperature over time change of 3°C/second. Comparing these temperature profile ramp-ups to that which a surface mount component undergoes in a temperature cycling reliability test proves that there should be no concern over damage to the component during reflow. In the temp cycling test, the surface mount components were submitted to 1000 cycles of sudden cycling from 150°C to −65°C within three seconds. This represents a temperature-time differential of:

$$\frac{150°C-(-65°C)}{3} = \frac{215°C}{3 \text{ sec}} = \frac{70°C}{\text{sec}}$$

with less than 0.5 percent failures.

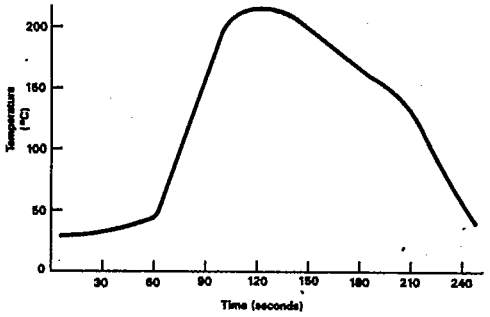



**Figure 6. Typical Temperature Profile for In-Line Vapor Phase Reflow**

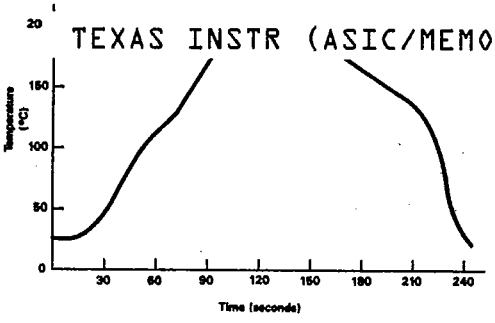



**Figure 7. Typical IR Reflow System Profile**

Since the surface mounted components were able to withstand a 70°C/second temperature change of 1000 cycles, they should be able to withstand the less severe conditions of a 4°C/second damage during reflow without reliability degradation.

Another concern in the solder reflow processing of surface mount components is the dwell time in reflow temperatures of 215°C or above. The dwell time for a small PWB populated with surface mount devices is about 20 seconds. For a larger board of about 10"×12" up to 50 seconds is needed for reflow. A generalized component degradation curve, relating accumulated time and temperature, can be assumed to exist. The shape of the curve for this discussion is assumed to be a decaying parabolic for simplicity and conservatism. There are two generally known points of this curve. The flame retardant mold compound (FRMC) of a plastic package starts to break down at 300°C in two to three seconds. Also, the molding and curing of a surface mount device is performed over several hours at 175°C. These two points are shown on the generalized curve shown in Figure 8, with the "safe" region being the area under the curve. Two points that fall within this region are the industry standard practice of solder dipping leads of several types of ICs, and of the soldering plastic devices on the bottom with Type III surface mount assembly, each submerges the component for three to four seconds in a solder wave.

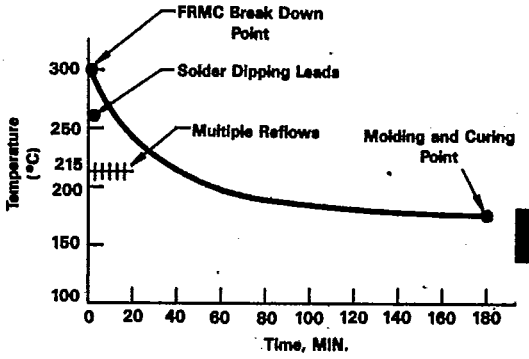



**Figure 8. General Plastic Degradation Curve**



## Summary

Surface mount assembly techniques provide a significant advantage in cost, volume, and reliability over the current "thru-hole" technology. These are well documented, and the manufacturing equipment and related products are becoming readily available to support new production lines. Also, as experience grows, improved products and ideas are developed from the cooperative efforts of vendors and users in standardization organizations and in problem-solving sessions. The broad selection of package types and product technologies available now are sufficient to begin conversion of existing electronic system products for size reduction or feature enhancement. Definitely, new products should be designed with surface mount technology.