

FEATURES

Reflective, 50 Ω design

Low insertion loss: 0.7 dB typical to 2.0 GHz

High power handling at $T_{CASE} = 105^{\circ}\text{C}$

Long-term (>10 years) average

CW power: 43 dBm

Peak power: 49 dBm

LTE average power (8 dB PAR): 41 dBm

Single event (<10 sec) average

LTE average power (8 dB PAR): 44 dBm

High linearity

P0.1dB: 47 dBm typical

IP3: 70 dBm typical

ESD ratings

HBM: 4 kV, Class 3A

CDM: 1.25 kV

Single positive supply: 5 V

Positive control, CMOS/TTL compatible

32-lead, 5 mm \times 5 mm LFCSP package

APPLICATIONS

Wireless infrastructure

Military and high reliability applications

Test equipment

Pin diode replacement

GENERAL DESCRIPTION

The ADRF5160 is a silicon-based, high power, 0.7 GHz to 4.0 GHz, silicon, single-pole, double-throw (SPDT) reflective switch in a leadless, surface-mount package. The switch is ideal for high power and cellular infrastructure applications, such as long-term evolution (LTE) base stations. The ADRF5160 has high power handling of 41 dBm (8 dB PAR LTE, long-term (>10 years) average typical), a low insertion loss of 0.7 dB typical

to 2.0 GHz, an input third-order intercept (IP3) of 70 dBm (typical), and a 0.1 dB compression point (P0.1dB) of 47 dBm. On-chip circuitry operates at a single positive supply voltage of 5 V at a typical supply current of 1.1 mA, making the ADRF5160 an ideal alternative to pin diode-based switches.

The ADRF5160 comes in an RoHS compliant, compact, 32-lead, 5 mm \times 5 mm LFCSP.

FUNCTIONAL BLOCK DIAGRAM

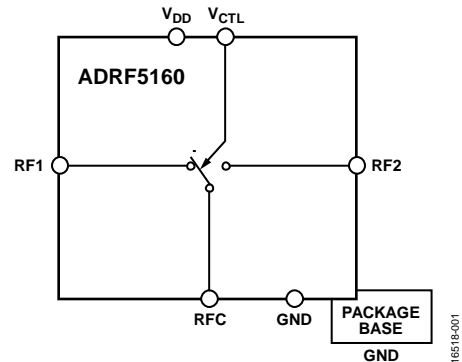


Figure 1.

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REVISION HISTORY

5/2018—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 5\text{ V}$, $V_{CTL} = 0\text{ V}/V_{DD}$, $T_A = 25^\circ\text{C}$, and the device is a $50\ \Omega$ system, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit		
FREQUENCY RANGE		0.7		4.0	GHz		
INSERTION LOSS	0.7 GHz to 2.0 GHz		0.7		dB		
	2.0 GHz to 3.5 GHz		0.8	1.0 ¹	dB		
	3.5 GHz to 4.0 GHz		0.9		dB		
ISOLATION	RFC to RF1 and RF2 (Worst Case)	0.7 GHz to 2.0 GHz	53		dB		
		2.0 GHz to 4.0 GHz	45		dB		
	RF1 to RF2	0.7 GHz to 2.0 GHz	51		dB		
		2.0 GHz to 4.0 GHz	35		dB		
RETURN LOSS	RFC	0.7 GHz to 2.0 GHz	20		dB		
		2.0 GHz to 4.0 GHz	19		dB		
	RF1 and RF2 (On State)	0.7 GHz to 2.0 GHz	19		dB		
		2.0 GHz to 4.0 GHz	18		dB		
SWITCHING CHARACTERISTICS	10%/90% radio frequency output (RF _{OUT}) 50% V _{CTL} to 10%/90% RF _{OUT}	Rise and Fall Time (t _{RISE} , t _{FALL})	0.27		μs		
		On and Off Time (t _{ON} , t _{OFF})	1.2		μs		
INPUT LINEARITY	Two-tone input power = 30 dBm per tone at 1 MHz tone spacing 0.7 GHz to 2.0 GHz 2.0 GHz to 4.0 GHz	0.1 dB Compression (P _{0.1dB})	47		dBm		
		Third-Order Intercept (IP3)	0.7 GHz to 2.0 GHz	72		dBm	
			2.0 GHz to 4.0 GHz	70		dBm	
SUPPLY CURRENT			1.1		mA		
DIGITAL CONTROL INPUT	$V_{DD} = 4.5\text{ V to }5.4\text{ V}$, $T_{CASE} = -40^\circ\text{C to }+105^\circ\text{C}$	Low Voltage	0	0.8	V		
		High Voltage	1.3	5	V		
		Low and High Current		<1		μA	
RECOMMENDED OPERATING CONDITIONS	Supply Voltage Range (V _{DD})	4.5		5.4	V		
		Control Voltage Range (V _{CTL})	0		V _{DD}	V	
	RF Input Power	Case Temperature (T _{CASE}) = 105°C ²	Continuous wave (CW)	8 dB peak average ratio (PAR) LTE, long-term (>10 years) average	43	dBm	
				8 dB PAR LTE, single event (<10 sec) average	44	dBm	
				CW	45	dBm	
			T _{CASE} = 85°C	8 dB PAR LTE, long-term (>10 years) average	8 dB PAR LTE, single event (<10 sec) average	41	dBm
					CW	44	dBm
					47.5	dBm	
			T _{CASE} = 25°C	8 dB PAR LTE, long-term (>10 years) average	8 dB PAR LTE, single event (<10 sec) average	41	dBm
					CW	44	dBm
					49	dBm	
			T _{CASE} = -40°C	8 dB PAR LTE, long-term (>10 years) average	8 dB PAR LTE, single event (<10 sec) average	41	dBm
					CW	44	dBm
					49	dBm	
T _{CASE} Range		-40		+105	°C		

¹ Guaranteed by design for device to device and over operating temperature variation.

² Peak power is 49 dBm, which corresponds to a PAR of 8 dB at LTE long-term.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage Range (V_{DD})	-0.3 V to +5.4 V
Control Voltage Range (V_{CTL})	-0.3 V to $V_{DD} + 0.3$ V
RF Input Power ¹	49.7 dBm
Channel Temperature	135°C
Maximum Peak Reflow Temperature (Moisture Sensitivity Level 3 (MSL3)) ²	260°C
Storage Temperature Range	-65°C to +150°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	4 kV (Class 3A)
Charged Device Model (CDM)	1.25 kV

¹ For the recommended operating conditions, see Table 1.

² See the Ordering Guide for additional information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 3. Thermal Resistance

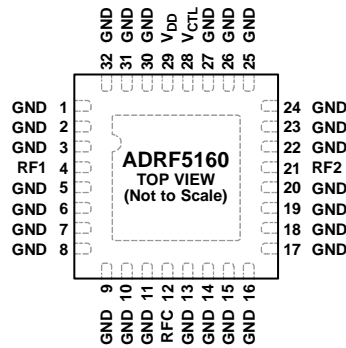
Package Type	θ_{JC}	Unit
HCP-32-1	8.4	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. EXPOSED PAD. EXPOSED PAD MUST BE CONNECTED TO RF/DC GROUND.

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 3, 5 to 11, 13 to 20, 22 to 27, 30 to 32	GND	Ground. The package bottom has an exposed metal pad that must connect to the PCB RF/dc ground.
4	RF1	RF Port 1. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin. See Figure 3 for the interface schematic.
12	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin. See Figure 3 for the interface schematic.
21	RF2	RF Port 2. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin. See Figure 3 for the interface schematic.
28	V _{CTL}	Control Input Pin. See Figure 4 for the V _{CTL} interface schematic. Refer to Table 5 for the signal path and the recommended input control voltage range shown in Table 1.
29	V _{DD} EPAD	Supply Voltage Pin. Exposed Pad. Exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

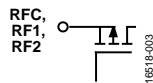


Figure 3. RFC, RF1, and RF2 Interface Schematic

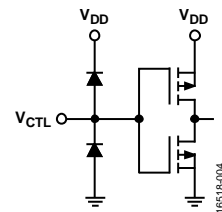


Figure 4. Control Input (V_{CTL}) Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

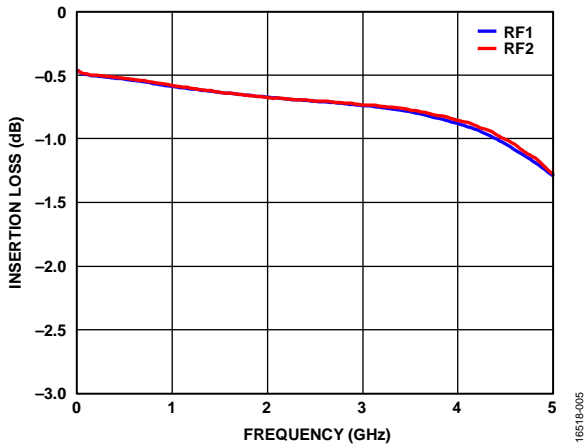


Figure 5. Insertion Loss for RF1 and RF2 vs. Frequency at $V_{DD} = 5 V$

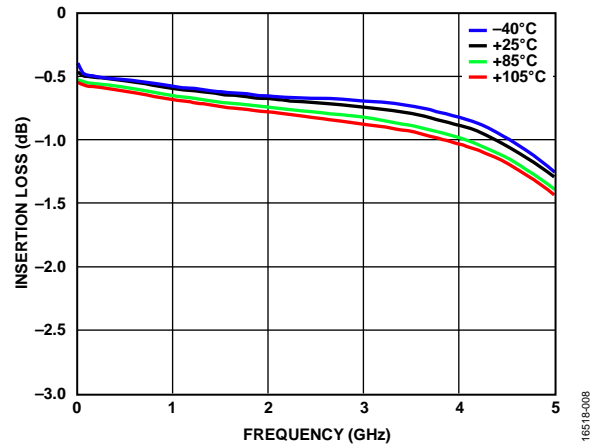


Figure 8. Insertion Loss vs. Frequency for Various Temperatures at $V_{DD} = 5 V$

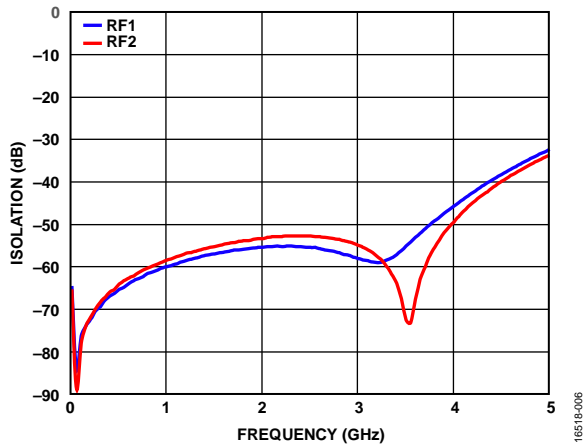


Figure 6. Isolation Between RFC and RF1 and RF2 vs. Frequency at $V_{DD} = 5 V$

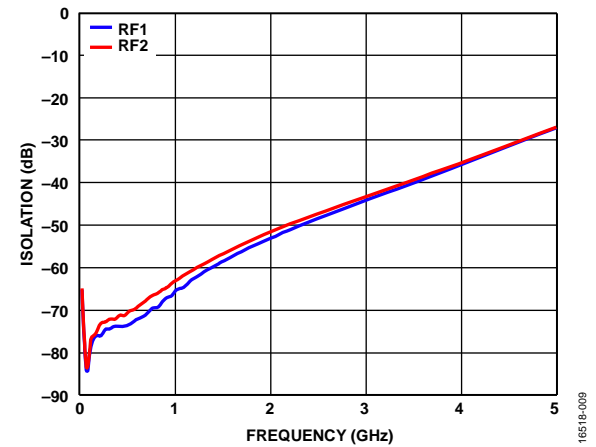


Figure 9. Isolation Between RF1 and RF2 vs. Frequency at $V_{DD} = 5 V$

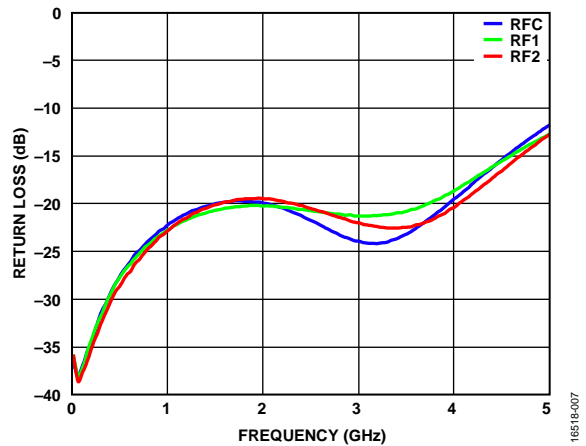


Figure 7. Return Loss vs. Frequency at $V_{DD} = 5 V$

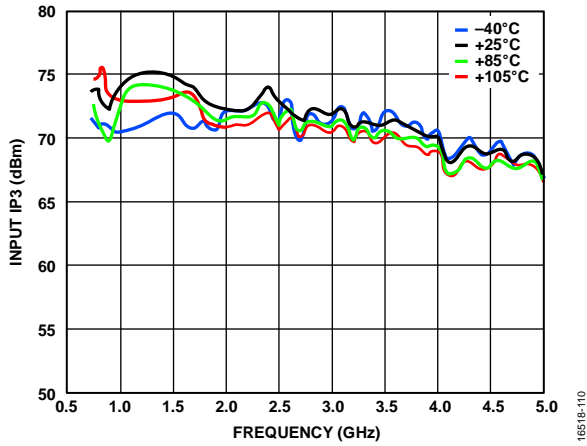


Figure 10. Input Third-Order Intercept (IP3) vs. Frequency for Various Temperatures, $V_{DD} = 5 V$

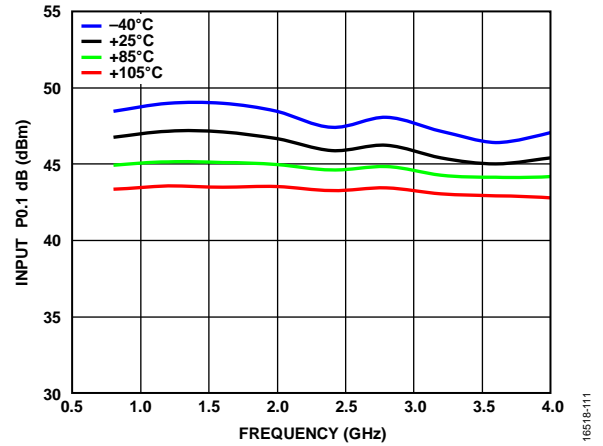


Figure 12. Input 0.1dB Compression ($P_{0.1 dB}$) vs. Frequency for Various Temperatures, $V_{DD} = 5 V$

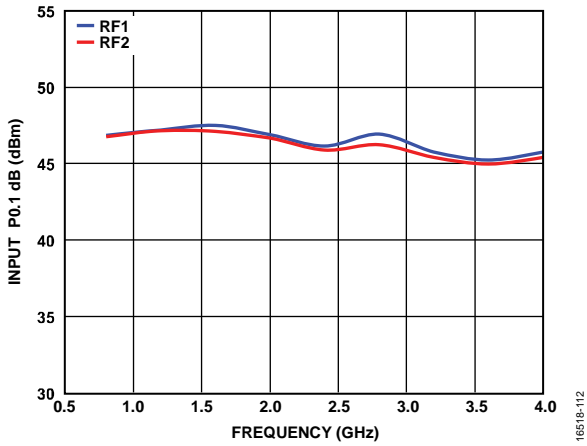


Figure 11. Input 0.1dB Power Compression ($P_{0.1 dB}$) vs. Frequency, $V_{DD} = 5 V$

THEORY OF OPERATION

The ADRF5160 requires a single-supply voltage applied to the V_{DD} pin. Bypassing capacitors are recommended on the supply line to minimize RF coupling.

The ADRF5160 is controlled via a digital control voltage applied to the V_{CTL} pin. A bypassing capacitor is recommended on this digital signal line to improve the RF signal isolation.

The ADRF5160 is internally matched to $50\ \Omega$ at the RF input port (RFC) and the RF output ports (RF1 and RF2). Therefore, no external matching components are required. The RFx pins are dc-coupled, and dc blocking capacitors are required on the RFx lines. The design is bidirectional, meaning that the input and outputs are interchangeable.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up V_{DD} .
3. Power up the digital control input. Power the digital control input before the V_{DD} supply to avoid inadvertently forward biasing and damaging the ESD protection structures.
4. Power up the RF input.

Depending on the logic level applied to the V_{CTL} pin, one RF output port (for example, RF1) is set to on mode, by which an insertion loss path is provided from the input to the output. While the other RF output port (for example, RF2) is set to off mode, by which the output is isolated from the input.

Table 5. Switch Operation Mode

Digital Control Input (V_{CTL})	Signal Path	
	RF1 to RFC	RF2 to RFC
Low	Isolation (off)	Insertion loss (on)
High	Insertion loss (on)	Isolation (off)

APPLICATIONS INFORMATION

EVALUATION BOARD

The [ADRF5160-EVALZ](#) can withstand high power levels and temperatures at which the device operates.

The [ADRF5160-EVALZ](#) evaluation board is constructed with eight metal layers and dielectrics between each layer, as shown in Figure 13. Each metal layer has a 1 oz (1.3 mil) copper thickness, and the external layers are plated to 2 oz.

The top dielectric material is 10 mil Rogers RO4350, which exhibits a low thermal coefficient, offering control over thermal rise of the board. The dielectrics between other metal layers are FR4. The overall board thickness is 62 mil.

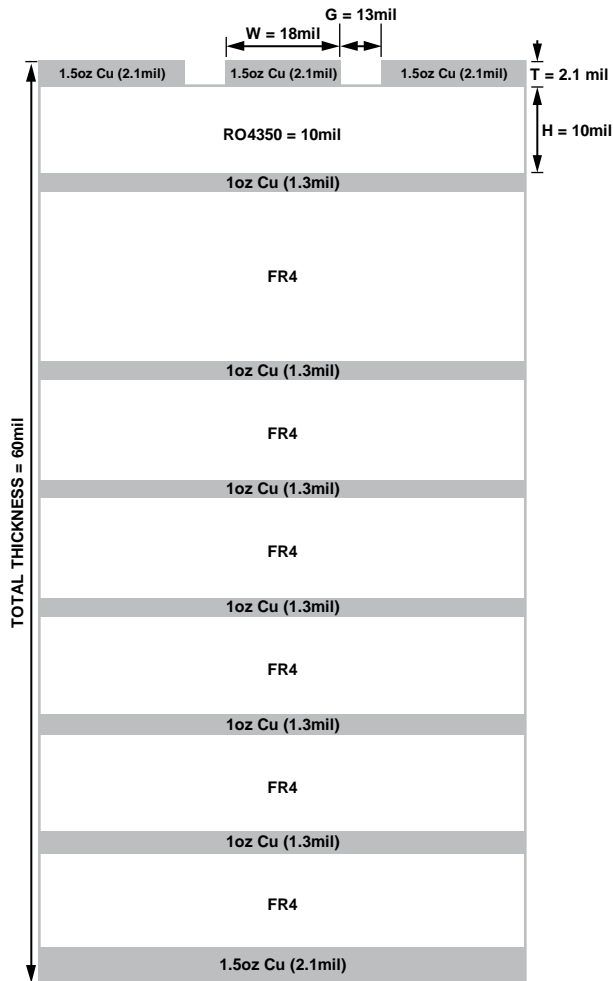


Figure 13. [ADRF5160-EVALZ](#) Evaluation Board Cross Sectional View

The top copper layer has all RF and dc traces. The other seven layers provide sufficient ground and help handle the thermal rise on the [ADRF5160-EVALZ](#). In addition, via holes are provided around transmission lines and under the exposed pad of package, as shown in Figure 15, for proper thermal grounding. RF transmission lines on the board are of a coplanar wave guide design with a width of 18 mils and ground spacing of 13 mils.

To ensure maximum heat dissipation and to reduce thermal rise on the board, some application considerations are essential. The evaluation board must be attached to a copper support plate at the bottom of the board. The [ADRF5160-EVALZ](#) comes with this support plate attachment. Attach this evaluation board with its support plate to a heat sink using thermal grease during all high power operations. Figure 14 shows the board temperature vs. the RF power input tested with the preceding conditions and precautions (the evaluation board and support plate are attached to a heat sink). The temperature rise is less than 8°C up to 48 dBm of RF power input, which provides the required thermal dissipation when operating at high power levels.

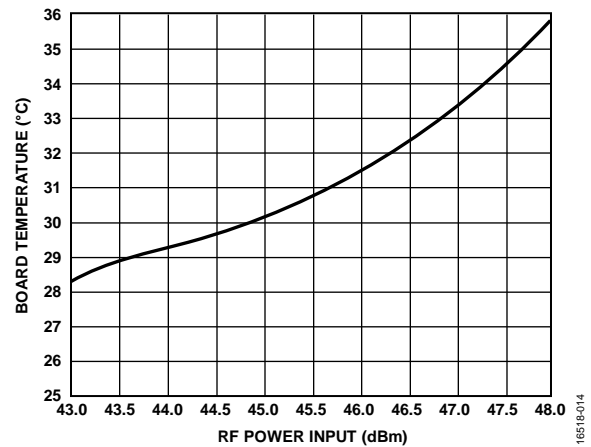


Figure 14. [ADRF5160-EVALZ](#) Evaluation Board Temperature Rise (Oven Temperature Set to 25°C)

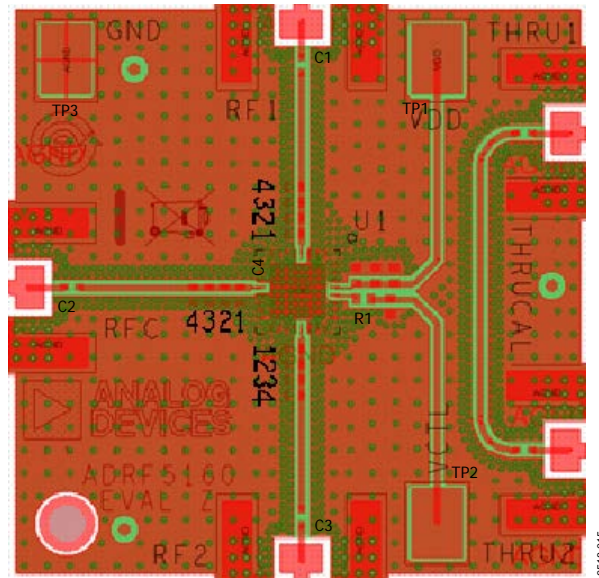


Figure 15. [ADRF5160-EVALZ](#) Evaluation Board Layout

TYPICAL APPLICATION CIRCUIT

Generate the evaluation PCB used in the typical application circuit shown in Figure 17 with proper RF circuit design techniques. Signal lines at the RF port must have a 50 Ω

impedance, and the package ground leads and backside ground slug must connect directly to the ground plane. The evaluation board shown in Figure 16 is available from Analog Devices, Inc., upon request.

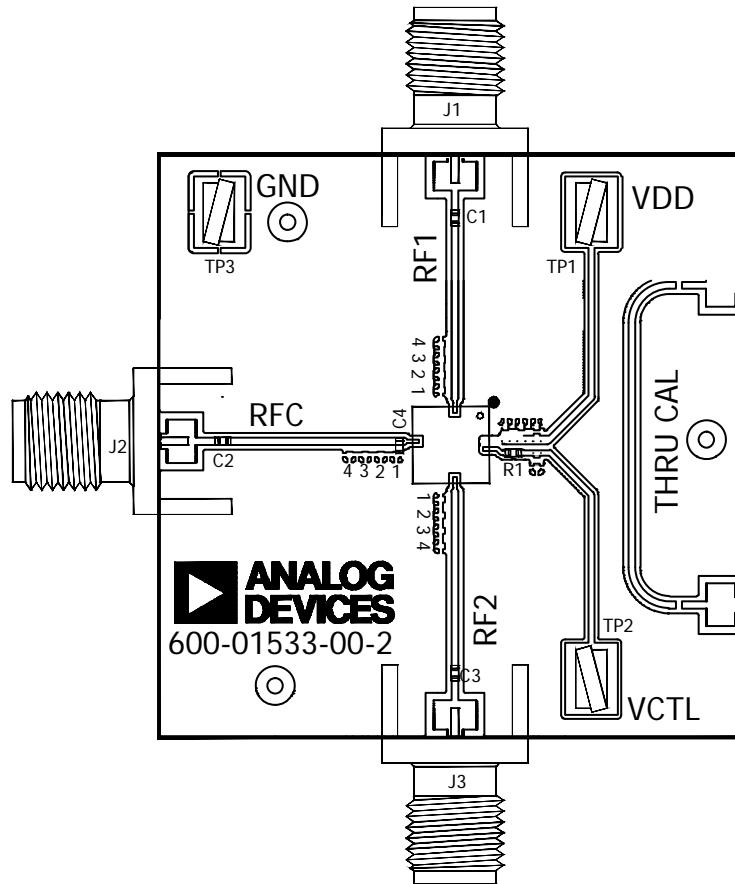


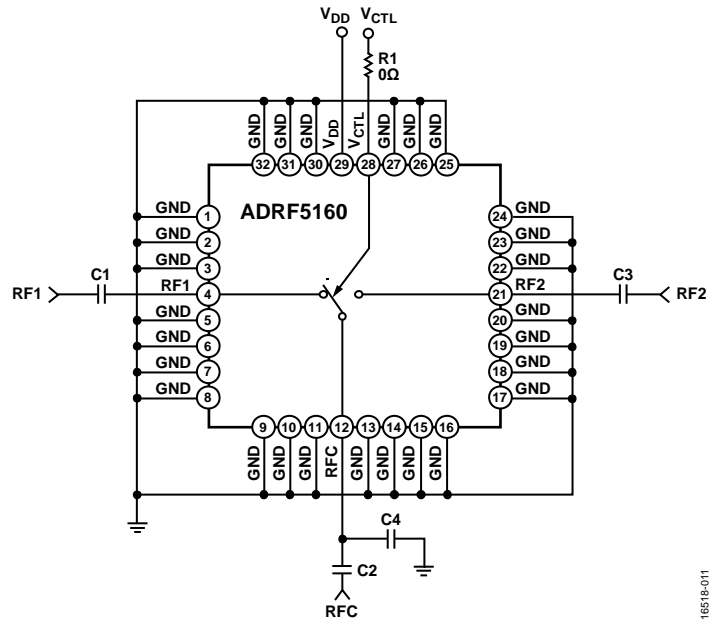
Figure 16. ADRF5160-EVALZ Evaluation Board Component Placement

Table 6. Bill of Materials for the ADRF5160-EVALZ Evaluation Board

Reference Designator	Description
C1 to C3	24 pF, 200 V ultralow, effective series resistance (ESR) capacitors, 0402 package
C4	0.3 pF, 200 V ultralow ESR capacitor, 0402 package
TP1, TP2, TP3	Test point connectors
R1	0 Ω resistor, 0402 package
J1, J2, J3	PCB mount, SubMiniature Version A (SMA) connectors
U1	ADRF5160 SPDT switch
PCB ¹	ADRF5160-EVALZ ² evaluation PCB

¹ The circuit board material is Roger 4350 or Arlon 25FR.

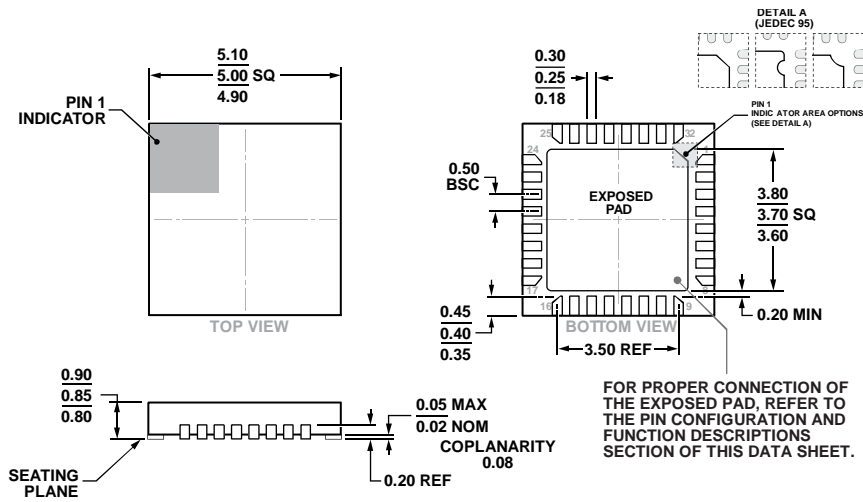
² Reference to this evaluation board number when ordering the complete evaluation board.



16518-011

Figure 17. Typical Application Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-4.

Figure 18. 32-Lead Lead Frame Chip Scale Package [LFCSPP]
 5 mm x 5 mm Body and 0.85 mm Package Height
 (HCP-32-1)
 Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	MSL Rating ²	Package Description	Package Option
ADRF5160BCPZ	-40°C to +105°C	MSL3	32-lead Lead Frame Chip Scale Package [LFCSPP]	HCP-32-1
ADRF5160BCPZ-R7	-40°C to +105°C	MSL3	32-lead Lead Frame Chip Scale Package [LFCSPP]	HCP-32-1
ADRF5160-EVALZ			Evaluation Board	

¹ Z = RoHS Compliant Part.

² See the Absolute Maximum Ratings section for additional information.