High Speed CMOS 9-bit Clocked FIFO

2Kx9: QS7223
4Kx9: QS7224

FEATURES/BENEFITS

- Clocked interface FIFOs for high speed systems
- Data and flags change on rising edge of clocks
- Fully independent Read and Write operation
- TTL input and output level compatible
- Dual Port RAM-based cell using 6T technology
- 66 MHz cycle time with symmetrical clocks
- Depth expansion without additional logic or pins
- Register-like: outputs show current word in FIFO
- Clock noise filters, low ground bounce design
- Available in 28-pin 300 mil PDIP, SOJ, 32-PLCC

DESCRIPTION

The QS7223 and QS7224 are 2Kx9 and 4Kx9 FIFOs respectively with clocked interfaces for both read and write. These interfaces provide high speed data buffering in system designs and allow symmetrical clocks at speeds to 66 mHz. Free running independent read and write clocks are controlled by read and write enable lines. All signals are relative to the rising edges of the clocks. Write enable and write data are accepted at the rising edge and the full flag and the half full flag change after the rising edge of the write clock. Read enable is accepted at the rising edge and read data and the empty flag changes after the rising edge of the read clock. These FIFOs use a dual-port RAM based architecture and have independent read and write pointers. The read and write pointers are set to zero by the reset pulse. A Write Enable causes data to be written and the write pointer to be incremented by the rising edge of the write clock. If the FIFO was empty, the write data will be present at the read outputs, and the empty flag will be cleared at the next rising edge of the read clock. A Read Enable will cause the read pointer to be incremented to the next word on the rising edge of the read clock. If there was only one word in the FIFO, the empty flag will be set by this same rising edge. HF and FF flags are after the rising edge of the write clock. The EF and FF flags prevent the FIFO from being written into when full or being read from when empty.

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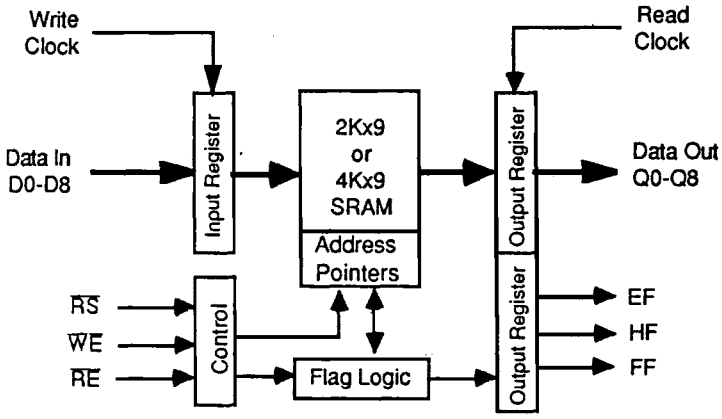
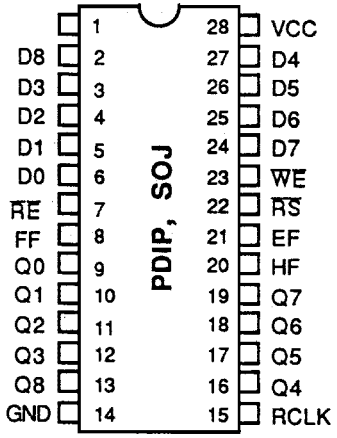
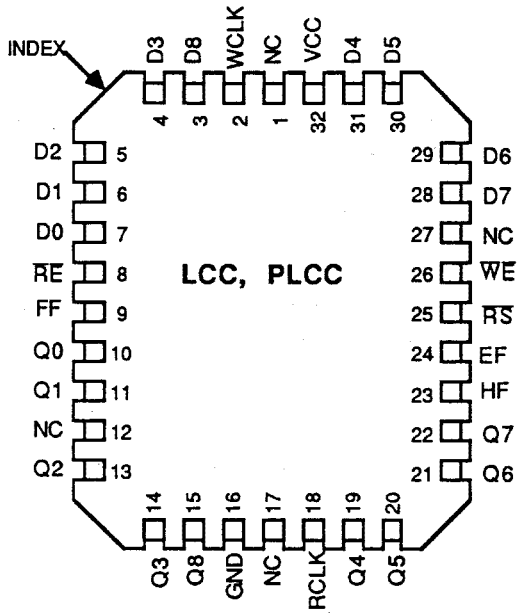
FUNCTIONAL BLOCK DIAGRAM



PINOUTS





ALL PINS TOP VIEW

PIN DESCRIPTIONS

Name	I/O	Description
Di	I	Data Inputs
Qi	O	Data Outputs
RCLK	I	Read Clock: synchronizes data and EF outputs
$\overline{RE}$	I	Read Enable: causes the read pointer to increment
WCLK	I	Write Clock: synchronizes WE and Di inputs, HF and FF outputs.
$\overline{WE}$	I	Write Enable: causes the write pointer to increment.
$\overline{RS}$	I	Reset: causes both read and write pointers to set to location 0.
EF	O	Empty Flag: indicates a empty condition. Generated by RCLK.
FF	O	Full Flag: indicates a full condition. Generated by WCLK.
HF	O	Half Full Flag: indicates a half-full condition. Generated by WCLK.
NC	-	No Connect: these pins should not be biased

FUNCTION TABLE

MOD	Input					Internal		Outputs (After			
	$\overline{RS}$	$\overline{WE}$	WC	$\overline{RE}$	RC	Write Pointe	Read Pointe	EF	FF	HF	QI
Read/Write Controls											
Reset	L	X	X	X	X	0000	0000	H	L	L	Q(0)
Write	H	L	↑	X	X	YY+1	XX	H	(3)	(3)	Q(XX)
Read	H	X	X	L	↑	YY	XX+1	(3)	L	(3)	Q(XX+1)
Hold	H	H	↑	H	↑	YY	XX	(3)	(3)	(3)	Q(XX)
Read/Write at Empty											
1st Write	H	L	↑	H	X	0001	0000	(5)	L	L	Q(0), (8)
2nd Write	H	L	↑	H	X	0002	0000	L	L	L	Q(0)
1st Read	H	H	X	L	↑	0002	0001	L	L	L	Q(1)
2nd Read	H	H	X	L	↑	0002	0002	H	L	L	Q(2)
Read/Write at Full (4)											
Last Write	H	L	↑	H	X	1000	0000	L	H	H	Q(0)
1st Read @ Full	H	H	X	L	↑	1000	0001	L	(6)	H	Q(1)
Read/Write at Half Full (4)											
2049th Write	H	L	↑	X	X	0800	0000	L	L	L	Q(0)
2049th+1 Write	H	L	↑	X	X	0801	0000	L	L	H	Q(0)
2nd Read @ HF	H	H	X	L	↑	0801	0001	L	L	(7)	Q(1)

Notes:
(1) The Read Pointer will not increment if the FIFO is empty.
(2) The Write pointer will not increment if the FIFO is full.
(3) The flags will reflect the relative locations of the read and write pointers.
(4) The hexidecimal addresses used in this example are for the QS7224 (4kx9)
(5) A EF transition (HItoLOW) will only happen after a read clock.
(6) A FF transition (HItoLOW) will only happen after a write clock.
(7) A HF transition (HItoLOW) will only happen after a write clock.
(8) A valid data transition will only happen after a read clock.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....-0.5V to +7.0V
DC Output Voltage V_O ..... -0.5V to V_{CC} + 0.5V
DC Input Voltage V_I ..... -0.5V to V_{CC} + 0.5V
AC Input Voltage (for pulse width≤20 ns)..... -3.0V
DC Input Diode Current with V_I<0..... -20 mA
DC Input Diode Current with V_I >V_{CC}..... 20 mA
DC Output Diode Current with V_O <0..... -50 mA
DC Output Diode Current with V_O >V_{CC} ..... 50 mA
DC Output Current Max. sink current/pin..... 70 mA
DC Output Current Max. source current/pin..... 30 mA
Total DC Ground Current..... (NxIOL +MxΔI CC) mA
Total DC VCC Power Supply Current..... (NxIOH + MxΔI CC) mA
N=Number of Outputs, M=Number of inputs
Maximum Power Dissipation.....0.5 watts
TSTG Storage Temperature..... -65° to +165°C
ESD..... >2001 V

CAPACITANCE

Ta = 25°C, f = 1 MHz

Name	Description	Conditions	Typ	Max	Units
Cin	Input Capacitance	Vin = 0 V	5	8	pF

Note: Capacitance is guaranteed but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±10% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.0	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -2 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
|Iil|	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	µA

Notes:
1. Transient inputs with Vil not more negative than -1.5 volts are permitted for pulse widths ≤ 10 ns

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POWER SUPPLY CHARACTERISTICS

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±10% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%
Icc is tested at 30 MHz only. Other speeds not guaranteed.

Symbol	Parameter		Typ	Max	Unit
Icc1	Operating OperatingCurrent Vcc = MAX, Outputs open $\overline{RE}$ = $\overline{WE}$ = Vil	Com	60	120	mA
		Mil	70	140	
Icc2	Standby Current $\overline{RE}$ = $\overline{WE}$ = $\overline{RS}$ = Vcc-0.2 clock free running	Com	6	15	
		Mil	12	20	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

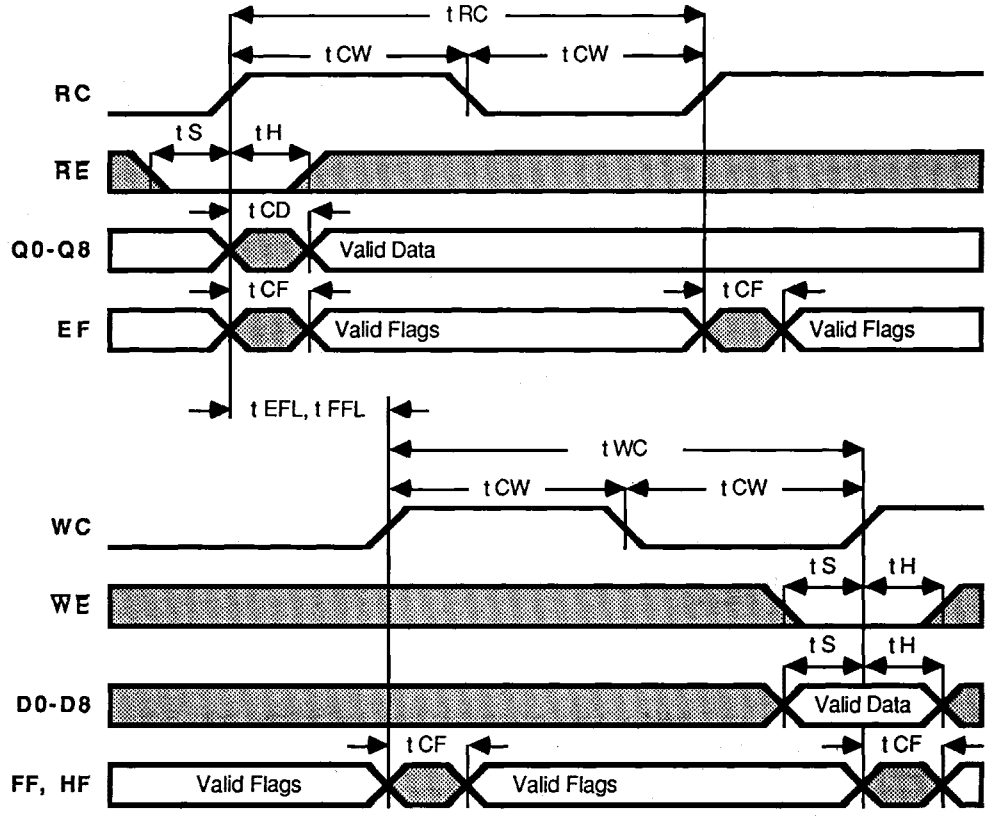
V_{CC}=5V±10%, Commercial T_A=0°C to +70°C, Military T_A=-55°C to +125°C

Symbol	Parameter	Note	-15	-20	-25	-30	-40	Unit	Type
f RC, f WC	Read or Write Clock, mHz	2	66	50	40	33	25	MHz	Min
t RC, t WC	Read or Write Cycle Time		15	20	25	30	40	ns	
t CW	Read or Write Clock High or Low	1	7	8	10	12	15		
t S	Enable, Write Data Setup Time		5	5	6	6	7		
t H	Enable, Write Data Hold Time		0	0	0	0	0		
t CF	Clock to Flag Output Delay		7	8	9	10	12		Max
t CD	Clock to Data Output Delay		9	10	11	13	15		
t RS	Reset Pulse Width	1	8	10	15	20	25		Min
t RSR	Reset Recovery Time	3	7	8	10	10	10		
t RF	Reset to Flag Delay		9	10	12	15	17		Max
t EFL, t FFL	Flag Latency, R/W to E/F	4	17	18	20	23	25		

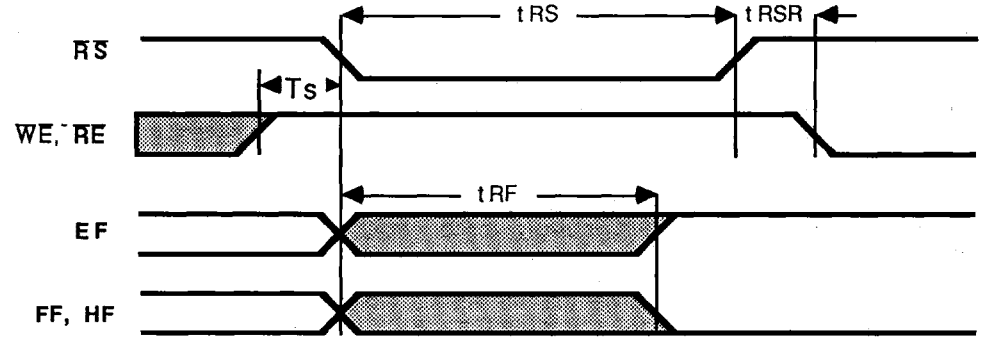
Notes: These timings are measured as defined in AC Test Conditions

1. Pulse widths less than the specified minimum value may upset the internal pointers and are not allowed.
2. These values are guaranteed by design and not tested
3. Minimum time to write clock edge for valid write enable to be accepted.
4. Minimum time from WCLK falling edge to RCLK edge for write to turn off EF on next clock;
   Minimum time from RCLK rising edge to WCLK edge for read to turn off FF on next clock,
   Minimum time from RCLK rising edge to WCLK edge for read to turn off HF on next clock.

TIMING DIAGRAMS



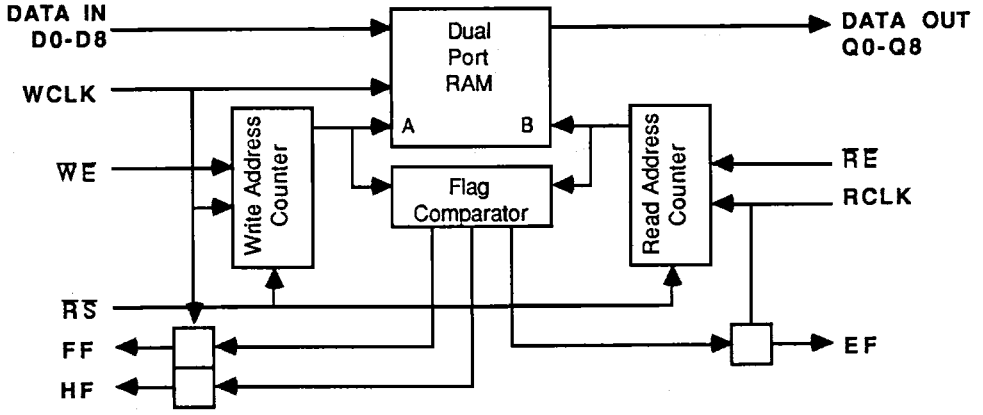
Read and Write Operations



Reset Timing

OPERATIONAL DESCRIPTION

The 7223/4 Clocked FIFO consists of a dual port RAM, read and write address counters, a flag comparator, and synchronizing flip flops for the flags. A simplified block diagram of the 7223/4 Clocked FIFO is shown below. Note that the internal design of the 7223/4 Clocked FIFO is more complex than shown for maximum performance. The simplified block diagram shown is provided for understanding the operation of the FIFO. For detailed timing in formation, refer to the AC Specifications and timing diagrams.



Clocked FIFO Simplified Block Diagram

The dual port RAM is a static RAM with two independent sets of addressing logic. Each set of addressing logic can simultaneously and independently address words in the RAM. Each combination of addressing logic and its associated data I/O is called a port, hence the name dual port RAM. In the FIFO, one port is used only for writing and one port only for reading. If both ports have the same address and data is written by one port, the same data will be read immediately at the other port after a read clock edge. The data is said to flow through the RAM.

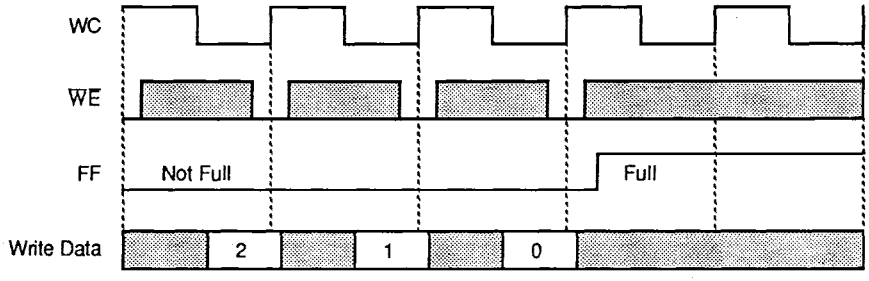
The read and write address counters address the read and write ports of the dual port RAM. Each is a binary counter that increments on the rising edge of the clock, is enabled for counting by a low active enable signal and is asynchronously reset by a reset pulse. They are similar in operation to the 74161 binary counter.

Data is written into the dual port RAM by each write clock. Data is rewritten by each clock until a write enable advances the write address counter. When the write address counter advances, the data written by the last write clock, the one that advances the counter, is the data retained by that RAM word. Data is read continuously by the read port at the address from the read address counter. If the FIFO is empty, data from the write port will flow through to the read port following each write clock pulse and will be output following a read clock pulse. When read enable is active, the read address counter advances to the next word.

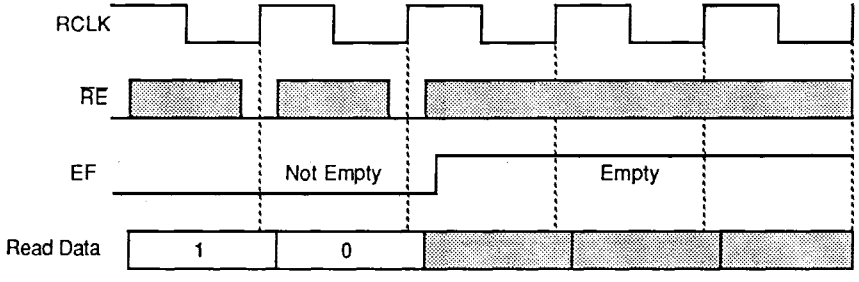
The flag comparator continuously compares the contents of the two address counters. If the contents of the two address counters are equal, the FIFO is empty, and the empty flag is active. This is the case immediately after a reset pulse when both counters have been reset to zero. If the write address counter value is equal to the read address counter value plus the depth of the RAM (e.g., 4096 for a 4Kx9 FIFO), the FIFO is full, and the full flag is active. The counters are one bit longer than the address required for the dual port RAM in order to make this comparison. This extra, most significant bit is used only by the flag comparator If the write address counter value is larger than the read address counter value plus half the depth of the RAM plus 1 (e.g., 2049 for a 4Kx9 FIFO), the FIFO is more than half full, and the half full flag is active. The flag outputs from the flag comparator are synchronized in flip flops by the appropriate read or write clocks so they change only following the rising edge of a clock.

Read and write enable are inhibited by the empty and full flags, respectively. If the FIFO is empty, read enable is inhibited because there is no next word in the FIFO to step to. If the FIFO is full, both the write enable and the write clock to the dual port RAM are inhibited because there is no place available to write another word. (The gates corresponding to these read and write enable inhibits are not shown on the simplified block diagram.) Note that when there is one word in the FIFO, read enable is allowed because the FIFO is stepping to the empty state to await another word. Write enable and read enable can be considered as "write next word" and "read next word," respectively.

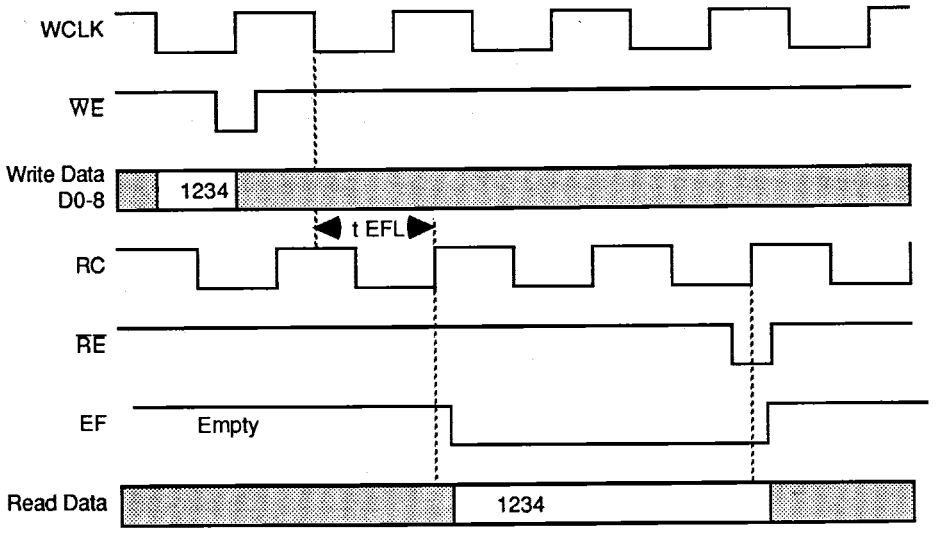
The general operation of the 7223/4 Clocked FIFO is shown in the following timing diagrams.



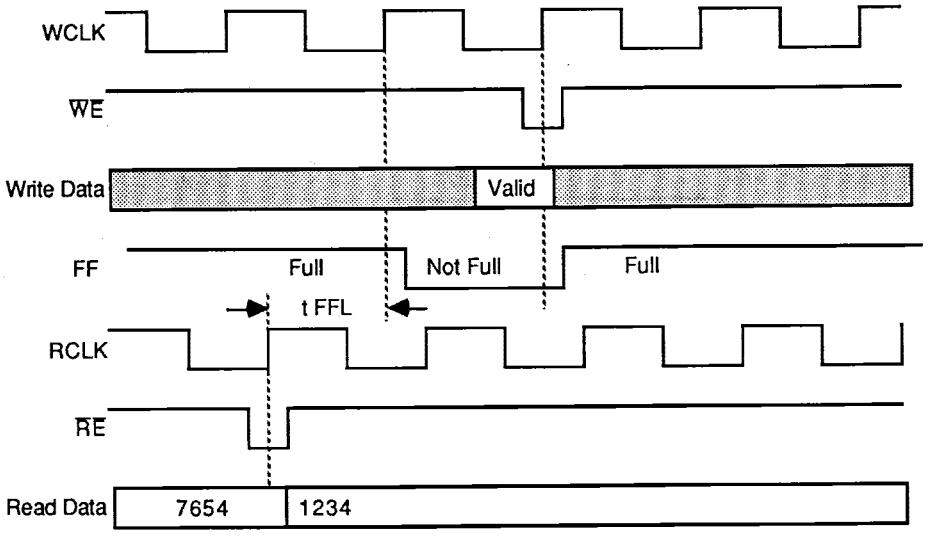
Write FIFO to Full



Read FIFO to Empty



Write, Read One Word to Empty FIFO



Read, Write One Word from Full FIFO

APPLICATION INFORMATION

Width Expansion

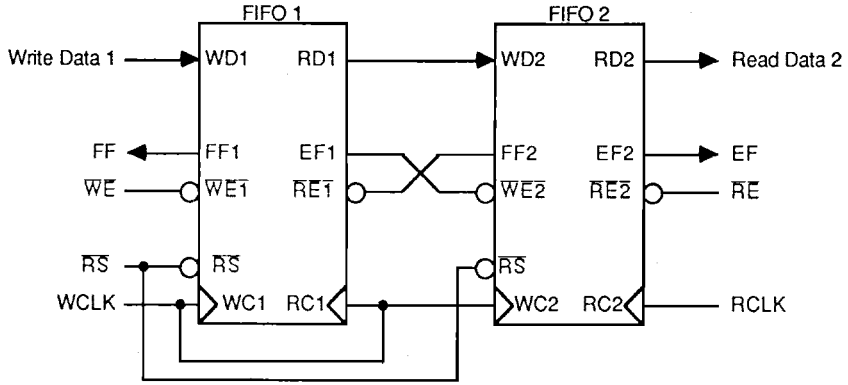
The 7223/4 Clocked FIFOs may be expanded in width by connecting the read and write clocks and enables and the reset lines of the FIFOs in parallel. The flags on all FIFOs will track, so any FIFO can be used for flag information.

Bus Width Funneling

The 7223/4 FIFOs simplify bus width funneling in high speed systems. Bus width funneling is where data must pass between two buses of different width, such as 32 bits and 8 bits. Funneling with the 7223/4 FIFOs is accomplished with external logic. The advantage of the 7223/4 Clocked FIFO interface is the simplification of the timing parameters for the funneling action. Funneling logic requires deciding which FIFOs are to be enabled for read or write on a particular cycle. For example, on a 32-bit to 8-bit transfer, 32-bit data is written into four FIFOs simultaneously. The 8-bit data is read out of the four FIFOs in round-robin fashion. With the 7223/4, most of the clock cycle is available for the round robin FIFO enable decision, since the read and write enables require only a short setup time before the rising edge of clock.

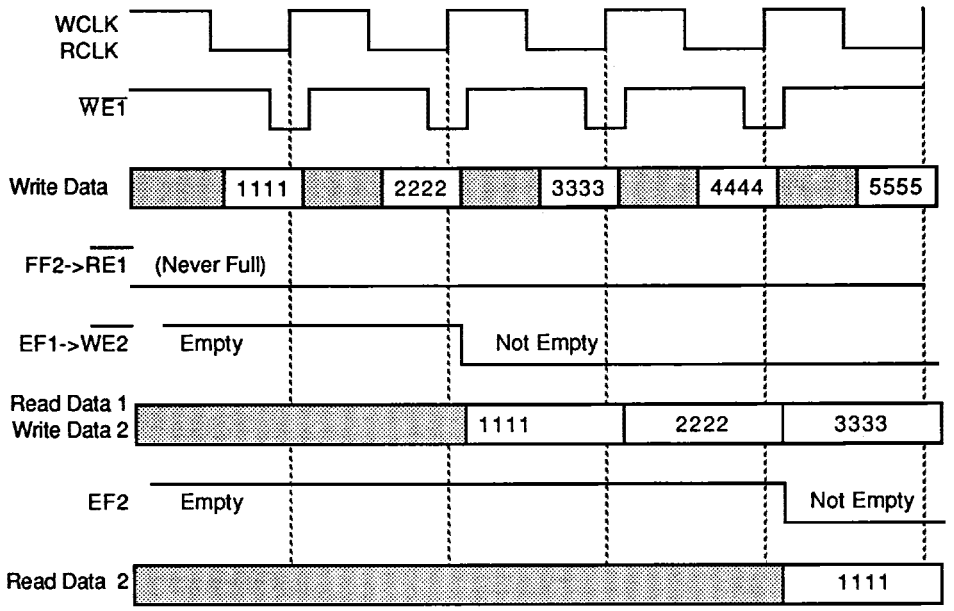
Depth Expansion

The 7223/4 is designed to be easily expanded in depth without additional logic by interconnecting the flags and enables of the FIFOs. The 7223/4 have empty and full flags which are compatible with their write and read enables, respectively. A depth expansion example is shown below. In this example, the flags and enables are interconnected, and the write clock is used to transfer data between the FIFOs. In general, the faster of the free running read or write clocks is used to clock data between the FIFOs.

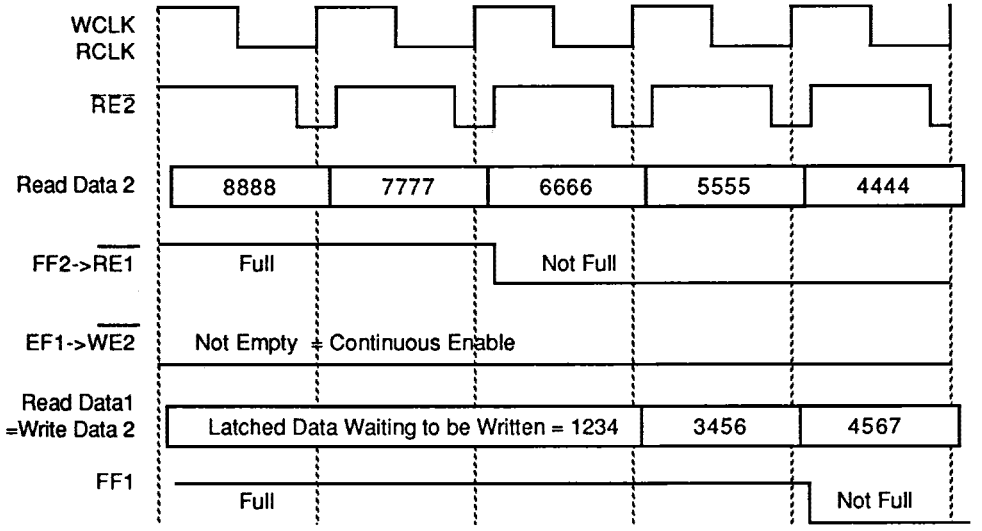


Cascading Two 7224 FIFOs to Make an 8Kx9 FIFO

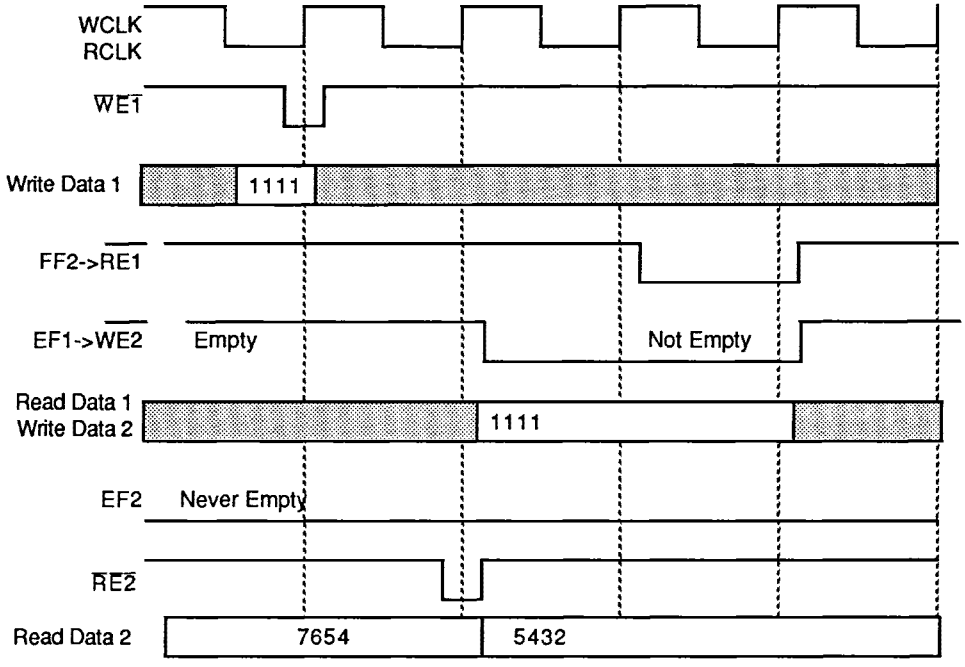
When the FIFOs are cascaded, data will be clocked from one FIFO to the next until an empty or full flag inhibits transfer by disabling the write or read enable of the other FIFO respectively as will as disabling the internal read or write, respectively, of the FIFO with the empty or full condition. This provides automatic, orderly transfer between the FIFO with a fall through time of the order of two clock times per FIFO in cascade. Timing diagrams for cascaded FIFOs are shown below.



Multiple Word Fall Through Two Empty FIFOs in Cascade



Multiple Word Fall Through Two Full FIFOs in Cascade



Detail of InterFIFO Transfer Handshake

One Word Transfer, First FIFO Initially Empty, Second FIFO Initially Full

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Ordering Information

Example:

QS7224-25VI

Device:	Speed (ns):	Package:	Grade:
7223 = 2kx9 7224 = 4kx9	commercial = 15,20,25,30 military = 20,25,30,40	P = plastic 300-mil DIP V = 300-mil SOJ JR = 32-PLCC L = 32-LCC D = 300-mil CERDIP or sidebraze	(blank) = commercial M = temperature -55 to +125 B = full 883 military I = industrial -45 to +85