

# Power Amplifier Module for LTE and 5G

The AFSC5G35D35 is a fully integrated Doherty power amplifier module designed for wireless infrastructure applications that demand high performance in the smallest footprint. Ideal for applications in massive MIMO systems, outdoor small cells, and low power remote radio heads. The field-proven LDMOS power amplifiers are designed for TDD and FDD LTE systems.

- Typical LTE Performance:  $P_{out} = 3 \text{ W Avg.}$ ,  $V_{DD} = 24 \text{ Vdc}$ ,  $1 \times 20 \text{ MHz LTE}$ , Input Signal PAR = 8 dB @ 0.01% Probability on CCDF.(1)

| Carrier Center Frequency | Gain (dB) | ACPR (dBc) | PAE (%) |
|--------------------------|-----------|------------|---------|
| 3400 MHz                 | 25.3      | -27.6      | 37.1    |
| 3500 MHz                 | 24.9      | -30.8      | 36.7    |
| 3600 MHz                 | 24.7      | -32.9      | 35.4    |

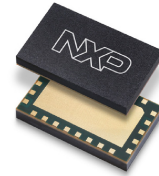
1. All data measured with device soldered in NXP reference circuit.

## Features

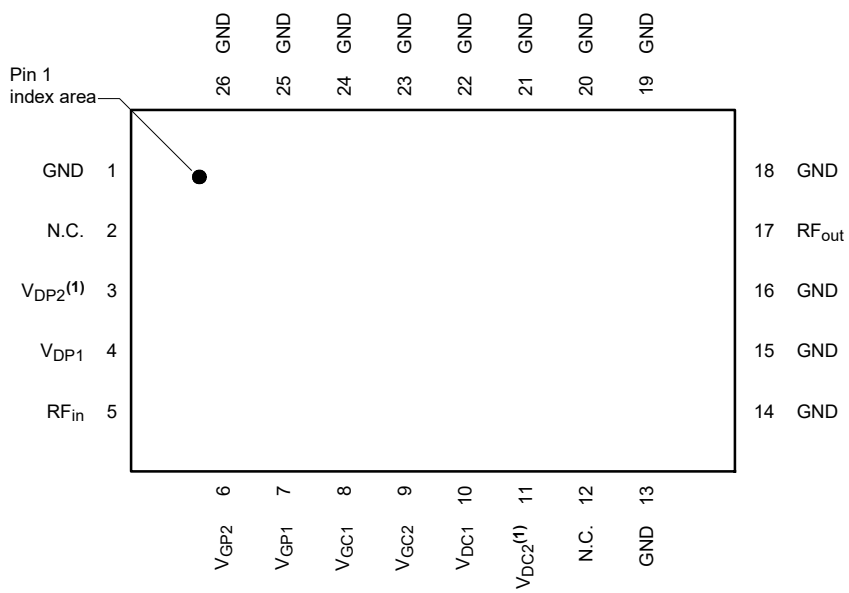
- Frequency: 3400–3600 MHz
- Advanced high performance in-package Doherty
- Fully matched (50 ohm input/output, DC blocked)
- Designed for low complexity analog or digital linearization systems

## AFSC5G35D35

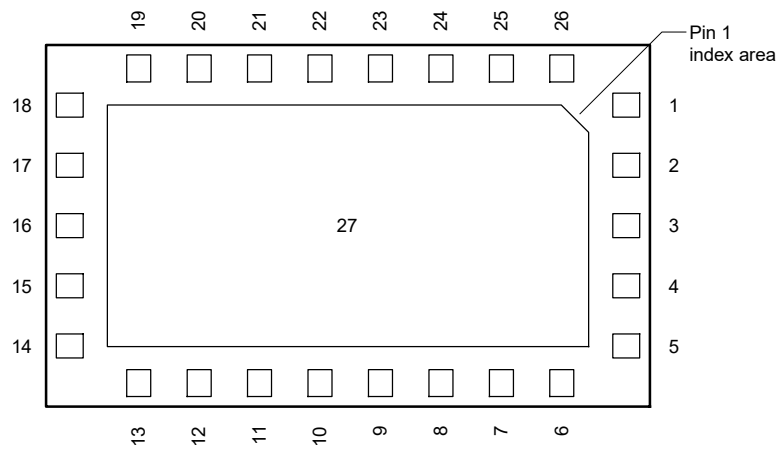
3400–3600 MHz, 26 dB, 3 W Avg.  
AIRFAST POWER AMPLIFIER  
MODULE



10 mm × 6 mm Module



(Top View)



(Bottom View)

Note: Exposed backside of the package is DC and RF ground.

**Figure 1. Pin Connections**

1.  $V_{DP2}$  and  $V_{DC2}$  are DC coupled internal to the package and must be powered by a single DC power supply.

**Table 1. Maximum Ratings**

| Rating  | Symbol    | Value       | Unit |
|---|-----------|-------------|------|
| Drain-Source Voltage  | $V_{DSS}$ | -0.5, +65   | Vdc  |
| Gate-Bias Voltage Range   | $V_G$     | -0.5 to +10 | Vdc  |
| Operating Voltage Range   | $V_{DD}$  | 0 to 32     | Vdc  |
| Storage Temperature Range   | $T_{stg}$ | -65 to +150 | °C   |
| Case Operating Temperature  | $T_C$     | 125         | °C   |
| Peak Input Power<br>(3500 MHz, Pulsed CW, 10 $\mu$ sec(on), 10% Duty Cycle) | $P_{in}$  | 30          | dBm  |

**Table 2. Lifetime**

| Characteristic   | Symbol | Value | Unit  |
|--|--------|-------|-------|
| Mean Time to Failure<br>Case Temperature 125°C, 3 W Avg., 32 Vdc | MTTF   | > 10  | Years |

**Table 3. ESD Protection Characteristics**

| Test Methodology                      | Class |
|---------------------------------------|-------|
| Human Body Model (per JS-001-2017)    | 1C    |
| Charge Device Model (per JS-002-2014) | C2    |

**Table 4. Moisture Sensitivity Level**

| Test Methodology                     | Rating | Package Peak Temperature | Unit |
|--------------------------------------|--------|--------------------------|------|
| Per JESD22-A113, IPC/JEDEC J-STD-020 | 3      | 260                      | °C   |

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

| Characteristic   | Symbol       | Typ | Range     | Unit |
|--|--------------|-----|-----------|------|
| <b>Carrier Stage 1 — On Characteristics</b>  |              |     |           |      |
| Gate Threshold Voltage <sup>(1)</sup><br>( $V_{DS} = 10\text{ Vdc}$ , $I_D = 1.6\ \mu\text{Adc}$ )                                       | $V_{GS(th)}$ | 1.1 | $\pm 0.4$ | Vdc  |
| Gate Quiescent Voltage<br>( $V_{DS} = 24\text{ Vdc}$ , $I_{DQ1A} = 19\text{ mAdc}$ )   | $V_{GS(Q)}$  | 2.0 | $\pm 0.4$ | Vdc  |
| Fixture Gate Quiescent Voltage <sup>(2)</sup><br>( $V_{DD} = 24\text{ Vdc}$ , $I_{DQ1A} = 19\text{ mAdc}$ , Measured in Functional Test) | $V_{GG(Q)}$  | 5.8 | $\pm 1.4$ | Vdc  |
| <b>Carrier Stage 2 — On Characteristics</b>  |              |     |           |      |
| Gate Threshold Voltage <sup>(1)</sup><br>( $V_{DS} = 10\text{ Vdc}$ , $I_D = 8.8\ \mu\text{Adc}$ )                                       | $V_{GS(th)}$ | 1.1 | $\pm 0.4$ | Vdc  |
| Gate Quiescent Voltage<br>( $V_{DS} = 24\text{ Vdc}$ , $I_{DQ2A} = 28\text{ mAdc}$ )   | $V_{GS(Q)}$  | 1.8 | $\pm 0.4$ | Vdc  |
| Fixture Gate Quiescent Voltage <sup>(3)</sup><br>( $V_{DD} = 24\text{ Vdc}$ , $I_{DQ2A} = 28\text{ mAdc}$ , Measured in Functional Test) | $V_{GG(Q)}$  | 2.6 | $\pm 1.2$ | Vdc  |
| <b>Peaking Stage 1 — On Characteristics <sup>(1)</sup></b>   |              |     |           |      |
| Gate Threshold Voltage<br>( $V_{DS} = 10\text{ Vdc}$ , $I_D = 3.2\ \mu\text{Adc}$ )  | $V_{GS(th)}$ | 1.1 | $\pm 0.4$ | Vdc  |
| <b>Peaking Stage 2 — On Characteristics <sup>(1)</sup></b>   |              |     |           |      |
| Gate Threshold Voltage<br>( $V_{DS} = 10\text{ Vdc}$ , $I_D = 16.8\ \mu\text{Adc}$ )   | $V_{GS(th)}$ | 1.1 | $\pm 0.4$ | Vdc  |

1. Each side of device measured separately.

2.  $V_{GG} = 2.90 \times V_{GS(Q)}$ . Parameter measured on NXP test fixture due to temperature compensation bias network on the board. Refer to reference circuit layout.

3.  $V_{GG} = 1.44 \times V_{GS(Q)}$ . Parameter measured on NXP test fixture due to temperature compensation bias network on the board. Refer to reference circuit layout.

(continued)

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

| Characteristic   | Symbol   | Min  | Typ          | Max          | Unit   |     |
|--|--|------|--------------|--------------|--------|-----|
| <b>Functional Tests</b> <sup>(1)</sup> (In NXP Doherty Production ATE <sup>(2)</sup> Test Fixture, 50 ohm system) $V_{DD} = 24\text{ Vdc}$ , $I_{DQ1A} = 19\text{ mA}$ , $I_{DQ2A} = 28\text{ mA}$ , $V_{GS1B} = (V_t - 0.01)$ <sup>(3)</sup> Vdc, $V_{GS2B} = (V_t - 0.22)$ <sup>(3)</sup> Vdc, $P_{out} = 3\text{ W Avg.}$ , Two-tone CW, $f_1 = 3470\text{ MHz}$ , $f_2 = 3530\text{ MHz}$ , 60 MHz Tone Spacing. |  |      |              |              |        |     |
| Gain   | G  | 22.7 | 23.7         | 26.1         | dB     |     |
| Drain Efficiency   | $\eta_D$   | 29.5 | 35.1         | —            | %      |     |
| Intermodulation Distortion   | IM3  | —    | -26.1        | -20.0        | dBc    |     |
| $P_{out}$ @ 3 dB Compression Point   | $f_1 = 3402.5\text{ MHz}$<br>$f_2 = 3597.5\text{ MHz}$ | P3dB | 40.0<br>41.2 | 42.0<br>42.2 | —<br>— | dBm |

**Wideband Ruggedness** <sup>(4)</sup> (In NXP Doherty Power Amplifier Module Reference Circuit, 50 ohm system)  $I_{DQ1A} = 19\text{ mA}$ ,  $I_{DQ2A} = 28\text{ mA}$ ,  $V_{GSP1} = 5.8\text{ Vdc}$ ,  $V_{GSP2} = 2.6\text{ Vdc}$ ,  $f = 3500\text{ MHz}$ , Additive White Gaussian Noise (AWGN) with 10 dB PAR

|   |                       |
|---|-----------------------|
| ISBW of 400 MHz at 24 Vdc, 9 W Avg. Modulated Output Power<br>(6 dB Input Overdrive from 3 W Avg. Modulated Output Power) | No Device Degradation |
|---|-----------------------|

**Typical Performance** <sup>(4)</sup> (In NXP Doherty Power Amplifier Module Reference Circuit, 50 ohm system)  $V_{DD} = 24\text{ Vdc}$ ,  $I_{DQ1A} = 19\text{ mA}$ ,  $I_{DQ2A} = 28\text{ mA}$ ,  $V_{GSP1} = 1.55\text{ Vdc}$ ,  $V_{GSP2} = 1.14\text{ Vdc}$ ,  $P_{out} = 3\text{ W Avg.}$ , 3500 MHz

|  |                  |        |            |        |       |
|--|------------------|--------|------------|--------|-------|
| VBW Resonance Point, 2-tone, 1 MHz Tone Spacing<br>(IMD Third Order Intermodulation Inflection Point)  | $VBW_{res}$      | —      | 300        | —      | MHz   |
| Quiescent Current Accuracy over Temperature <sup>(5)</sup><br>with 2.2 k $\Omega$ Gate Feed Resistors (-40 to 85°C) Stage 1<br>with 2.2 k $\Omega$ Gate Feed Resistors (-40 to 85°C) Stage 2 | $\Delta I_{QT}$  | —<br>— | 1.0<br>2.0 | —<br>— | %     |
| <b>1-carrier 20 MHz LTE, 8 dB Input Signal PAR</b>   |                  |        |            |        |       |
| Gain   | G                | —      | 24.9       | —      | dB    |
| Power Added Efficiency   | PAE              | —      | 36.7       | —      | %     |
| Adjacent Channel Power Ratio   | ACPR             | —      | -30.8      | —      | dBc   |
| Adjacent Channel Power Ratio   | ALT1             | —      | -40.0      | —      | dBc   |
| Adjacent Channel Power Ratio   | ALT2             | —      | -49.0      | —      | dBc   |
| Output Peak-to-Average Ratio @ 0.01% Probability   | PAR              | —      | 8.1        | —      | dB    |
| Gain Flatness <sup>(6)</sup>   | $G_F$            | —      | 0.5        | —      | dB    |
| <b>Fast CW, 27 ms Sweep</b>  |                  |        |            |        |       |
| $P_{out}$ @ 3 dB Compression Point   | P3dB             | —      | 43.2       | —      | dBm   |
| AM/PM @ P3dB   | $\Phi$           | —      | -25        | —      | °     |
| <b>Pulsed CW, 10 <math>\mu\text{sec}</math>(on), 10% Duty Cycle @ P1dB</b>   |                  |        |            |        |       |
| Gain Variation over Temperature<br>(-40°C to +105°C)   | $\Delta G$       | —      | 0.029      | —      | dB/°C |
| Output Power Variation over Temperature<br>(-40°C to +105°C)   | $\Delta P_{1dB}$ | —      | 0.016      | —      | dB/°C |

**Table 6. Ordering Information**

| Device        | Tape and Reel Information                               | Package             |
|---------------|---|---------------------|
| AFSC5G35D35T2 | T2 Suffix = 2,000 Units, 24 mm Tape Width, 13-inch Reel | 10 mm x 6 mm Module |

- Part input and output matched to 50 ohms.
- ATE is a socketed test environment.
- Refer to AN12071, *Doherty Biasing Methodology for Volume Production*. Go to <http://www.nxp.com/RF> and search for AN12071.
- All data measured in fixture with device soldered in NXP reference circuit.
- Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.nxp.com/RF> and search for AN1977 or AN1987.
- Gain flatness =  $\text{Max}(G(f_{Low} \text{ to } f_{High})) - \text{Min}(G(f_{Low} \text{ to } f_{High}))$

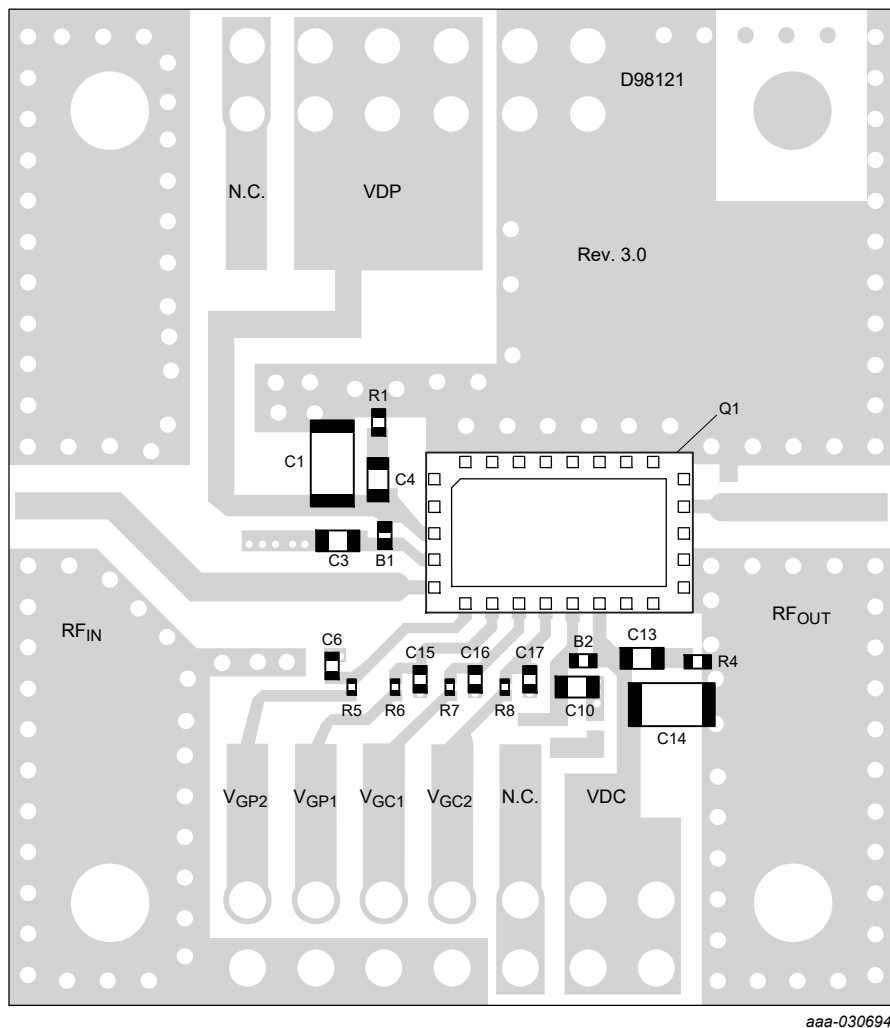


Figure 2. AFSC5G35D35 Reference Circuit Component Layout

Table 7. AFSC5G35D35 Reference Circuit Component Designations and Values

| Part              | Description                                 | Part Number       | Manufacturer |
|-------------------|---|-------------------|--------------|
| B1, B2            | 30 $\Omega$ Ferrite Bead                    | BLM15PD300SN1     | Murata       |
| C1, C14           | 10 $\mu$ F Chip Capacitor                   | CL31A106KBHNNNE   | Samsung      |
| C3, C4, C10, C13  | 1 $\mu$ F Chip Capacitor                    | 06035D105KAT2A    | AVX          |
| C6, C15, C16, C17 | 0.1 $\mu$ F Chip Capacitor                  | GRM155R61H104KE14 | Murata       |
| Q1                | Power Amplifier Module                      | AFSC5G35D35       | NXP          |
| R1, R4            | 5.1 $\Omega$ , 1/10 W Chip Resistor         | ERJ-2GEJ5R1X      | Panasonic    |
| R5, R6, R7, R8    | 2.2 k $\Omega$ , 1/20 W Chip Resistor       | ERJ-1GEJ222C      | Panasonic    |
| PCB               | Rogers RO4350B, 0.020", $\epsilon_r = 3.67$ | D98121            | MTL          |

Note: Component numbers C2, C5, C7, C8, C9, C11, C12, R2 and R3 are intentionally omitted.

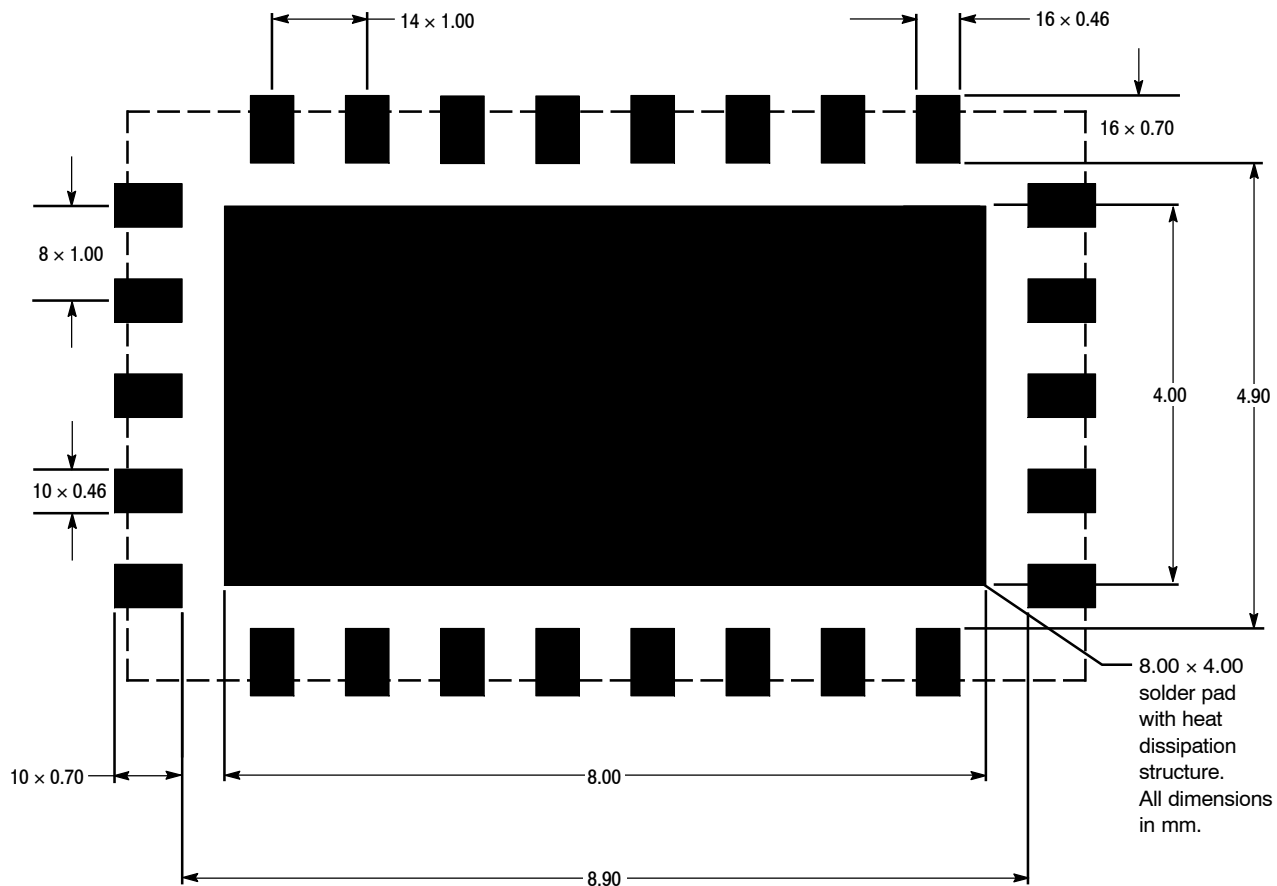
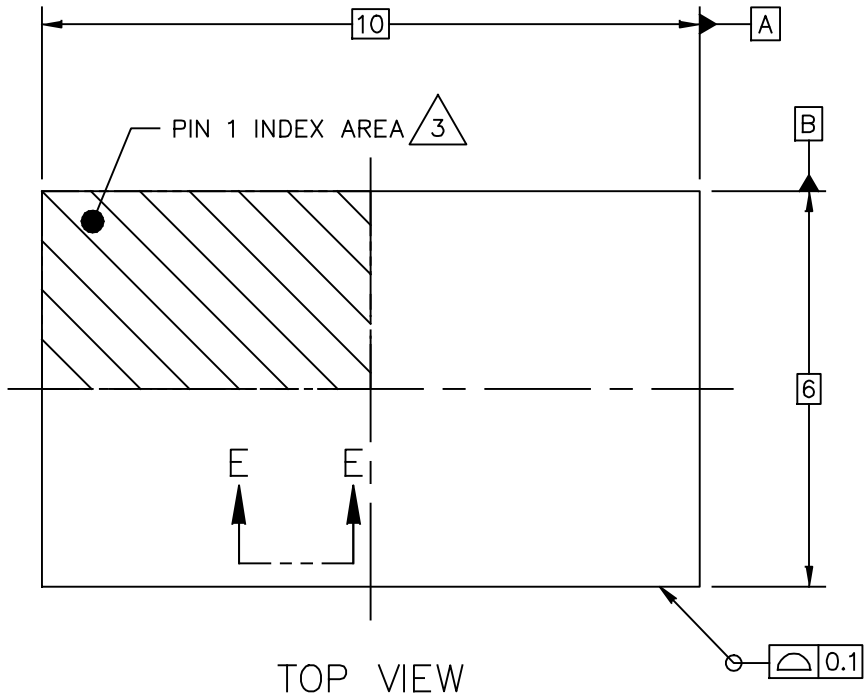


Figure 3. PCB Pad Layout for 10 mm x 6 mm Module



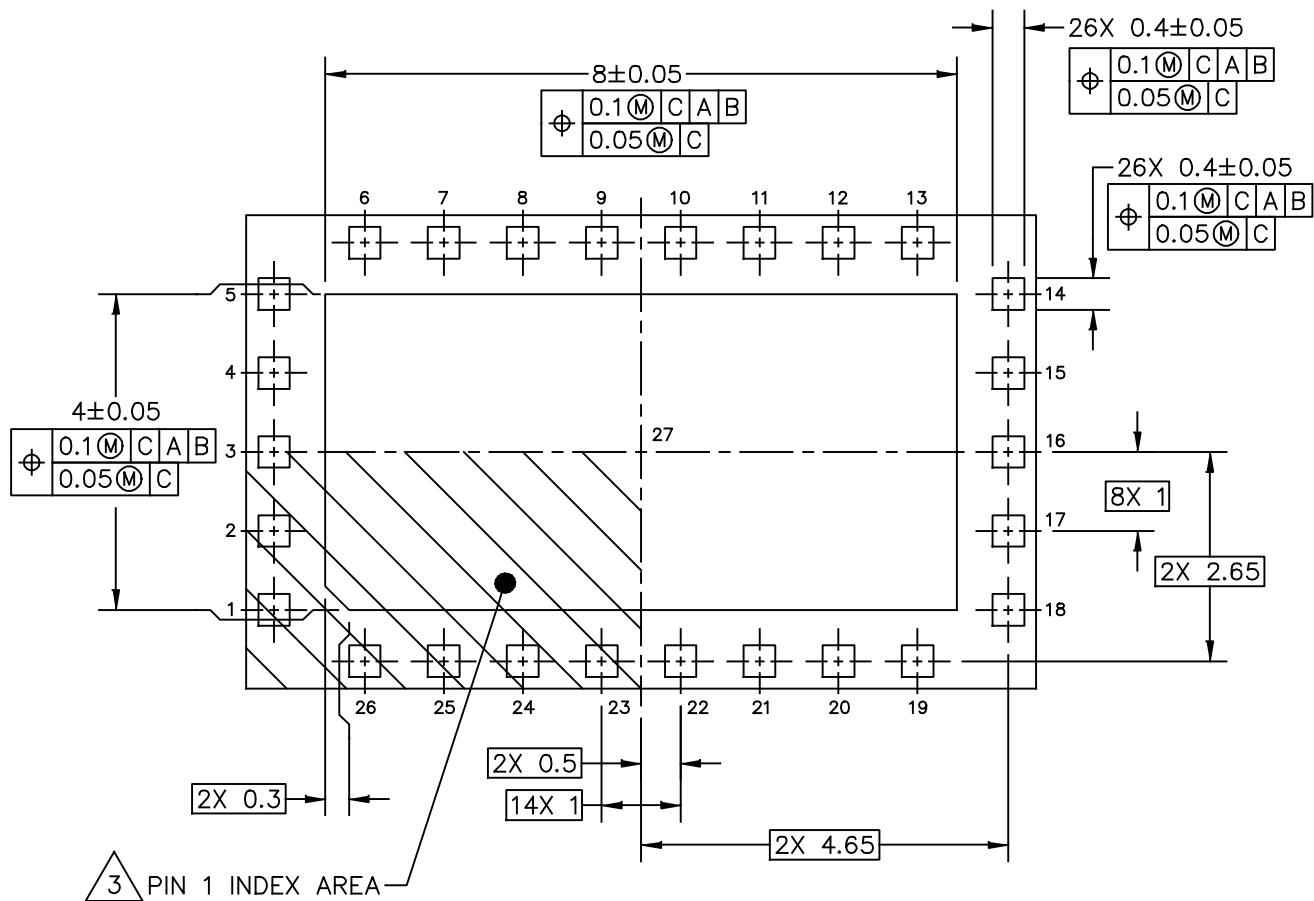
Figure 4. Product Marking

PACKAGE DIMENSIONS

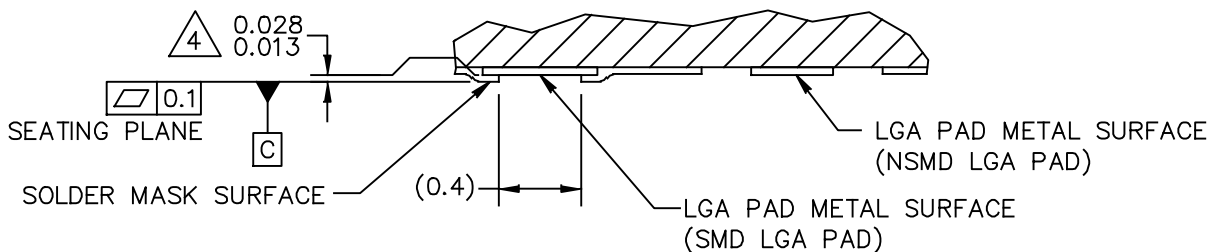


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| TITLE: WBMOD,<br>10 X 6 X 1.348 PKG,<br>1 MM PITCH, 27 I/O | DOCUMENT NO: 98ASA00953D | REV: A                     |
|  | STANDARD: NON-JEDEC      |                            |
|  | SOT1831-1                | 20 JUL 2017                |





VIEW D-D  
(BOTTOM VIEW)



SECTION E-E  $\triangle 5$

|  |                    |                            |             |
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|  |                    | STANDARD: NON-JEDEC        |             |
|  |                    | SOT1831-1                  | 20 JUL 2017 |

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. PIN 1 CONFIGURATION MAY VARY.

4. DIMENSION APPLIES TO ALL LEADS AND FLAG.

5. THE BOTTOM VIEW SHOWS THE SOLDERABLE AREA OF THE PADS. THE CENTER PAD (PIN 27) IS SOLDER MASK DEFINED. SOME PERIPHERAL PADS ARE SOLDER MASK DEFINED (SMD) AND OTHERS ARE NON–SOLDERMASK DEFINED (NSMD).

|  |                    |                            |             |
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|  |                    | STANDARD: NON–JEDEC        |             |
|  |                    | SOT1831–1                  | 25 JUL 2017 |

## PRODUCT DOCUMENTATION AND TOOLS

Refer to the following resources to aid your design process.

### Application Notes

- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN12071: Doherty Biasing Methodology for Volume Production

### Development Tools

- Printed Circuit Boards

## FAILURE ANALYSIS

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where NXP is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local NXP Sales Office.

## REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date      | Description  |
|----------|-----------|--|
| 0        | May 2018  | <ul style="list-style-type: none"><li>• Initial release of data sheet</li></ul>  |
| 1        | July 2018 | <ul style="list-style-type: none"><li>• Table 3, ESD Protection Characteristics: changed ESD human body model (HBM) from Class 1B to 1C to reflect recent ESD test results of the device, p. 2</li></ul>   |
| 2        | May 2019  | <ul style="list-style-type: none"><li>• Typical LTE Performance table: table values and condition updated to reflect 1 × 20 MHz LTE performance measurement, pp. 1, 5</li><li>• Table 1, Maximum Ratings: add drain-source voltage to table, p. 3</li><li>• Added Wideband Ruggedness table, p. 5</li><li>• General updates made to align data sheet to current standard</li></ul> |

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