

MAXIM

10Gbps Modulator Driver

MAX3942

General Description

The MAX3942 is designed to drive high-speed optical modulators at data rates up to 10.7Gbps. It functions as a modulation circuit, with an integrated control op amp externally programmed by a DC voltage.

A high-bandwidth, fully differential signal path is internally implemented to minimize jitter accumulation. When a clock signal is available, the integrated data-retiming function can be selected to reject input-signal jitter.

The MAX3942 receives differential CML signals (ground-referenced) with on-chip line terminations of 50Ω . Each of the differential outputs has an on-chip 50Ω resistor for back termination. The driver is able to deliver a modulation current of $40\text{mA}_{\text{P-P}}$ to $120\text{mA}_{\text{P-P}}$, with an edge speed of 23ps (typical 20% to 80%). This modulation current reflects a modulation voltage of $1.0\text{V}_{\text{P-P}}$ to $3.0\text{V}_{\text{P-P}}$ single ended or $2.0\text{V}_{\text{P-P}}$ to $6.0\text{V}_{\text{P-P}}$ differential.

The MAX3942 also includes an adjustable pulse-width control circuit to precompensate for asymmetrical modulator characteristics. It is available in a compact 4mm x 4mm, 24-pin thin QFN package and operates over the -40°C to $+85^\circ\text{C}$ temperature range.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3942ETG	-40°C to $+85^\circ\text{C}$	24 Thin QFN (4mm x 4mm)
MAX3942ETG+	-40°C to $+85^\circ\text{C}$	24 Thin QFN (4mm x 4mm)

+Denotes a lead-free package.

Features

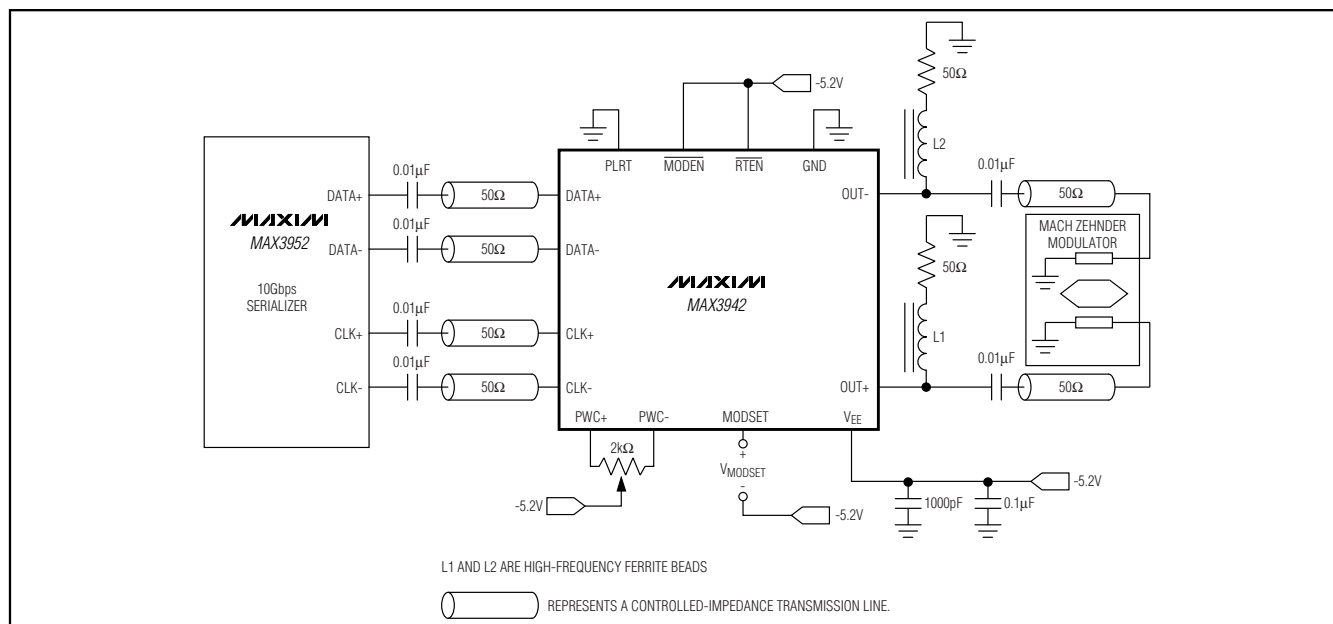
- ◆ 23ps Edge Speed
- ◆ Single-Ended Modulation Voltage Up to $3\text{V}_{\text{P-P}}$
- ◆ Differential Modulation Voltage Up to $6\text{V}_{\text{P-P}}$
- ◆ Selectable Data-Retiming Latch
- ◆ Up to 10.7Gbps Operation
- ◆ 50Ω On-Chip Input and Output Terminations
- ◆ Pulse-Width Adjustment
- ◆ Enable and Polarity Controls
- ◆ ESD Protection

Applications

Mach Zehnder Modulators
 Packaged Direct-Modulated Lasers
 SONET OC-192 and SDH STM-64 Transmission Systems
 DWDM Systems
 Long/Short-Reach Optical Transmitters
 10Gbps Ethernet

Pin Configuration appears at end of data sheet.

Typical Application Circuit



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{EE} -6.0V to +0.5V
 Voltage at MODEN, RTEN, PLRT, MODSET.....($V_{EE} - 0.5V$) to +0.5V
 Voltage at DATA+, DATA-, CLK+, and CLK-.....-1.65V to +0.5V
 Voltage at OUT+, OUT--4V to +0.5V
 Voltage at PWC+, PWC-($V_{EE} - 0.5V$) to ($V_{EE} + 1.7V$)

Continuous Power Dissipation ($T_A = +85^\circ\text{C}$)
 24-Pin Thin QFN (derate 20.8mW/ $^\circ$ above $+85^\circ\text{C}$)1354mW
 Current into or out of OUT+, OUT-80mA
 Storage Temperature Range-55 $^\circ\text{C}$ to +150 $^\circ\text{C}$
 Operating Temperature Range-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
 Lead Temperature (soldering, 10s).....+300 $^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{EE} = -5.5V$ to $-4.9V$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. Typical values are at $V_{EE} = -5.2V$, $I_{MOD} = 100\text{mA}$, and $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Voltage	V_{EE}		-5.5		-4.9	V
Supply Current	I_{EE}	Excluding I_{MOD} (Note 1)		125	175	mA
			Retime disabled			
				140	200	
Power-Supply Noise Rejection	PSNR	$f \leq 2\text{MHz}$ (Note 2); see Figure 3		15		dB
SIGNAL INPUT (Note 3)						
Input Data Rates		NRZ		10.7		Gbps
Single-Ended Input Resistance	R_{IN}	Input to GND	42.5	50	58.5	Ω
Single-Ended Input Voltage	V_{IS}	DC-coupled, Figure 1a	-1		0	V
		AC-coupled, Figure 1b	-0.4		+0.4	
Differential Input Voltage	V_{ID}	DC-coupled (Note 4)	0.2		2.0	V_{P-P}
		AC-coupled (Note 4)	0.2		1.6	
Differential Input Return Loss	RL_{IN}	$\leq 15\text{GHz}$		15		dB
MODULATION (Note 5)						
Maximum Modulation Current			112	120		mA_{P-P}
Minimum Modulation Current		$V_{MODSET} = V_{EE}$		37	41	mA_{P-P}
MODSET Voltage Range	V_{MODSET}		V_{EE}		$V_{EE} +$	V
Equivalent Modulation	R_{MODEQV}	(Note 7)		11.1		Ω
Modulation Set Bandwidth		Modulation depth 10%, 50 Ω driver load		5		MHz
MODSET Input Resistance				20		k Ω
Modulation-Current Temperature Stability		(Note 6)	-980		0	ppm/ $^\circ\text{C}$
Modulation-Current-Setting Error		50 Ω driver load, $T_A = +25^\circ\text{C}$	-10		+10	%
Output Resistance	R_{OUT}	OUT+ and OUT- to GND	42.5	50	58.5	Ω

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ELECTRICAL CHARACTERISTICS (continued)

($V_{EE} = -5.5V$ to $-4.9V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$. Typical values are at $V_{EE} = -5.2V$, $I_{MOD} = 100mA$, and $T_A = +25^{\circ}C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Off Current		$\overline{MODEN} = V_{EE}$, $MODSET = V_{EE}$, $DATA+ =$ high, $DATA- =$ low			1.6	mA
Differential Output Return Loss	RL _{OUT}	$I_{MOD} = 50mA$ 10GHz		10		dB
Output Edge Speed		20% to 80% (Notes 6, 8)		23	32	ps
Setup/Hold Time	t_{SU} , t_{HD}	Figure 2 (Note 6)	25			ps
Pulse-Width Adjustment Range		(Notes 6, 8)	± 30	± 50		ps
Pulse-Width Control Input Range (Single Ended)		For PWC+ and PWC-	$V_{EE} + 0.5$		$V_{EE} + 1.5$	V
Pulse-Width Control Input Range (Differential)		(PWC+) - (PWC-)	-0.5		+0.5	V
Output Overshoot	δ	(Notes 6, 8)		5		%
Driver Random Jitter	RJ _{DR}	(Note 6)		0.3	0.8	ps _{RMS}
Driver Deterministic Jitter	DJ _{DR}	PWC- = GND (Notes 6, 9)		8	13	ps _{P-P}
CONTROL INPUTS						
Input High Voltage	V_{IH}	(Note 10)	$V_{EE} + 2.0$			V
Input Low Voltage	V_{IL}	(Note 10)			$V_{EE} + 0.8$	V
Input Current		(Note 10)	-80		+200	μA

Note 1: Supply current remains elevated once the retiming function has been enabled. Power must be cycled to reduce supply current after the retiming function has been disabled.

Note 2: Power-supply noise rejection is specified as $PSNR = 20\text{Log}(V_{\text{noise}}(\text{on } V_{CC}) / \Delta V_{\text{OUT}})$. V_{OUT} is the voltage across a 50 Ω load. $V_{\text{noise}}(\text{on } V_{CC}) = 100\text{mV}_{\text{P-P}}$.

Note 3: For DATA+, DATA-, CLK+, and CLK-.

Note 4: CLK input characterized at 10.7Gbps.

Note 5: Minimum voltage on OUT+ and OUT- is $V_{EE} + 1.9V$.

Note 6: Guaranteed by design and characterization using the circuit shown in Figure 3.

Note 7: $R_{MODEQV} = (V_{MODSET} - V_{EE}) / (I_{MOD} - 37mA)$.

Note 8: 50 Ω load, characterized at 10.7Gbps with a 1111 1111 0000 0000 pattern.

Note 9: Deterministic jitter is defined as the arithmetic sum of PWD (pulse-width distortion) and PDJ (pattern-dependent jitter). Measured with a 10.7Gbps $2^7 - 1$ PRBS pattern with 80 zeros and 80 ones inserted in the data pattern.

Note 10: For \overline{MODEN} and PLRT.

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Test Circuits and Timing Diagrams

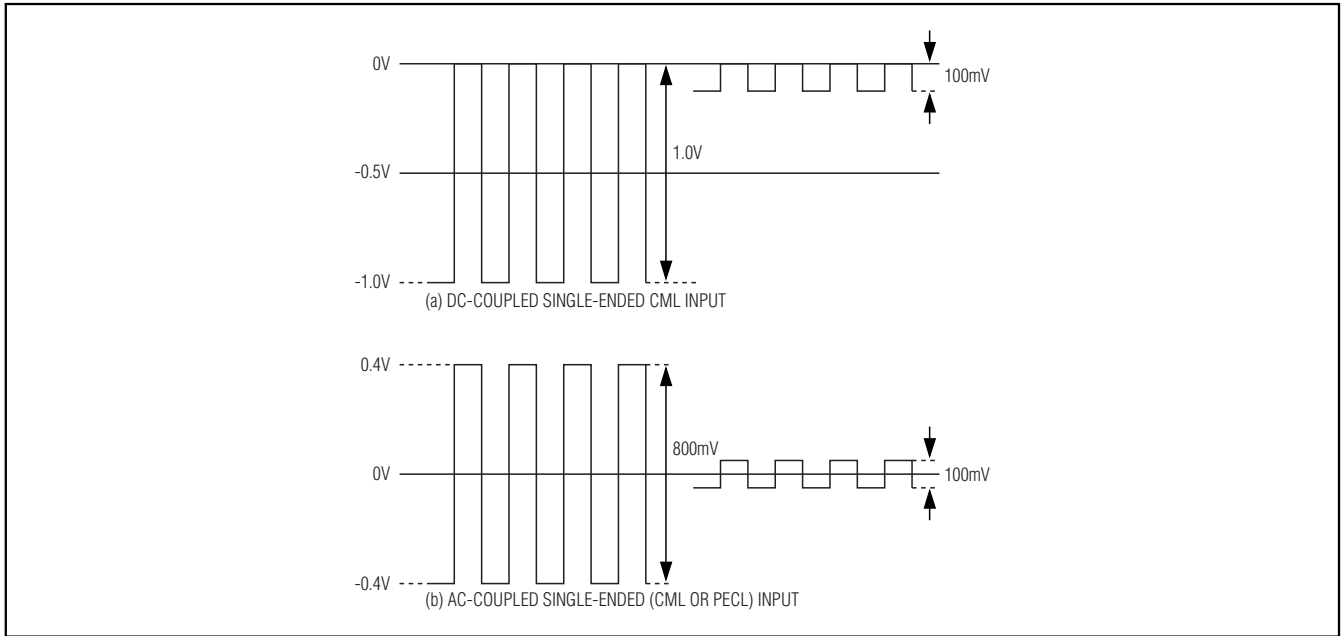


Figure 1. Definition of Single-Ended Input Voltage Range

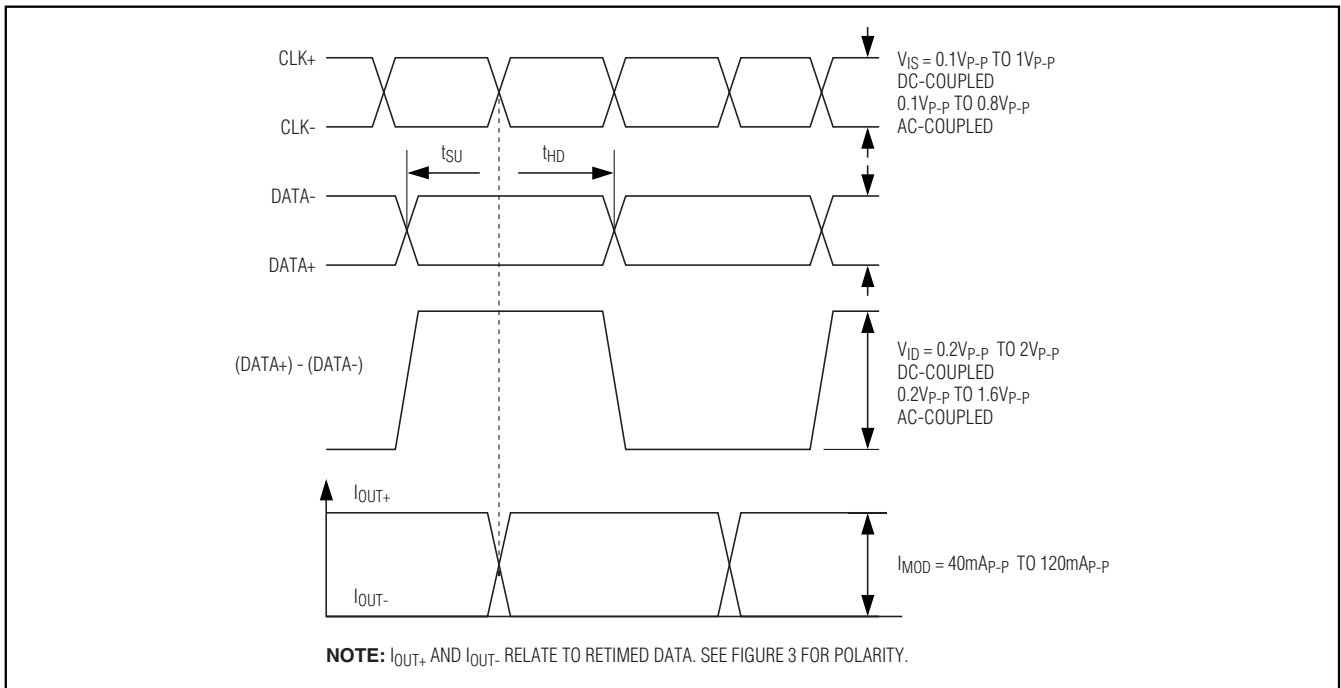


Figure 2. Setup and Hold Timing Definition

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Test Circuits and Timing Diagrams (continued)

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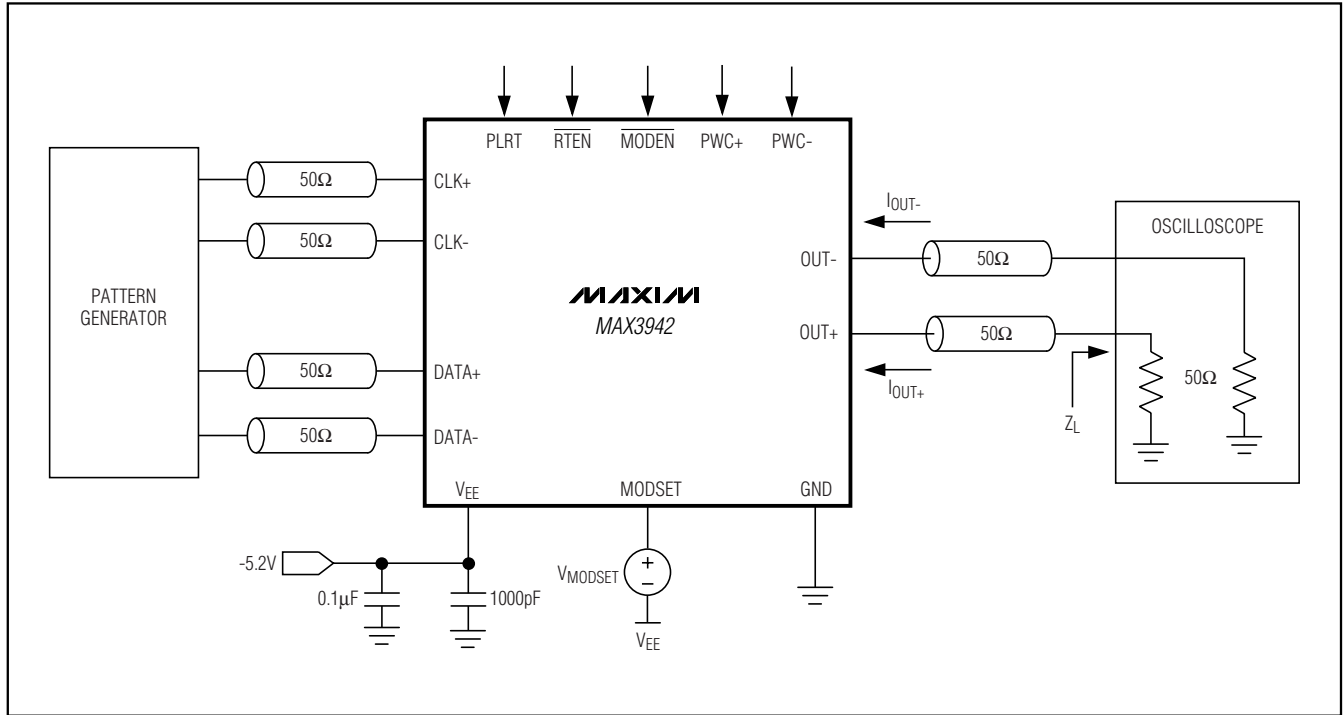


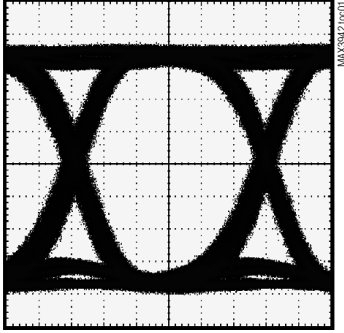
Figure 3. AC Characterization Circuit

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Typical Operating Characteristics

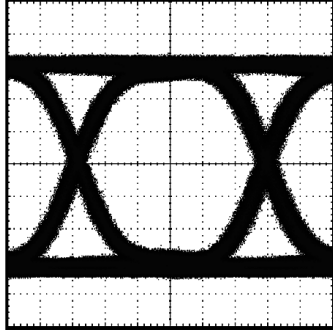
(Typical values are at $V_{EE} = -5.2V$, $I_{MOD} = 100mA$, $T_A = +25^\circ C$, unless otherwise noted.)

10.7Gbps ELECTRICAL EYE DIAGRAM
($V_{MOD} = 2V_{P-P}$ DIFFERENTIAL, $2^{31} - 1$ PRBS)



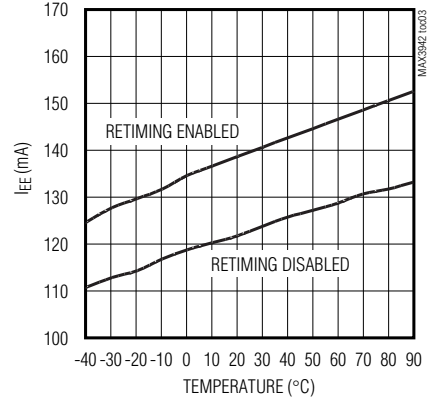
16ps/div

10.7Gbps ELECTRICAL EYE DIAGRAM
($V_{MOD} = 6V_{P-P}$ DIFFERENTIAL, $2^{31} - 1$ PRBS)

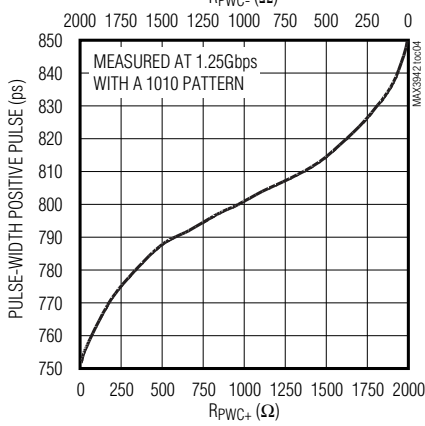


16ps/div

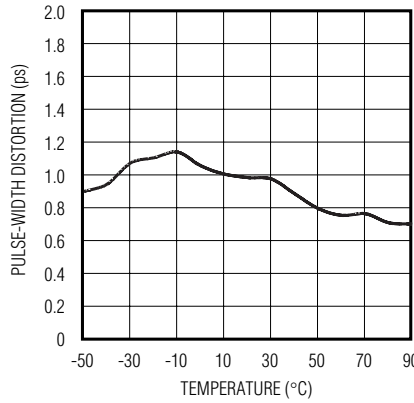
SUPPLY CURRENT vs. TEMPERATURE
(50Ω LOAD, EXCLUDES I_{MOD})



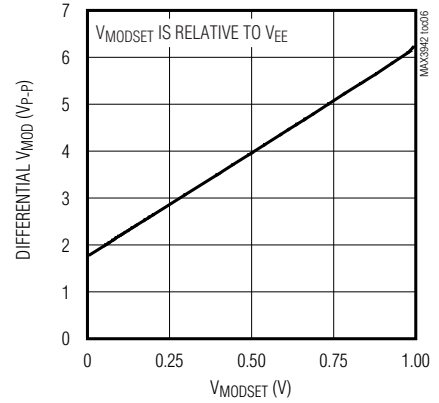
PULSE WIDTH vs. R_{PWC}



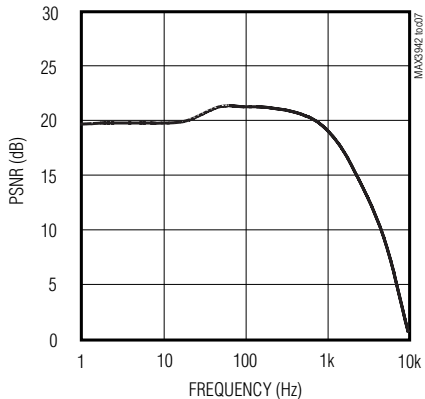
PULSE-WIDTH DISTORTION vs. TEMPERATURE



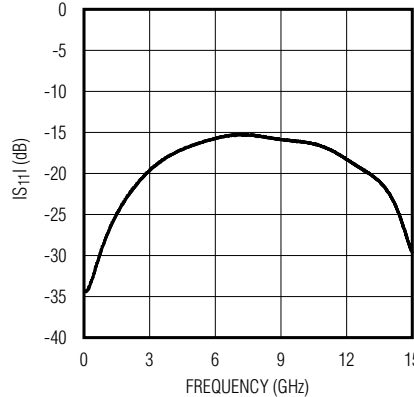
DIFFERENTIAL V_{MOD} vs. V_{MODSET}
($Z_L = 50\Omega$ ON OUT+ AND OUT-)



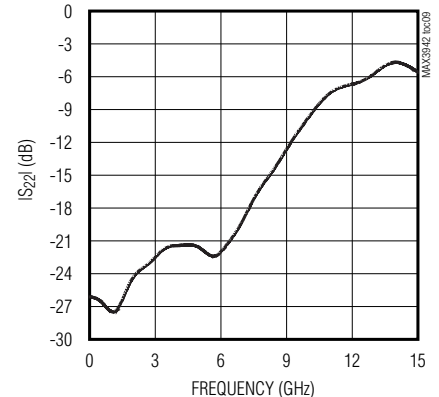
POWER-SUPPLY NOISE REJECTION vs. FREQUENCY



DIFFERENTIAL S_{11} vs. FREQUENCY (DEVICE POWERED)



DIFFERENTIAL S_{22} vs. FREQUENCY (DEVICE POWERED)



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Pin Description

PIN	NAME	FUNCTION
1	DATA+	Noninverting Data Input, with 50Ω On-Chip Termination
2	DATA-	Inverting Data Input, with 50Ω On-Chip Termination
3, 4, 14, 17	GND	Ground. All pins must be connected to board ground.
5	CLK+	Noninverting Clock Input for Data Retiming, with 50Ω On-Chip Termination
6	CLK-	Inverting Clock Input for Data Retiming, with 50Ω On-Chip Termination
7, 11, 12, 13, 18, 19, 21, 24	VEE	Negative Supply Voltage. All pins must be connected to board VEE.
8	PWC+	Positive Input for Modulation Pulse-Width Adjustment (see the <i>Design Procedure</i> section).
9	PWC-	Negative Input for Modulation Pulse-Width Adjustment. Ground to disable the pulse-width adjustment feature (see the <i>Design Procedure</i> section).
10	MODSET	Modulation Current Set. Apply a voltage to set the modulation current of the driver output.
15	OUT-	Inverting Driver Output. Provides modulation output with 50Ω back termination. Sinks current when PLRT is high and when differential data is high.
16	OUT+	Noninverting Driver Output. Provides modulation output with 50Ω back termination. Sinks current when PLRT is high and when differential data is low.
20	PLRT	Differential Data Polarity Swap Input. Set high or float for normal operation. Set low to invert the differential signal polarity. Contains an internal 100kΩ pullup to GND.
22	$\overline{\text{MODEN}}$	TTL/CMOS Modulation Enable Input. Set low or float for normal operation. Set high to put the EAM in the absorption (logic 0) state. Contains an internal 100kΩ pulldown to VEE.
23	$\overline{\text{RTEN}}$	Data-Retiming Input. Connect to VEE for retimed data. Connect to GND to bypass retiming latch.
EP	Exposed Pad	Ground. Must be soldered to the circuit board ground for proper thermal and electrical performance. See the <i>Layout Considerations</i> section.

Detailed Description

The MAX3942 modulator driver accepts differential clock and data inputs that are compatible with PECL and CML logic levels.

The modulation output stage is composed of a high-speed differential pair and a programmable current source with a maximum modulation current of 120mA. The rise and fall times are typically 23ps. The modulation current is designed to produce a modulation voltage up to 3.0V_{P-P} single endedly, or 6.0V_{P-P} differentially when driving a 50Ω module. The 3.0V_{P-P} results from 120mA_{P-P} through the parallel combination of the 50Ω modulator load and the internal 50Ω back termination.

Polarity Switch

The MAX3942 includes a polarity switch. When the PLRT pin is high or left floating, the outputs maintain the polarity of the input data. When the PLRT pin is low, the outputs are inverted relative to the input data.

Clock/Data Input Logic Levels

The MAX3942 is directly compatible with ground-reference CML. Either DC- or AC-coupling may be used for CML referenced to ground. For all other logic types, AC-coupling should be used.

Optional Data Input Latch

To reject pattern-dependent jitter in the input data, a synchronous differential clock signal should be connected to the CLK+ and CLK- inputs, and the $\overline{\text{RTEN}}$ control input should be connected to VEE.

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The input data is retimed on the rising edge of CLK+. If $\overline{\text{RTEN}}$ is connected to ground, the retiming function is disabled and the input data is directly connected to the output stage. Leave CLK+ and CLK- open when retiming is disabled.

Pulse-Width Control

The pulse-width control circuit can be used to compensate for pulse-width distortion introduced by the modulator. The differential voltage between PWC+ and PWC- adjusts the pulse-width compensation. The adjustment range is typically $\pm 50\text{ps}$. Optional single-ended operation is possible by forcing a voltage on the PWC+ pin while leaving the PWC- pin unconnected. When PWC- is connected to ground, the pulse-width control circuit is automatically disabled.

Modulation Output Enable

The MAX3942 incorporates a modulation current-enable input. When $\overline{\text{MODEN}}$ is low or floating, the modulation outputs OUT+ and OUT- are enabled. When $\overline{\text{MODEN}}$ is high, the drive current is switched to OUT+. The typical enable time is 2ns and the typical disable time is 2ns.

Design Procedure

Programming the Modulation Voltage

The modulation voltage results from I_{MOD} passing through the load impedance (Z_L) in parallel with the internal 50Ω termination resistor (R_{OUT}):

$$V_{\text{MOD}} \approx I_{\text{MOD}} \times \frac{Z_L \times R_{\text{OUT}}}{Z_L + R_{\text{OUT}}}$$

To program the desired modulation current, force a voltage at the MODSET pin (see the *Typical Application Circuit*). The resulting I_{MOD} current can be calculated by the following equation:

$$I_{\text{MOD}} \approx \frac{V_{\text{MODSET}}}{11.1\Omega} + 37\text{mA}$$

An internal, independent current source drives a constant 37mA to the modulation circuitry and any voltage above V_{EE} on the MODSET pin adds to this. The input impedance of the MODSET pin is typically $20\text{k}\Omega$. Note that the minimum output voltage is $V_{\text{EE}} + 1.9\text{V}$.

Programming the Pulse-Width Control

Three methods of control are possible when pulse predistortion is desired to minimize distortion at the receiver. The pulse width may be set with a $2\text{k}\Omega$ potentiometer with the center tapped to V_{EE} (or equivalent fixed resistors), or by applying a voltage to the PWC+ pin, or by applying a differential voltage across the PWC+ and PWC- pins. See Table 1 for the desired effect of the pulse-width setting. Pulse width is defined as $(\text{positive pulse width}) / ((\text{positive pulse width} + \text{negative pulse width}) / 2)$.

Input Termination Requirement

The MAX3942 data and clock inputs are CML compatible. However, it is not necessary to drive the IC with a standard CML signal. As long as the specified input voltage swings are met, the MAX3942 operates properly.

Applications Information

Layout Considerations

To minimize loss and crosstalk, keep the connections between the MAX3942 output and the modulator as short as possible. Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk. Circuit boards should be made using low-loss dielectrics. Use controlled-impedance lines for the clock and data inputs, as well as for the data output.

Table 1. Pulse-Width Control

PULSE WIDTH (%)	$R_{\text{PWC+}}, R_{\text{PWC-}}$ FOR $R_{\text{PWC+}} + R_{\text{PWC-}} = 2\text{k}\Omega$	$V_{\text{PWC+}}$ (PWC- OPEN) (V)	$V_{\text{PWC+}} - V_{\text{PWC-}}$ (V)
100	$R_{\text{PWC+}} = R_{\text{PWC-}}$	$V_{\text{EE}} + 1$	0
>100	$R_{\text{PWC+}} > R_{\text{PWC-}}$	$> V_{\text{EE}} + 1$	>0
<100	$R_{\text{PWC+}} < R_{\text{PWC-}}$	$< V_{\text{EE}} + 1$	<0

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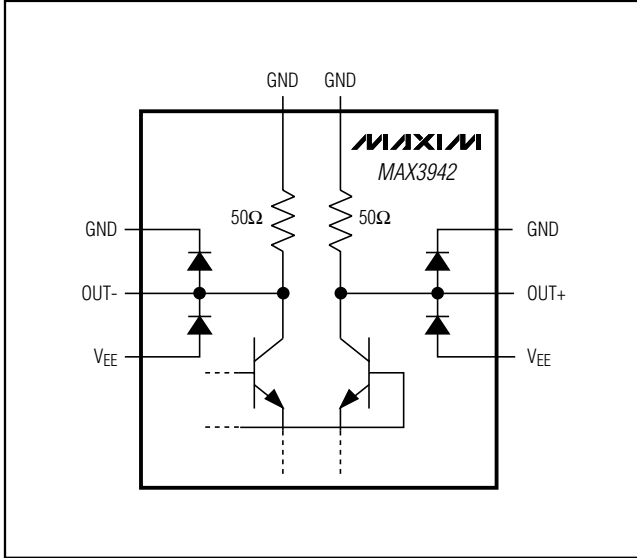


Figure 6. Simplified Output Circuit

Exposed-Pad Package

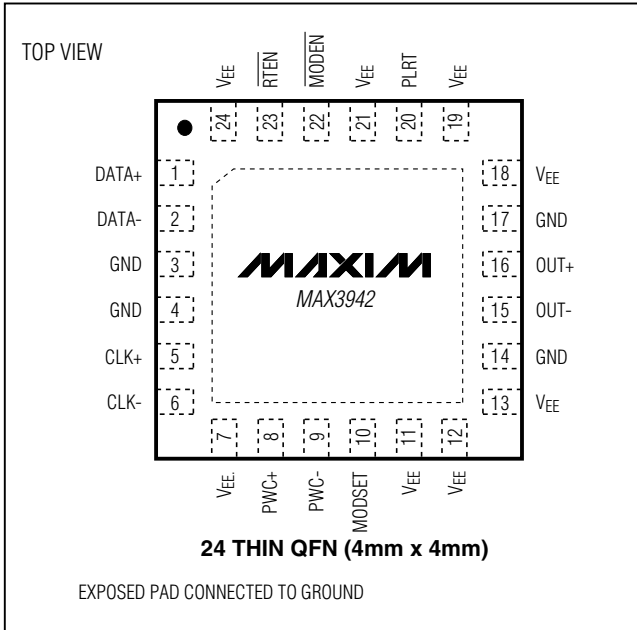
The exposed pad on the 24-pin QFN provides a very low thermal resistance path for heat removal from the IC. The pad is also electrical ground on the MAX3942 and must be soldered to the circuit board ground for proper thermal and electrical performance. Refer to Maxim Application Note *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages* for additional information.

Chip Information

TRANSISTOR COUNT: 1918

PROCESS: SiGe Bipolar

Pin Configuration



Package Information

For the latest package outline information, go to www.maxim-ic.com/packages.

PART	PACKAGE TYPE	PACKAGE CODE
MAX3942ETG	24 Thin QFN (4mm x 4mm x 0.8mm)	T2444-1

Revision History

Pages changed at Rev 1: 1, 2, 10.

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