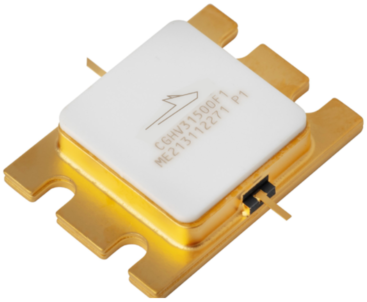
CGHV31500F1

2.7 – 3.1 GHz, 500 W GaN HEMT



Package Type: 440226
PN: CGHV31500F1

Description

Wolfspeed's CGHV31500F1 is a gallium nitride (GaN) high electron mobility transistor (HEMT) designed specifically with high efficiency and high gain for the 2.7 - 3.1 GHz S-Band radar band. The device has been developed with long pulse capability to meet the developing trends in radar architectures. The transistor is matched to 50-ohms on the input and 50-ohms on the output. The CGHV31500F1 is based on Wolfspeed's high power density 50 V, 0.4 µm GaN on Silicon Carbide (SiC) manufacturing process. The transistor is supplied in a ceramic/metal flange package.

Features

- P_{SAT}: 500W
- DE: >65%
- LSG: 13 dB

Note: Features are typical performance across frequency under 25°C operation. Please reference performance charts for additional details.

Applications

- Civil and Military Pulsed Radar Amplifiers

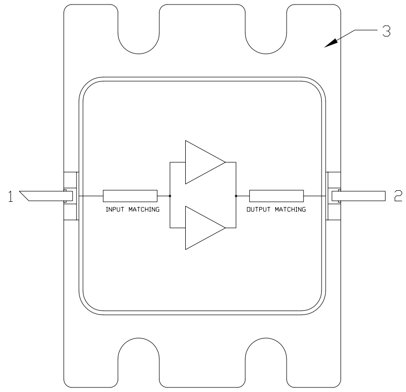


Figure 1: Functional Block Diagram

RoHS compliant

4600 Silicon Drive | Durham, NC 27703 | Tel: +1.919.313.5300

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units	Conditions
Drain Voltage	V_D	50	V	25°C
Gate Voltage	V_G	-10, +2		
Drain Current	I_D	24	A	
Gate Current	I_G	80	mA	25°C
Input Power	P_{IN}	48	dBm	
Dissipated Power	P_{DISS}	418	W	85°C
Storage Temperature	T_{STG}	-55, +150	°C	
Mounting Temperature	T_J	320		30 seconds
Junction Temperature		225		MTTF > 1e6 Hours
Output Mismatch Stress	VSWR	5:1	Ψ	
PulseWidth	PW	2000	µs	
Duty Cycle	DC	20	%	

Recommended Operating Conditions

Parameter	Symbol	Rating	Units	Conditions
Drain Voltage	V_D	50	V	
Gate Voltage	V_G	-2.7		
Drain Current	I_{DQ}	500	mA	
Input Power	P_{IN}	46	dBm	
Case Temperature	T_{CASE}	-40 to 75	°C	2mS, DC = 20%

RF Specifications

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500 mA, PW = 2000 µs, DC = 20%, T_{BASE} = +25 °C

Parameter	Units	Frequency	Min	Typical	Max	Conditions
Frequency	GHz	—	-2.7	—	3.1	
Output Power	dBm	2.7 GHz	—	57.0	—	P_{IN} = 46 dBm
		2.9 GHz	—	57.9	—	
		3.1 GHz	—	57.0	—	
Drain Efficiency	%	2.7 GHz	—	63	—	
		2.9 GHz	—	71	—	
		3.1 GHz	—	61	—	
LSG	dB	2.7 GHz	—	11.0	—	
		2.9 GHz	—	11.9	—	
		3.1 GHz	—	11.0	—	
Small-Signal		—	—	14.5	—	P_{IN} = -20 dBm
Input Return		—	—	-15	—	
Output Return		—	—	-6	—	

Large Signal Performance Versus Temperature – Short Pulse

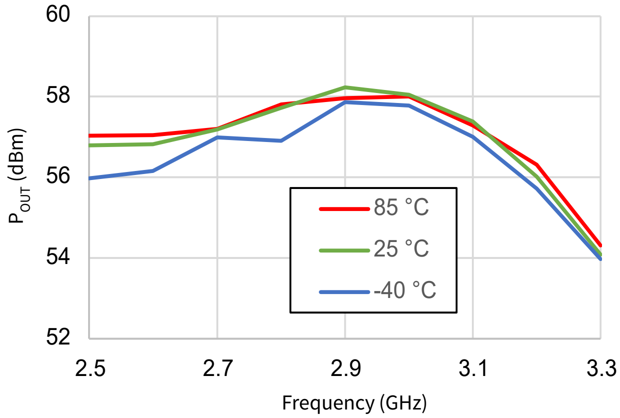


Figure 2. P_{OUT} v. Frequency v. Temperature

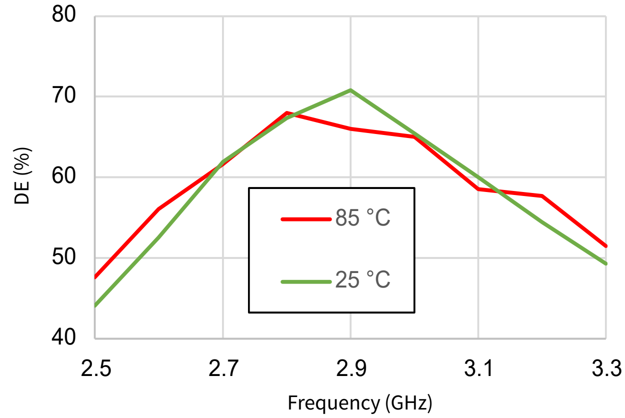


Figure 3. DE v. Frequency v. Temperature

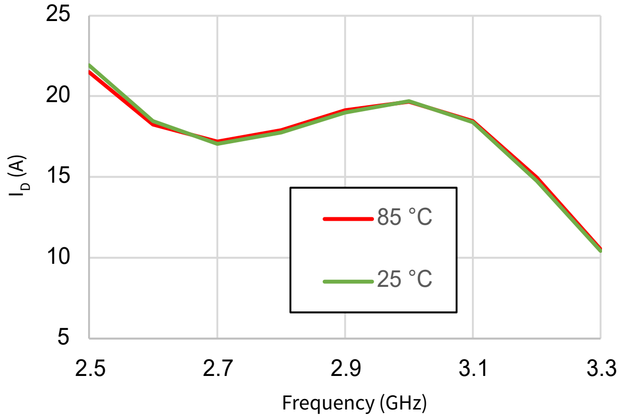


Figure 4. I_D v. Frequency v. Temperature

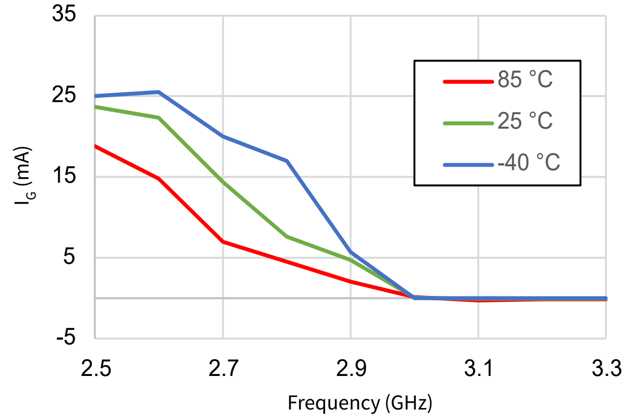


Figure 5. I_G v. Frequency v. Temperature

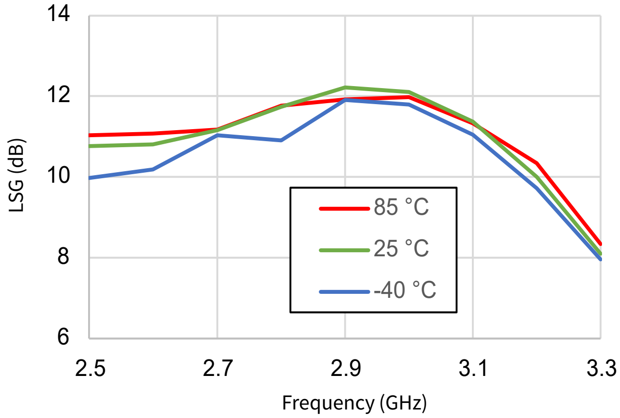


Figure 6. LSG v. Frequency v. Temperature

Large Signal Performance Versus V_D – Short Pulse

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500 mA, PW = 100µs, DC = 10%, P_{IN} = 46 dBm, T_{BASE} = 25°C, Frequency = 2.9 GHz

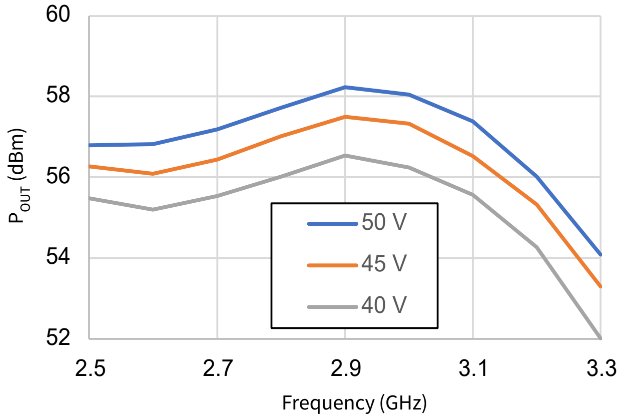


Figure 7. P_{OUT} v. Frequency v. V_D

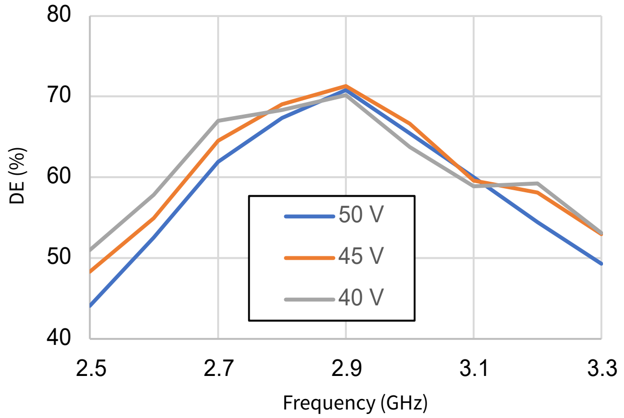


Figure 8. DE v. Frequency v. V_D

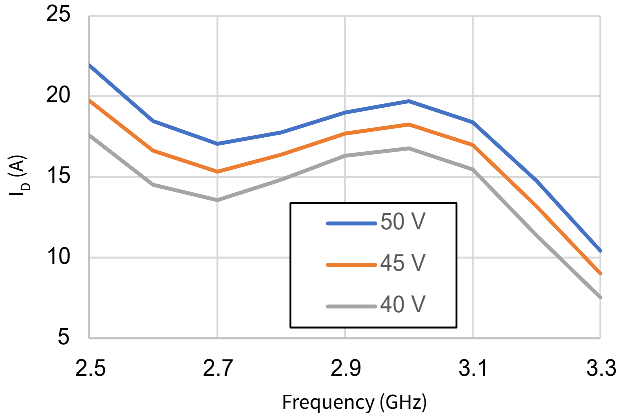


Figure 9. I_D v. Frequency v. V_D

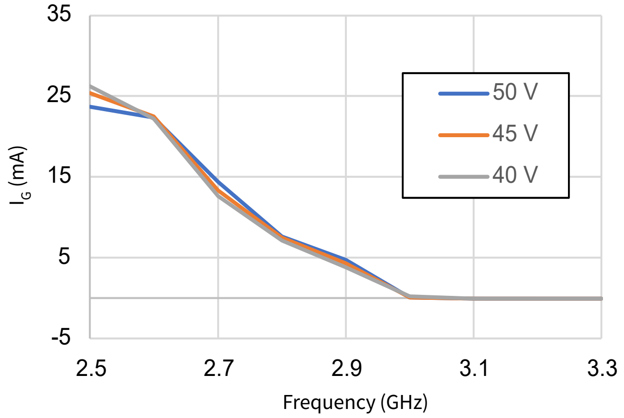


Figure 10. I_G v. Frequency v. V_D

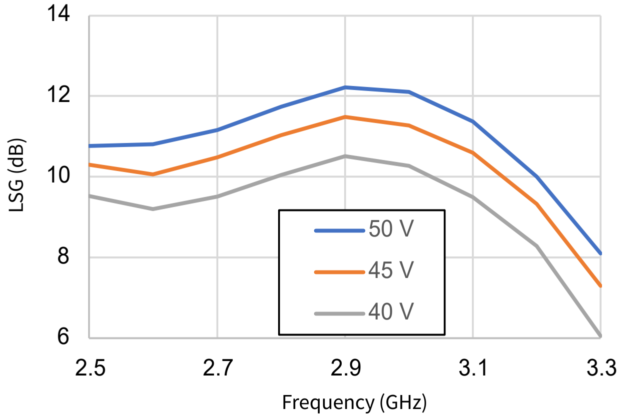


Figure 11. LSG v. Frequency v. V_D

Large Signal Performance Versus V_D – Short Pulse

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500 mA, PW = 100µs, DC = 10%, P_{IN} = 46 dBm, T_{BASE} = 25°C, Frequency = 2.9 GHz

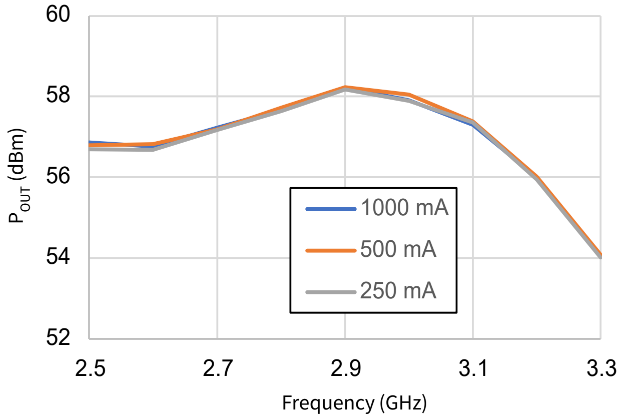


Figure 12. P_{OUT} v. Frequency v. I_{DQ}

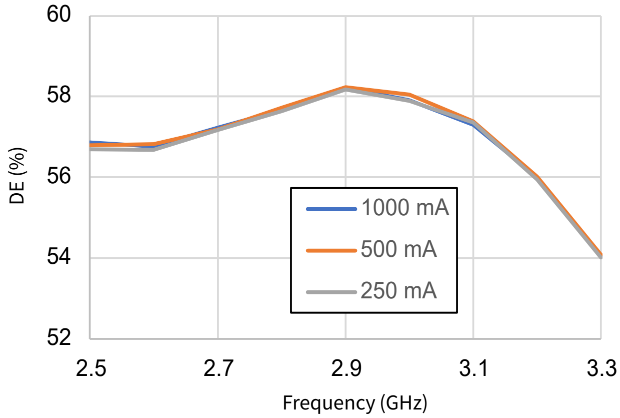


Figure 13. DE v. Frequency v. I_{DQ}

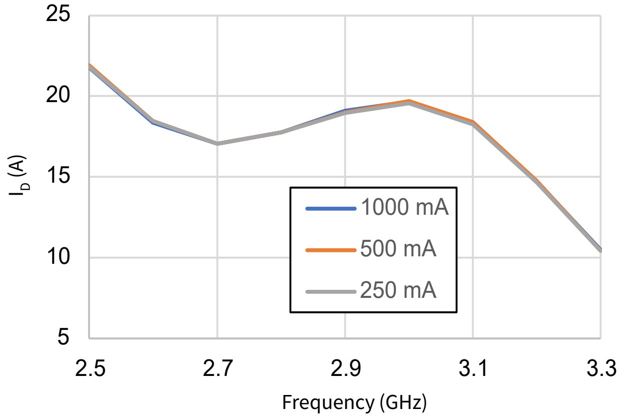


Figure 14. I_D v. Frequency v. I_{DQ}

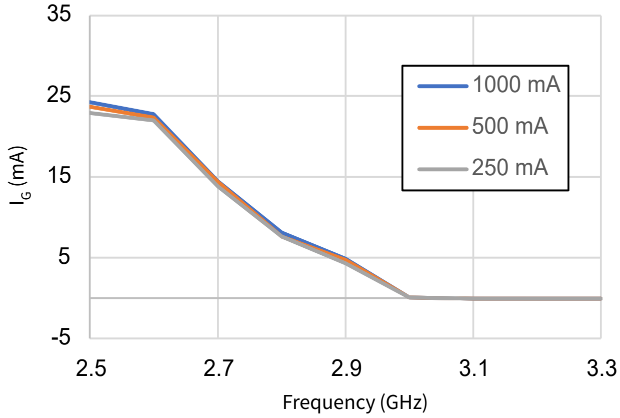


Figure 15. I_G v. Frequency v. I_{DQ}

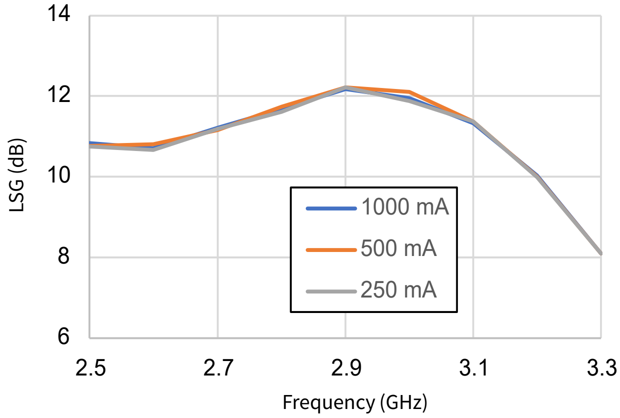


Figure 16. LSG v. Frequency v. I_{DQ}

Drive-up Versus Frequency – Short Pulse

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500 mA, PW = 100µs, DC = 10%, P_{IN} = 46 dBm, T_{BASE} = 25°C, Frequency = 2.9 GHz

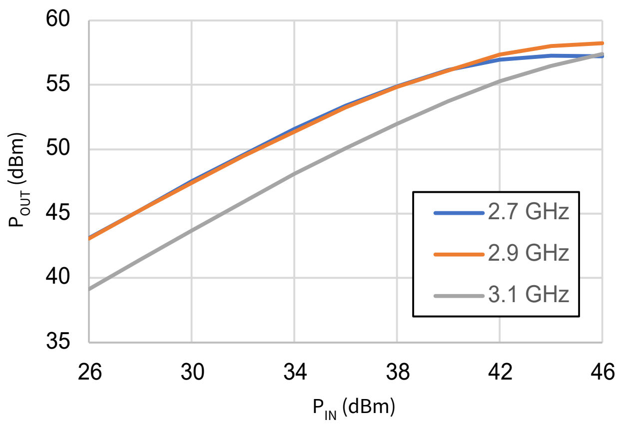


Figure 17. P_{OUT} v. P_{IN} v. Frequency

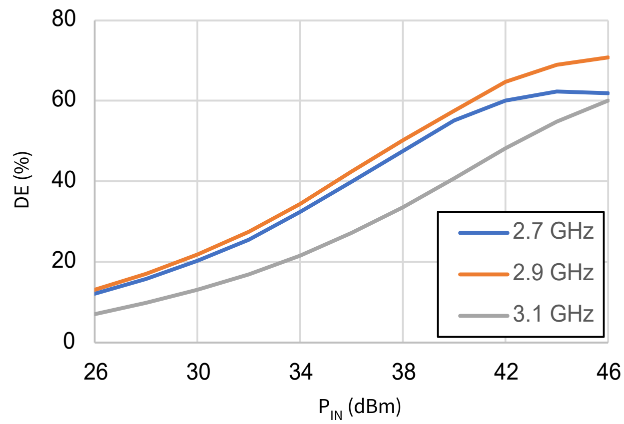


Figure 18. DE v. P_{IN} v. Frequency

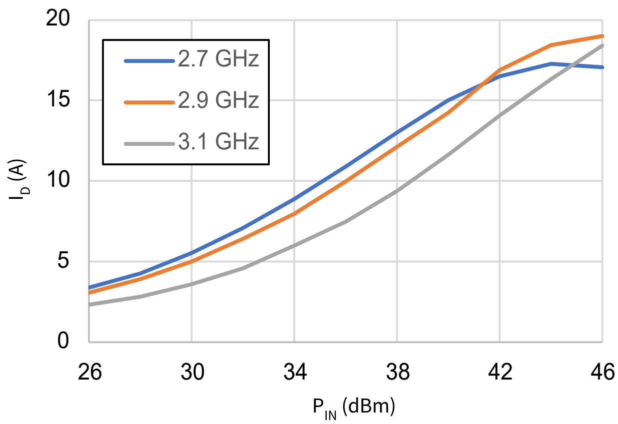


Figure 19. I_D v. P_{IN} v. Frequency

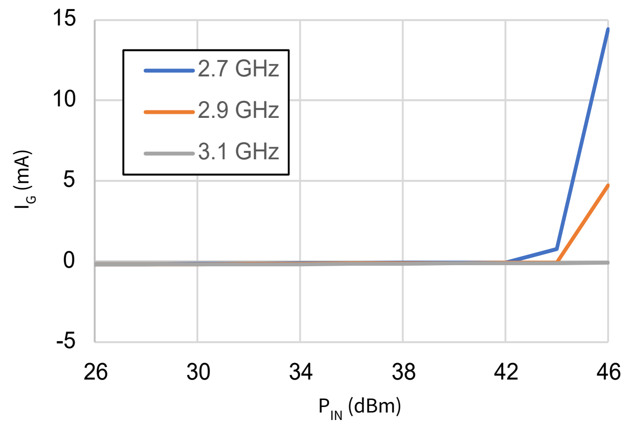


Figure 20. I_G v. P_{IN} v. Frequency

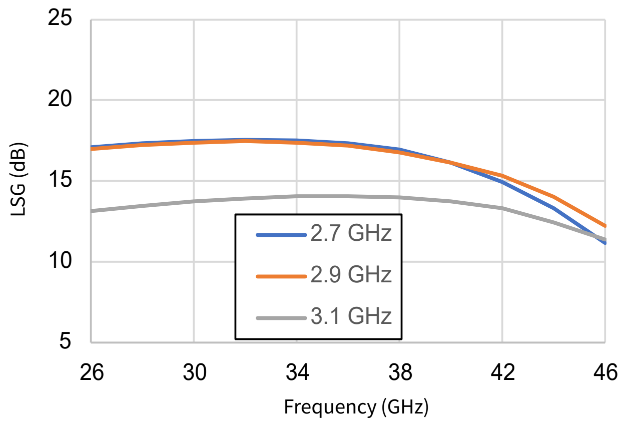


Figure 21. Gain v. P_{IN} v. Frequency

Drive-up Versus Temperature – Short Pulse

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500 mA, PW = 100µs, DC = 10%, P_{IN} = 46 dBm, T_{BASE} = 25°C, Frequency = 2.9 GHz

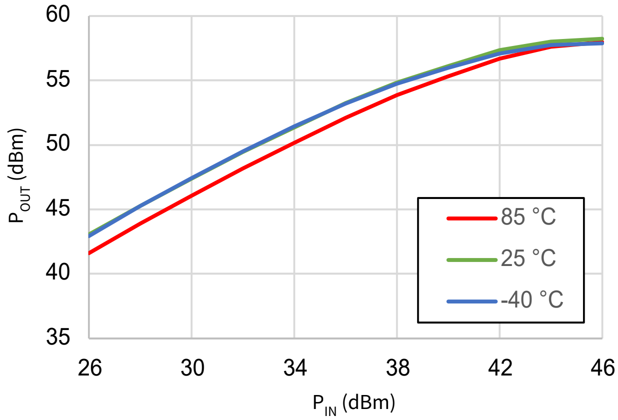


Figure 22. P_{OUT} v. P_{IN} v. Temperature

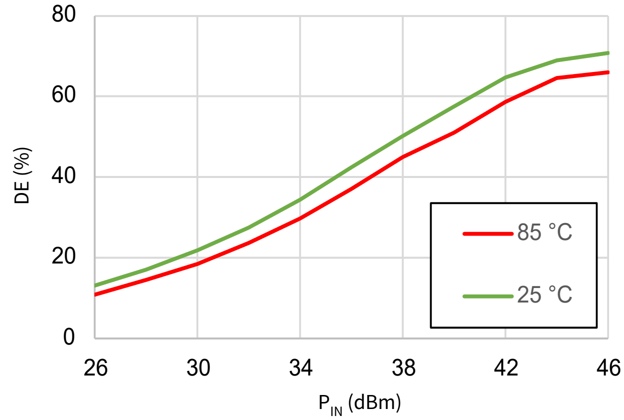


Figure 23. DE v. P_{IN} v. Temperature

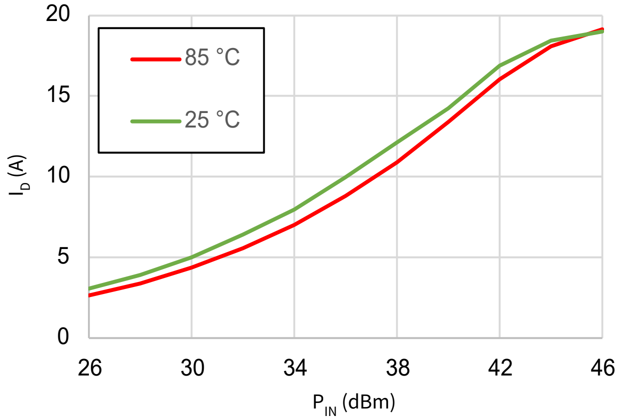


Figure 24. I_D v. P_{IN} v. Temperature

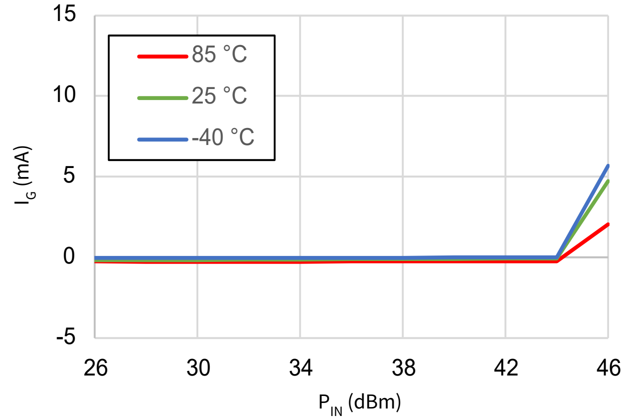


Figure 25. I_G v. P_{IN} v. Temperature

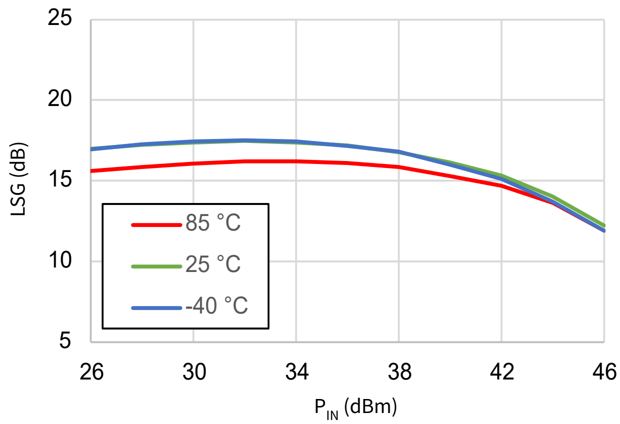


Figure 26. Gain v. P_{IN} v. Temperature

Drive-up Versus V_D – Short Pulse

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500 mA, PW = 100µs, DC = 10%, P_{IN} = 46 dBm, T_{BASE} = 25°C, Frequency = 2.9 GHz

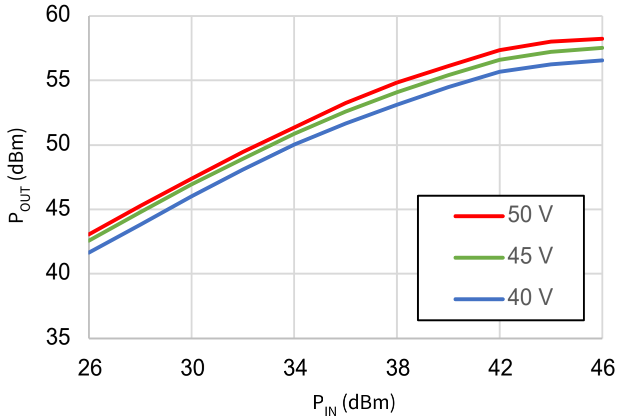


Figure 27. P_{OUT} v. P_{IN} v. V_D

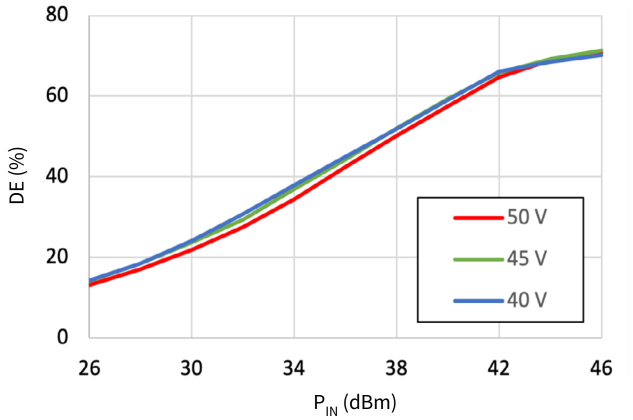


Figure 28. DE v. P_{IN} v. V_D

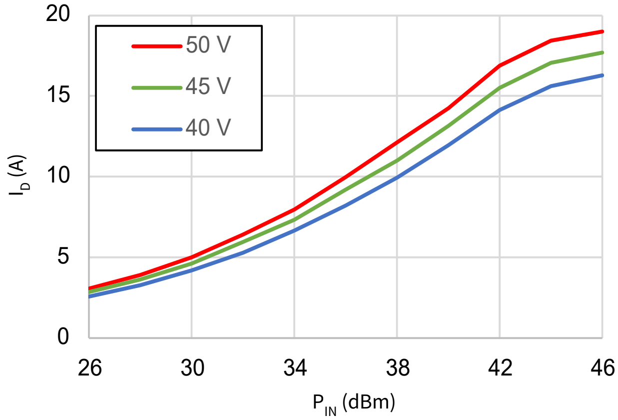


Figure 29. I_D v. P_{IN} v. V_D

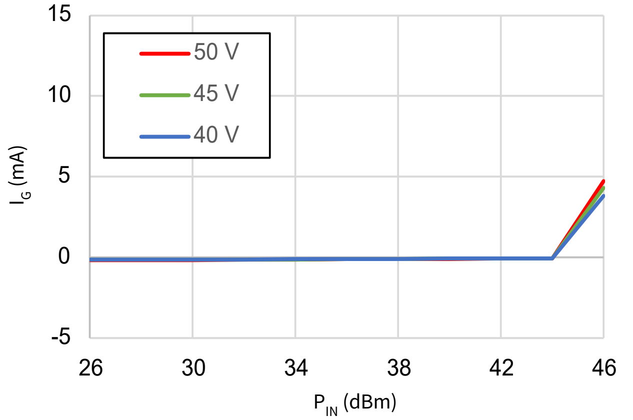


Figure 30. I_G v. P_{IN} v. V_D

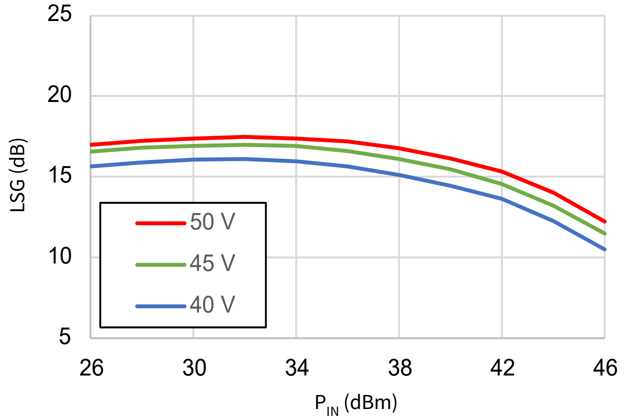


Figure 31. Gain v. P_{IN} v. V_D

Drive up Versus I_{DQ} – Short Pulse

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500 mA, PW = 100µs, DC = 10%, P_{IN} = 46 dBm, T_{BASE} = 25°C, Frequency = 2.9 GHz

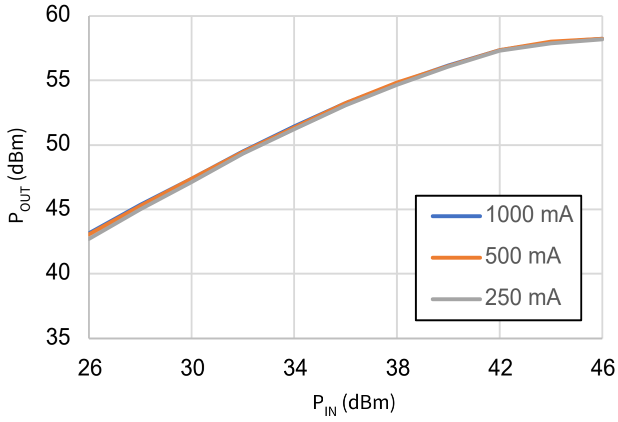


Figure 32. P_{OUT} v. P_{IN} v. I_{DQ}

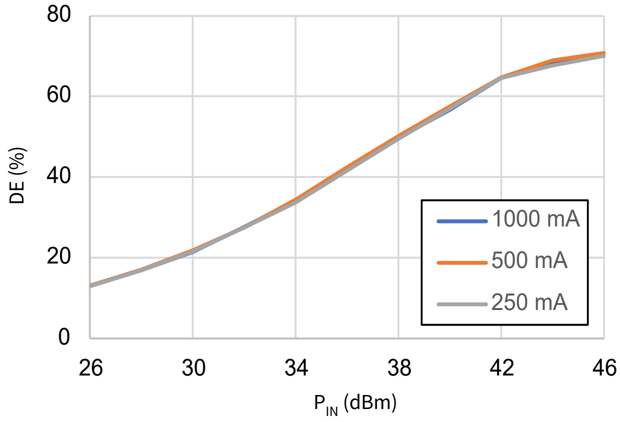


Figure 33. DE v. P_{IN} v. I_{DQ}

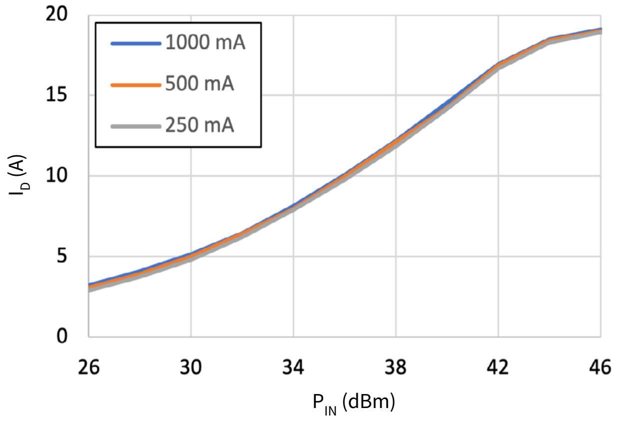


Figure 34. I_D v. P_{IN} v. I_{DQ}

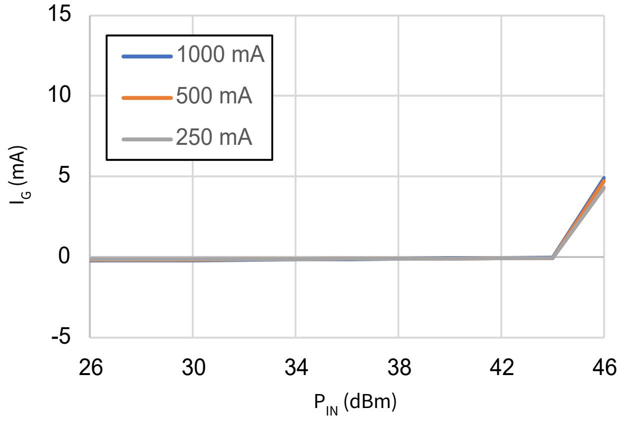


Figure 35. I_G v. P_{IN} v. I_{DQ}

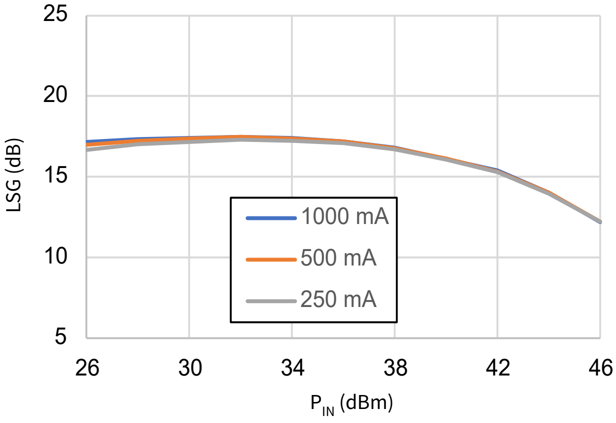


Figure 36. Gain v. P_{IN} v. I_{DQ}

Large Signal Performance Versus Temperature – Short Pulse

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500 mA, PW = 100µs, DC = 10%, P_{IN} = 46 dBm, T_{BASE} = 25°C, Frequency = 2.9 GHz

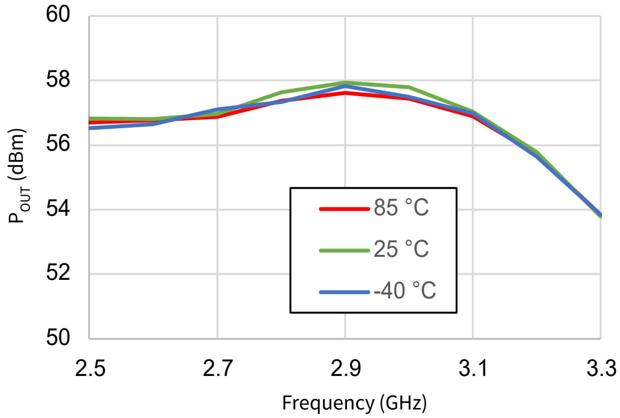


Figure 37. P_{OUT} v. Frequency v. Temperature

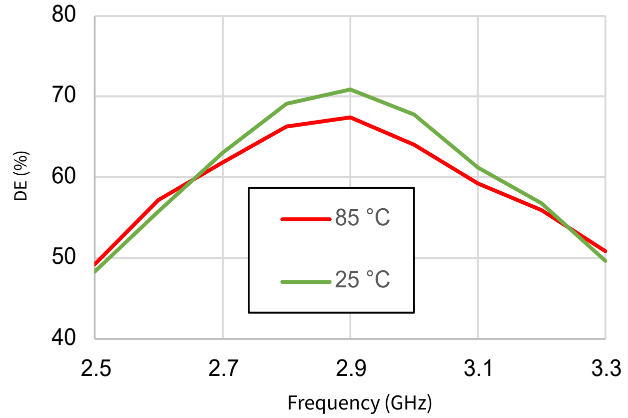


Figure 38. DE v. Frequency v. Temperature

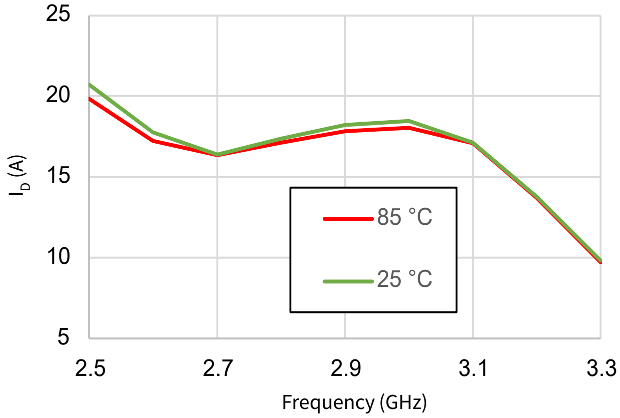


Figure 39. I_D v. Frequency v. Temperature

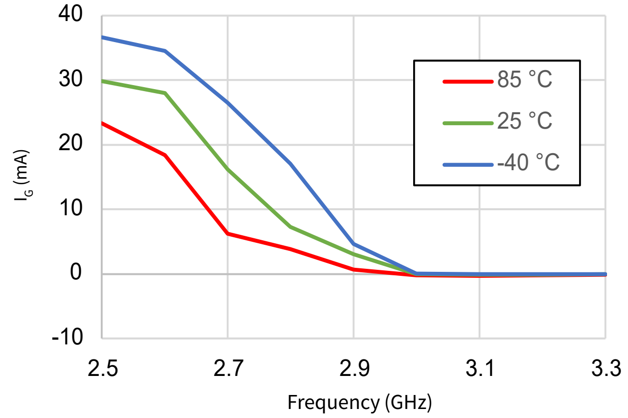


Figure 40. I_G v. Frequency v. Temperature

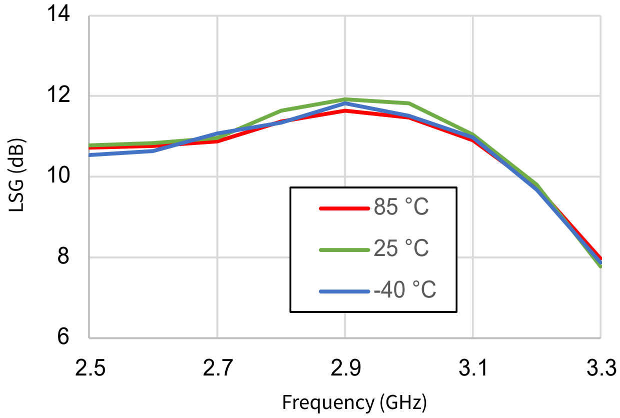


Figure 41. LSG v. Frequency v. Temperature

Large Signal Performance Versus V_D – Short Pulse

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500 mA, PW = 100µs, DC = 10%, P_{IN} = 46 dBm, T_{BASE} = 25°C, Frequency = 2.9 GHz

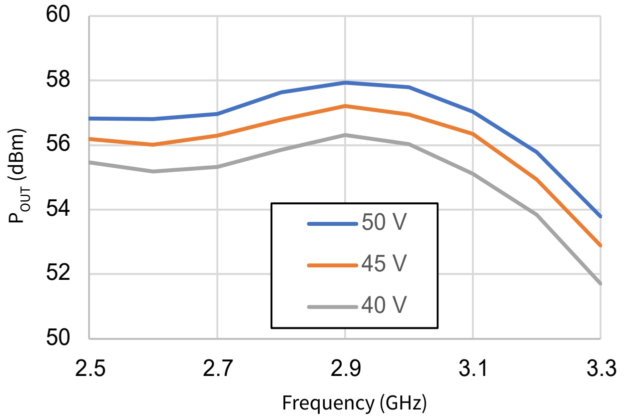


Figure 42. P_{OUT} v. Frequency v. V_D

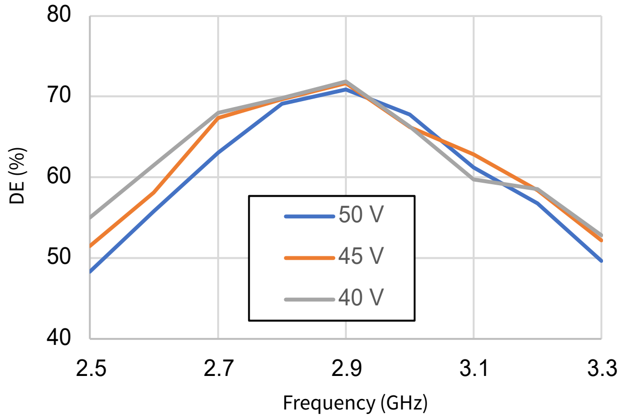


Figure 43. DE v. Frequency v. V_D

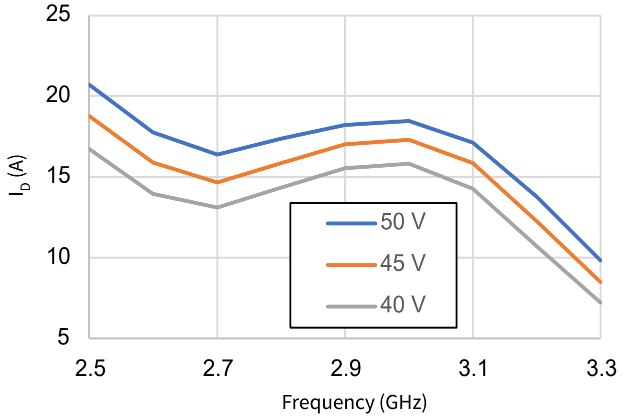


Figure 44. I_D v. Frequency v. V_D

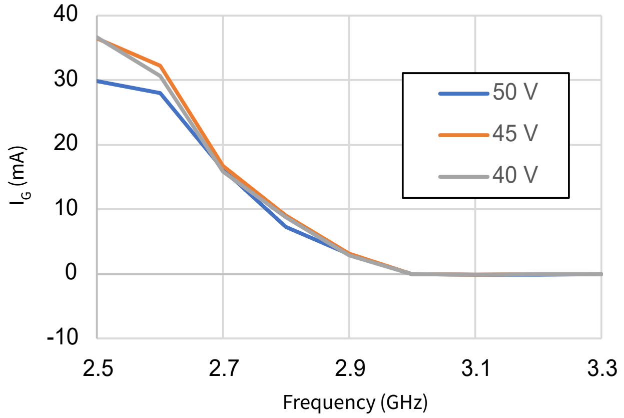


Figure 45. I_G v. Frequency v. V_D

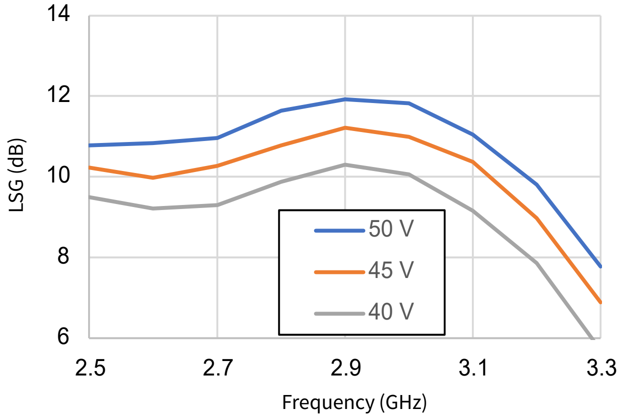


Figure 46. LSG v. Frequency v. V_D

Large Signal Performance Versus I_{DQ} – Short Pulse

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500 mA, PW = 100µs, DC = 10%, P_{IN} = 46 dBm, T_{BASE} = 25°C, Frequency = 2.9 GHz

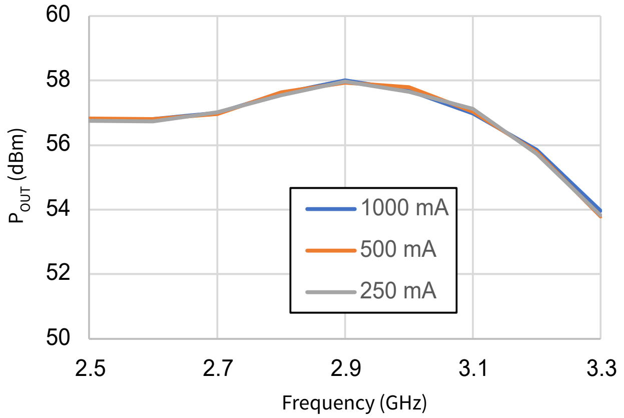


Figure 47. P_{OUT} v. Frequency v. I_{DQ}

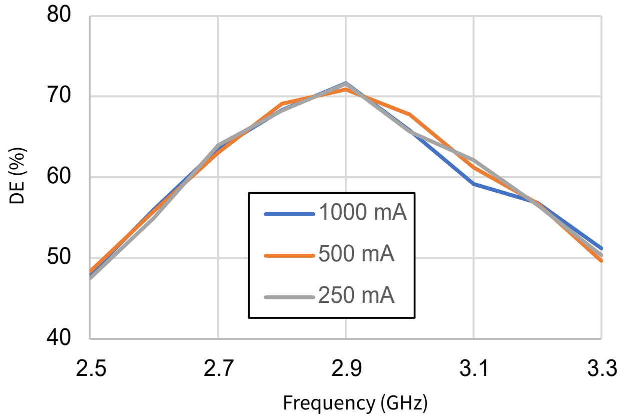


Figure 48. DE v. Frequency v. I_{DQ}

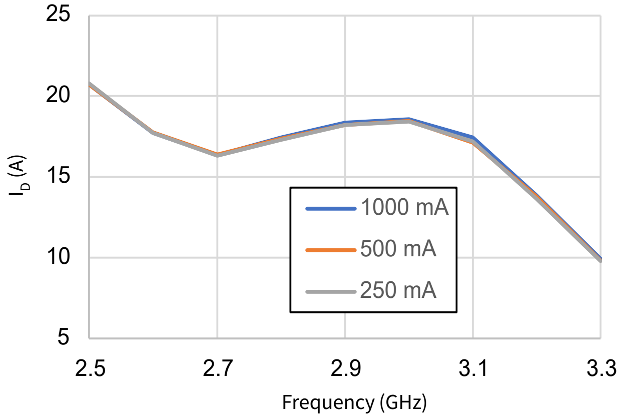


Figure 49. I_D v. Frequency v. I_{DQ}

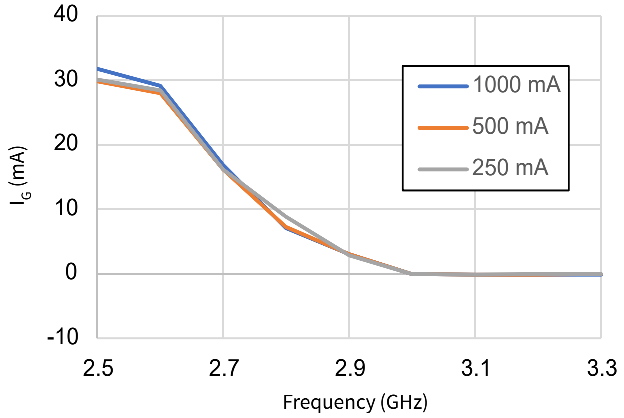


Figure 50. I_G v. Frequency v. I_{DQ}

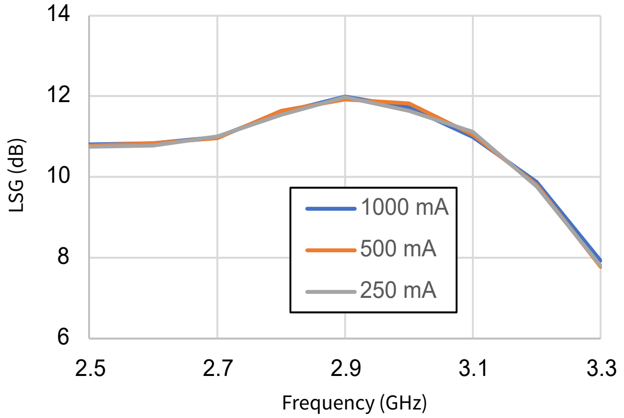


Figure 51. LSG v. Frequency v. I_{DQ}

Drive-up Versus Frequency – Short Pulse

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500 mA, PW = 100µs, DC = 10%, P_{IN} = 46 dBm, T_{BASE} = 25°C, Frequency = 2.9 GHz

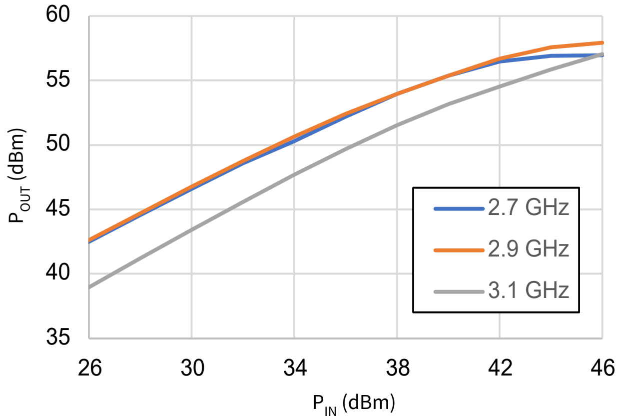


Figure 52. P_{OUT} v. P_{IN} v. Frequency

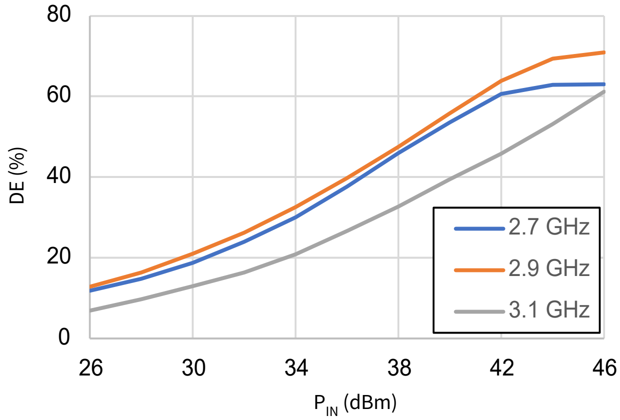


Figure 53. DE v. P_{IN} v. Frequency

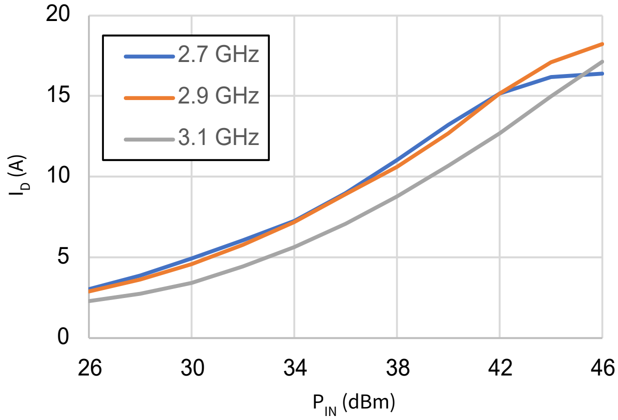


Figure 54. I_D v. P_{IN} v. Frequency

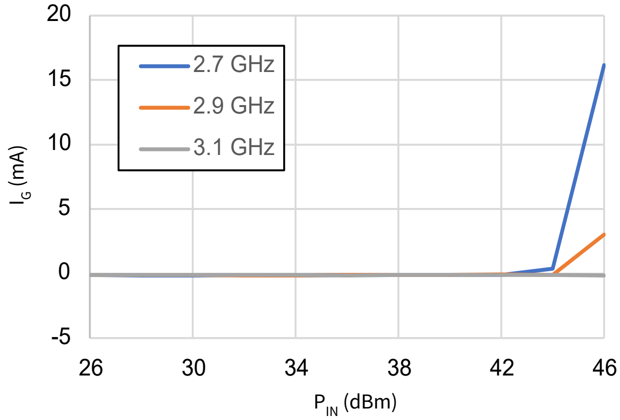


Figure 55. I_G v. P_{IN} v. Frequency

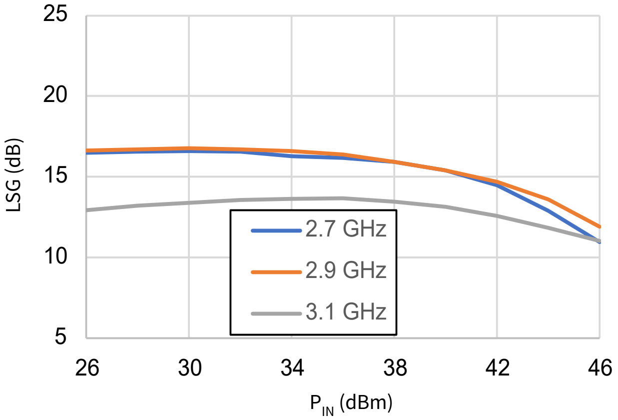


Figure 56. Gain v. P_{IN} v. Frequency

Drive-up Versus Temperature – Short Pulse

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500 mA, PW = 100µs, DC = 10%, P_{IN} = 46 dBm, T_{BASE} = 25°C, Frequency = 2.9 GHz

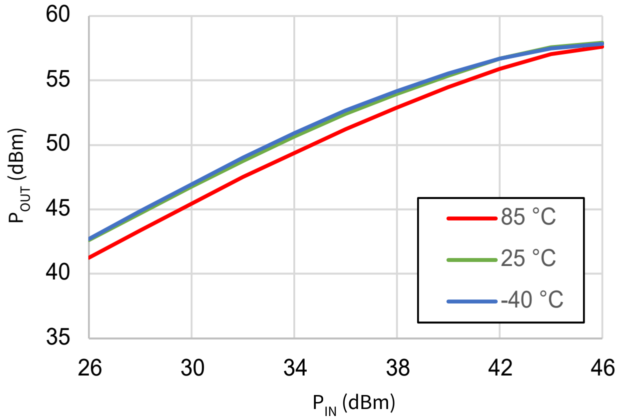


Figure 57. P_{OUT} v. P_{IN} v. Temperature

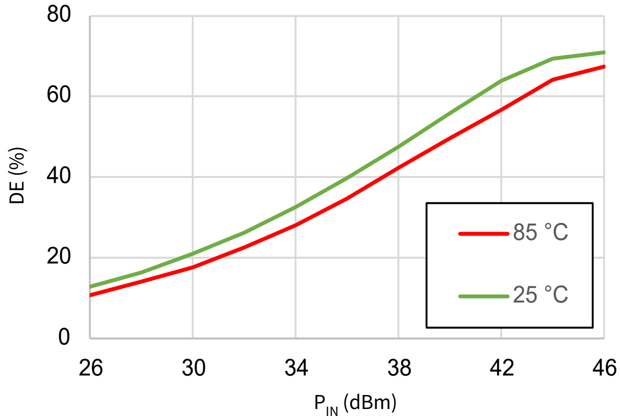


Figure 58. DE v. P_{IN} v. Temperature

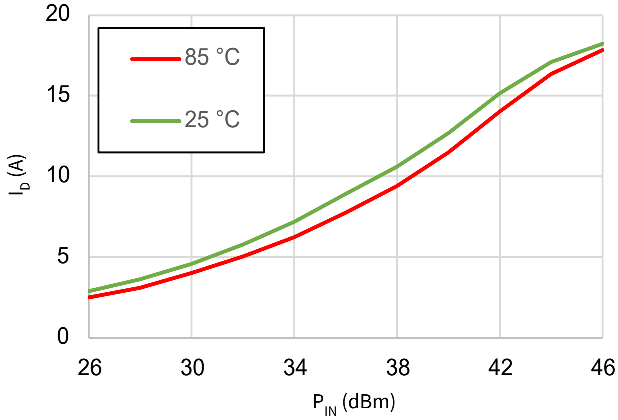


Figure 59. I_D v. P_{IN} v. Temperature

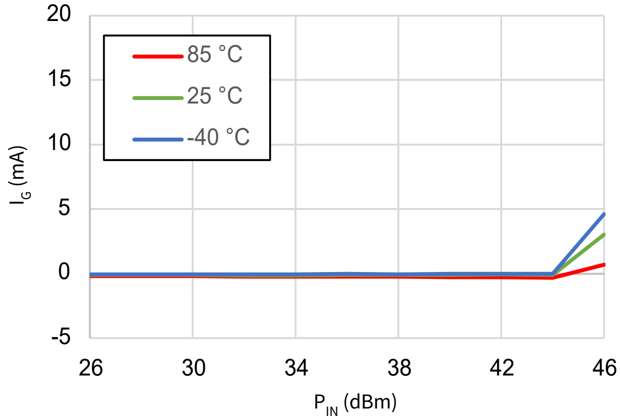


Figure 60. I_G v. P_{IN} v. Temperature

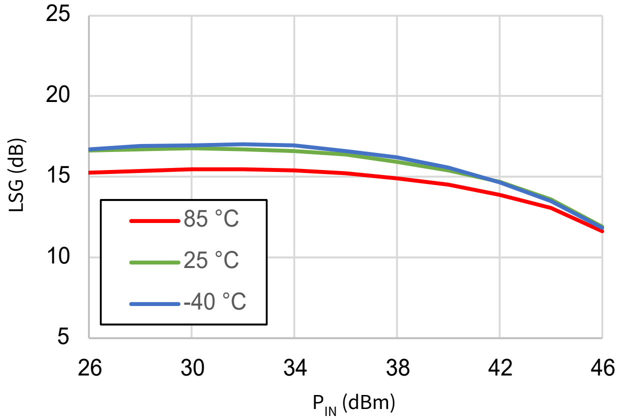


Figure 61. Gain v. P_{IN} v. Temperature

Drive-up Versus V_D – Long Pulse

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500 mA, PW = 2000µs, DC = 20%, P_{IN} = 46 dBm, T_{BASE} = 25°C, Frequency = 2.9 GHz

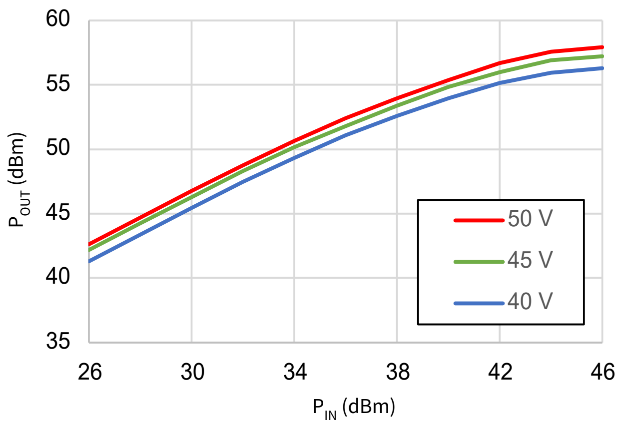


Figure 62. P_{OUT} v. P_{IN} v. V_D

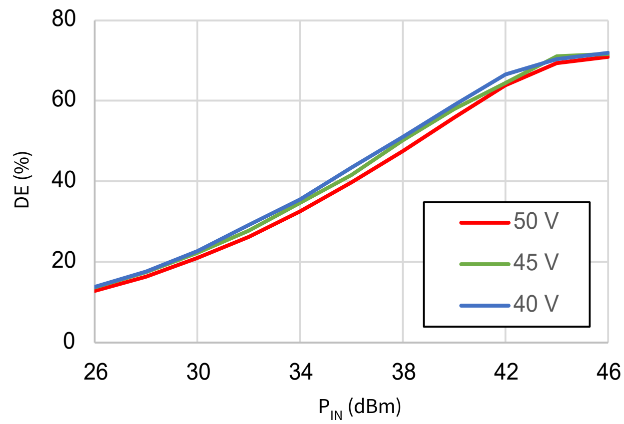


Figure 63. DE v. P_{IN} v. V_D

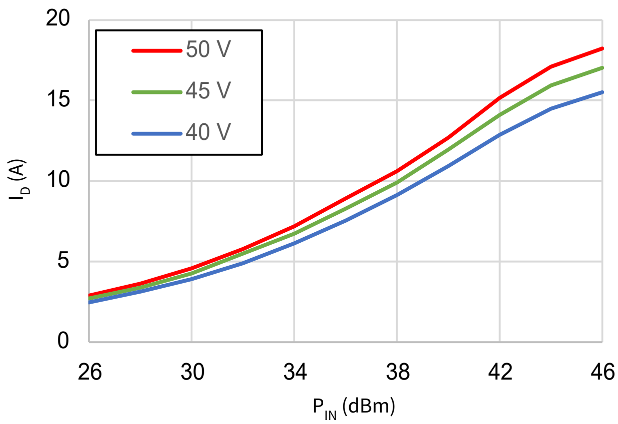


Figure 64. I_D v. P_{IN} v. V_D

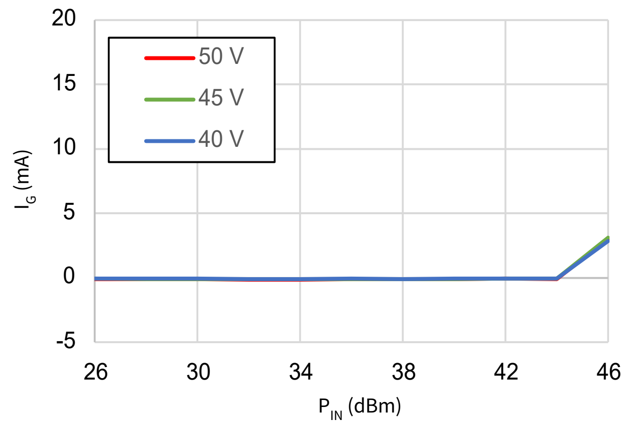


Figure 65. I_G v. P_{IN} v. V_D

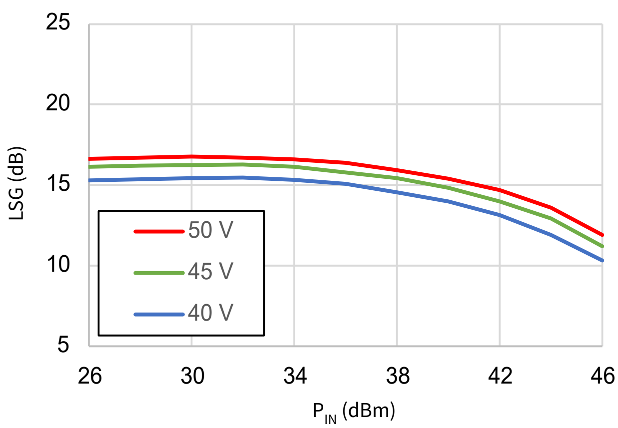


Figure 66. Gain v. P_{IN} v. V_D

Drive-up Versus V_D – Long Pulse

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500 mA, PW = 2000µs, DC = 20%, P_{IN} = 46 dBm, T_{BASE} = 25°C, Frequency = 2.9 GHz

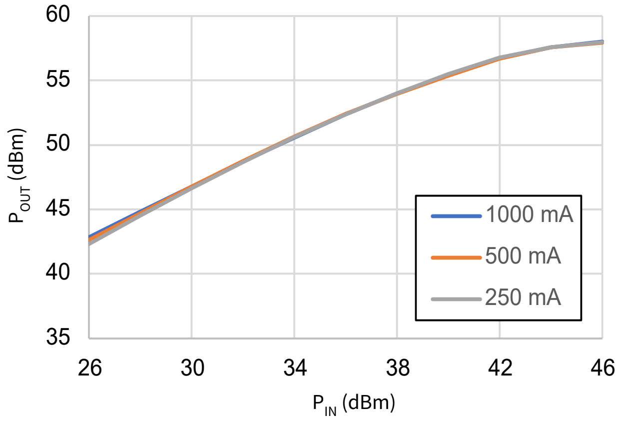


Figure 67. P_{OUT} v. P_{IN} v. I_{DQ}

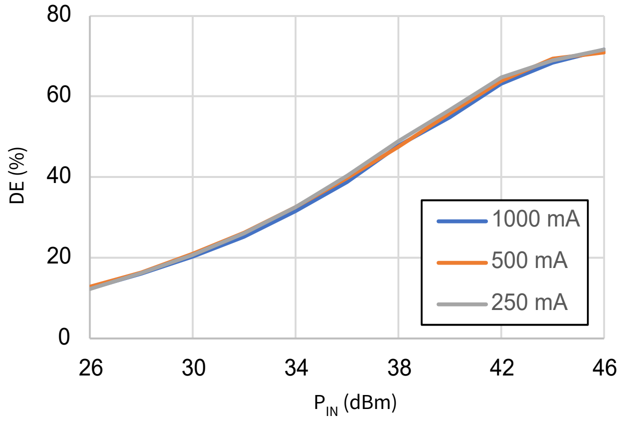


Figure 68. DE v. P_{IN} v. I_{DQ}

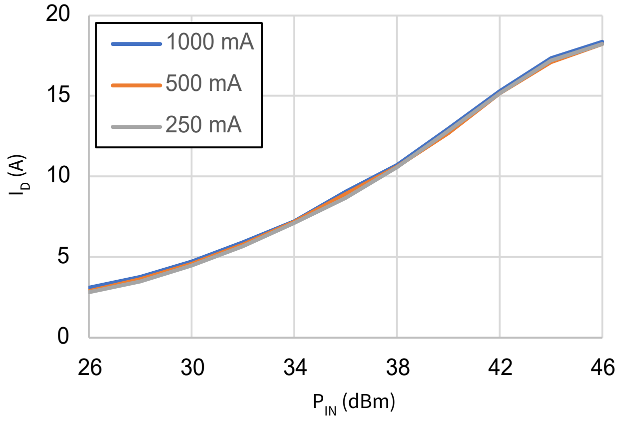


Figure 69. I_D v. P_{IN} v. I_{DQ}

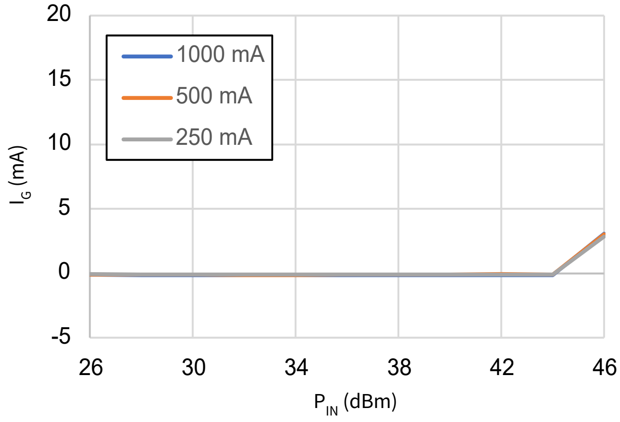


Figure 70. I_G v. P_{IN} v. I_{DQ}

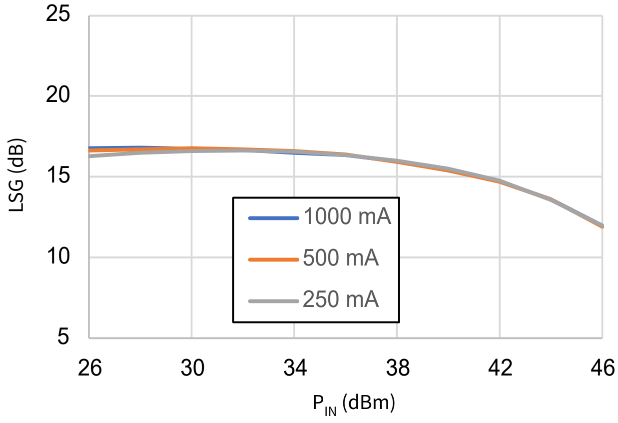


Figure 71. Gain v. P_{IN} v. I_{DQ}

Small Signal v. Temperature and Bias

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500 mA, P_{IN} = -20 dBm, T_{BASE} = 25°C

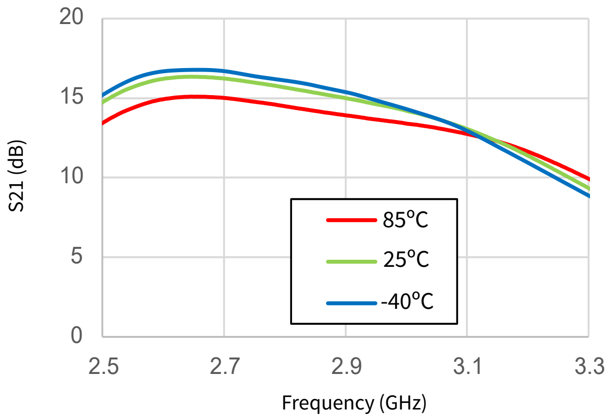


Figure 72. S21 v. Frequency v. Temperature

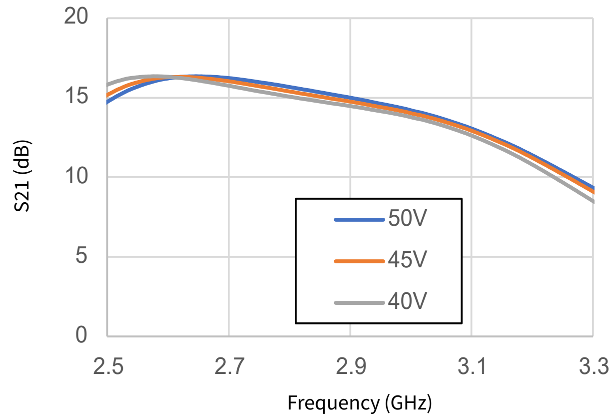


Figure 73. S21 v. Frequency v. V_D

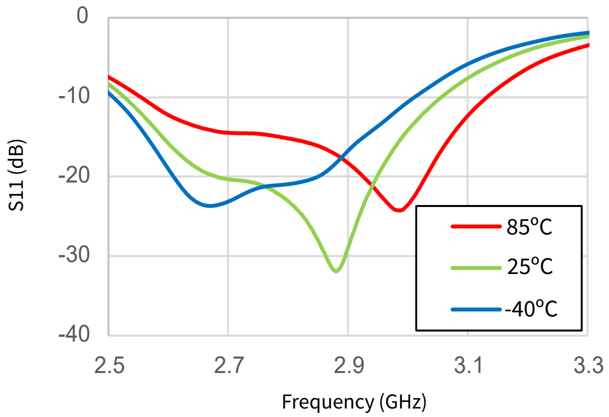


Figure 74. S11 v. Frequency v. Temperature

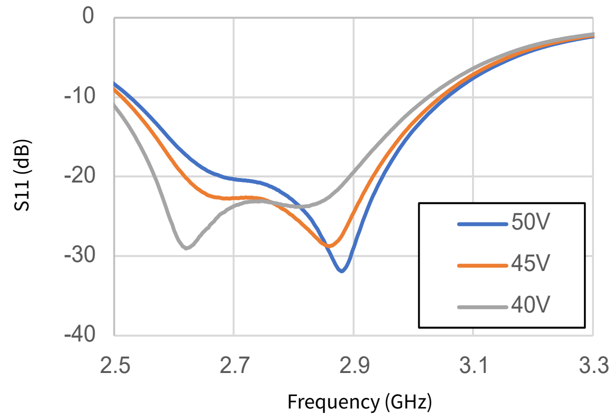


Figure 75. S11 v. Frequency v. V_D

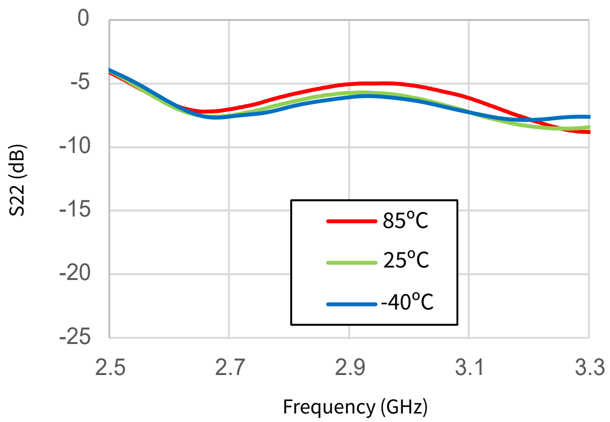


Figure 76. S22 v. Frequency v. Temperature

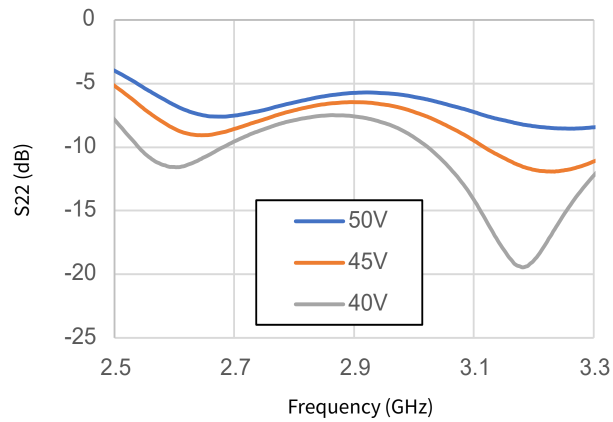


Figure 77. S22 v. Frequency v. V_D

Small Signal v. Bias

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500 mA, P_{IN} = -20 dBm, T_{BASE} = 25°C

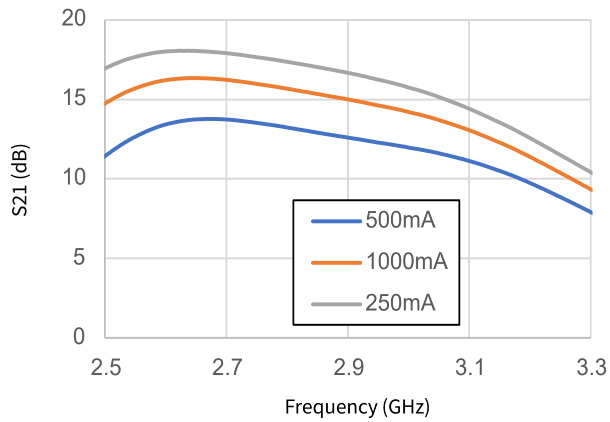


Figure 78. S21 v. Frequency v. I_{DQ}

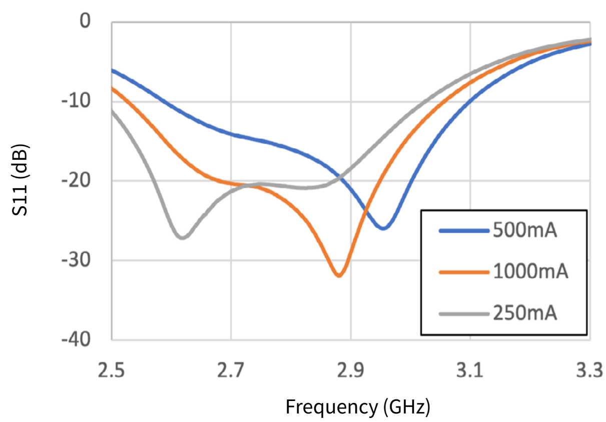


Figure 79. S11 v. Frequency v. I_{DQ}

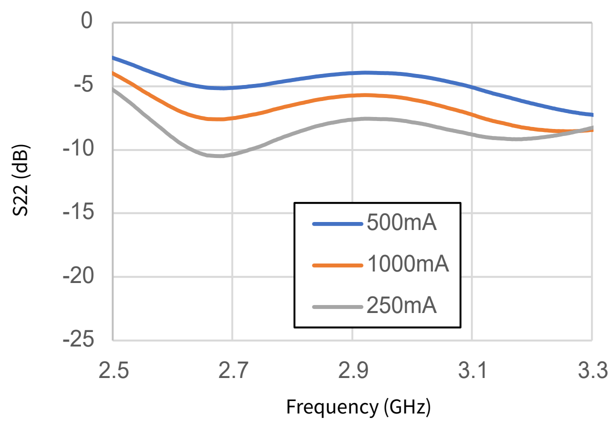


Figure 80. S22 v. Frequency v. I_{DQ}

Harmonics

Test conditions unless otherwise noted: V_D = 50 V, I_{DQ} = 500mA, PW = 2000µs, DC = 20%, P_{IN} = 46dBm, Frequency 1= 2.7 GHz (F1), Frequency 2 = 2.9 GHz (F2), Frequency 3 = 3.1 GHz (F3), T_{BASE} = 25°C

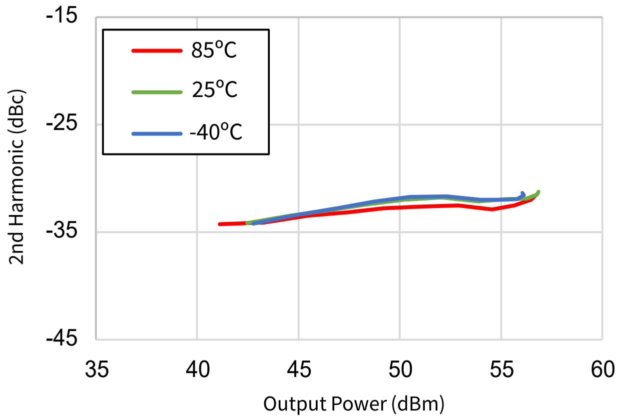


Figure 81. 2f v. P_{OUT} v. Temperature, F1

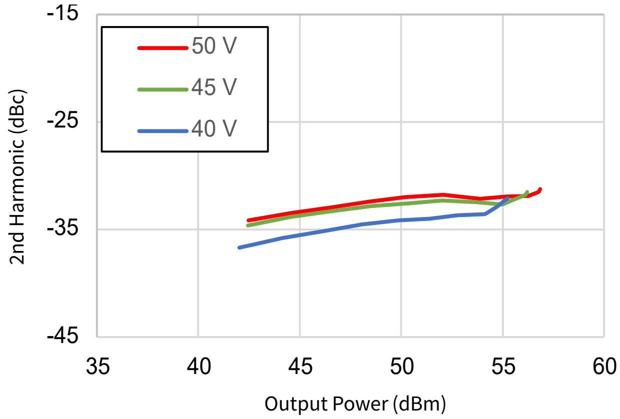


Figure 82. 2f v. P_{OUT} v. V_D, F1

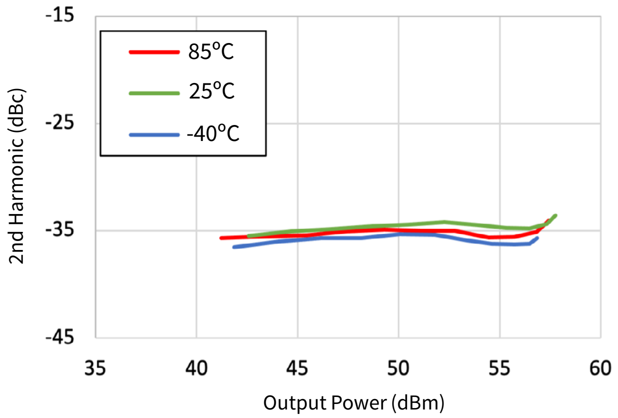


Figure 83. 2f v. P_{OUT} v. Temperature, F2

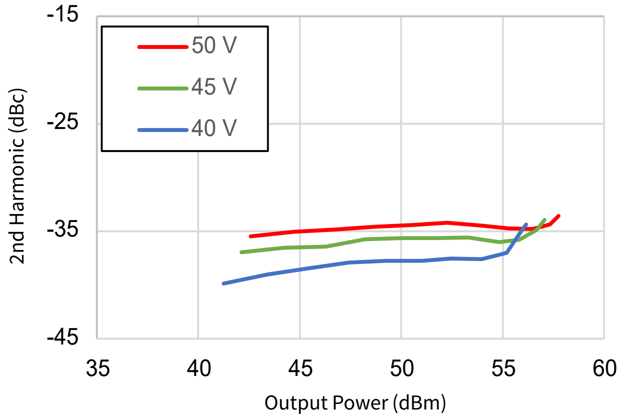


Figure 84. 2f v. P_{OUT} v. V_D, F2

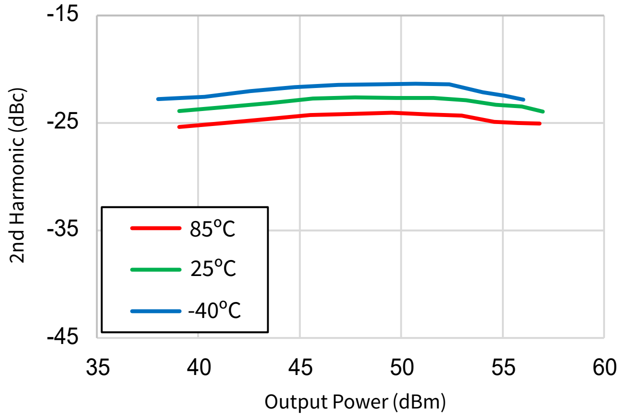


Figure 85. 2f v. P_{OUT} v. Temperature, F3

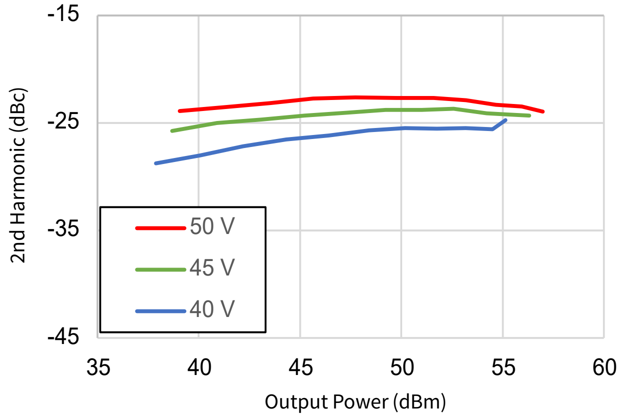
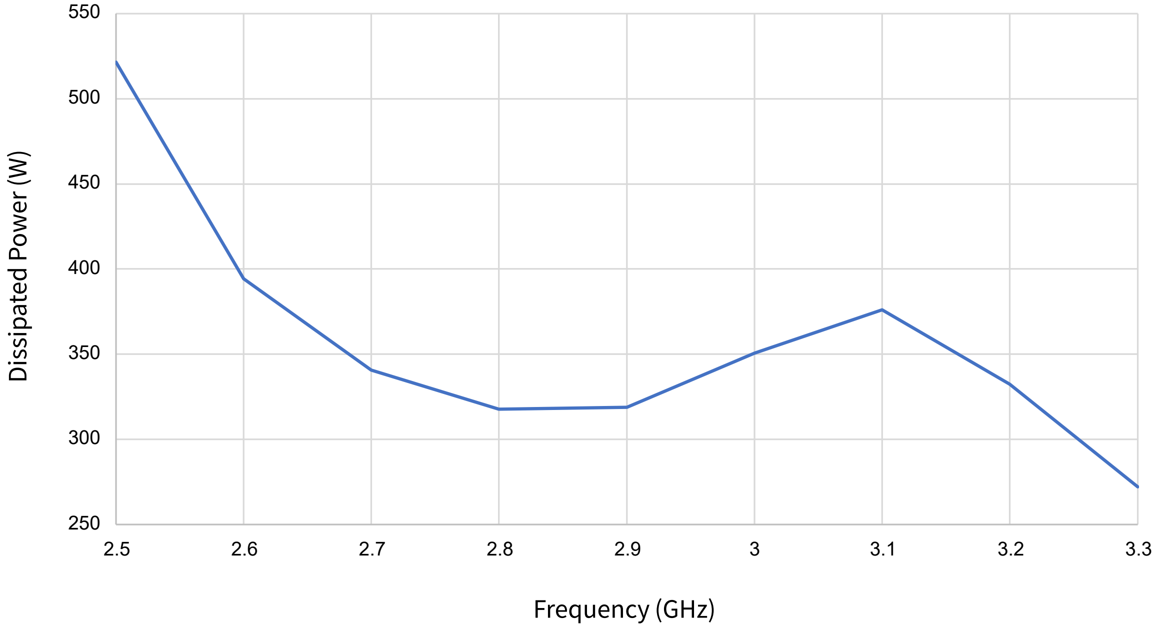


Figure 86. 2f v. P_{OUT} v. V_D, F3

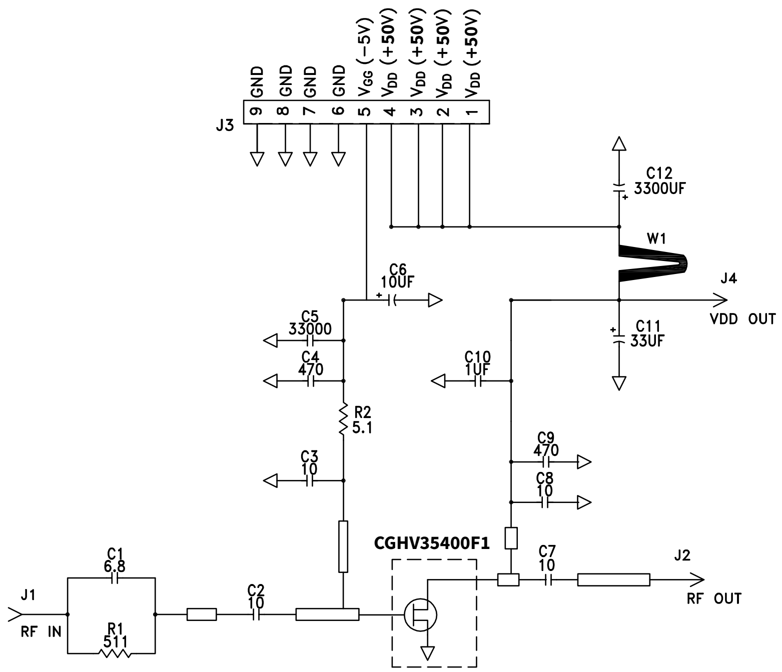
Thermal Information

Thermal Characteristics	Symbol	Value	Operating Conditions
Operating Junction Temperature	T_J	212	Freq = 2.9 GHz, V_D = 50 V, I_{DQ} = 500 mA, I_{DRIVE} = 18.2 A , P_{IN} = 46 dBm, P_{OUT} = 57.9 dBm, P_{DISS} = 319 W, T_{CASE} = 85°C, PW = 2000 µs, DC = 20%
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.4	

Power Dissipation v. Frequency (T_{CASE} = 85°C)



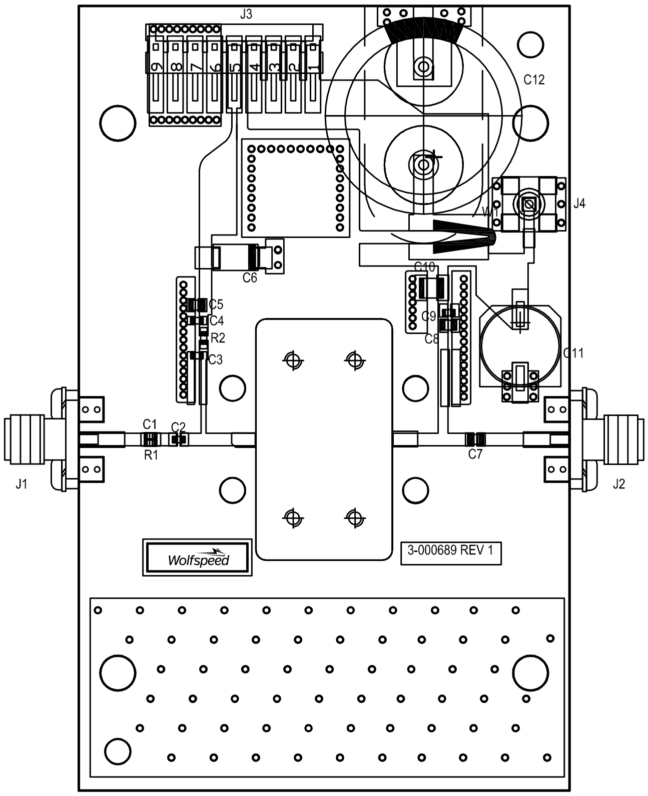
CGHV31500F1-AMP Evaluation Board Schematic



CGHV31500F1-AMP Bill of Materials

Designator	Description	Qty
R1	RES, 511 ohm, +/- 1%, 1/16W, 0603	1
R2	RES, 5.1 ohm, +/- 1%, 1/16W, 0603	1
C1	CAP, 6.8 pF, +/-0.25%, 250V, 0603	1
C2, C7, C8	CAP, 10.0 pF, +/-1%, 250V, 0805	3
C3	CAP, 10.0 pF, +/-5%, 250V, 0603	1
C4, C9	CAP, 470 pF, 5%, 100V, 0603, X	2
C5	CAP, 33000 pF, 0805, 100V, X7R	1
C6	CAP, 10 µF 16V TANTALUM	1
C10	CAP, 1.0 µF, 100V, 10%, X7R, 1210	1
C11	CAP, 33 µF, 20%, G CASE	1
C12	CAP, 3300 µF, +/-20%, 100V, ELECTROLYTIC	1
J1, J2	CONN, SMA, PANEL MOUNT JACK, FL	2
J3	HEADER, RT>PLZ, 0.1CEN LK 9POS	1
J4	CONNECTOR; SMB, Straight, JACK, SMD	1
W1	CABLE, 18 AWG, 4.2	1
	PCB, RO4350, 2.5 X 4.0 X 0.030	1
Q1	CGHV35400F1	1

CGHV31500F1-AMP Evaluation Board Assembly Drawing



Bias On Sequence

1. Ensure RF is turned-off
2. Apply pinch-off voltage of -5 V to the gate (V_G)
3. Apply nominal drain voltage (V_D)
4. Adjust Vg to obtain desired quiescent drain current (I_{DQ})
5. Apply RF

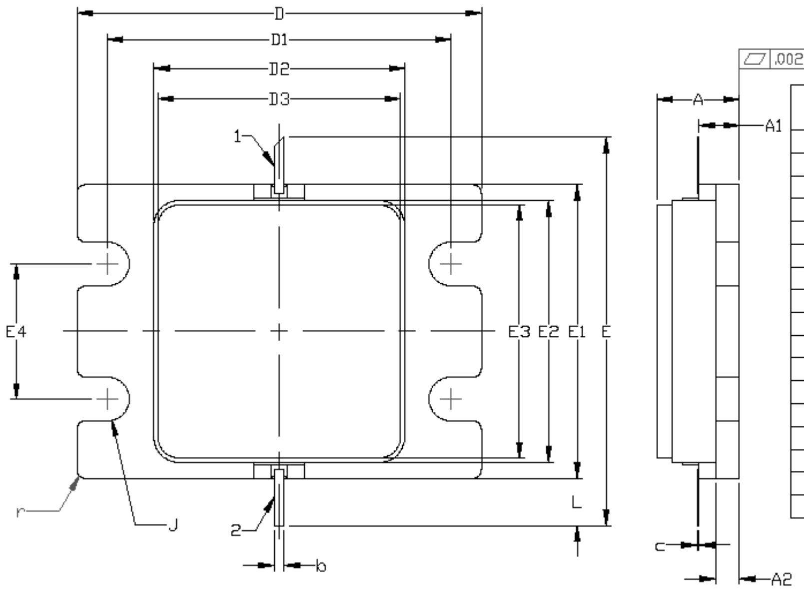
Bias Off Sequence

1. Turn RF off
2. Apply pinch-off to the gate (V_G=-5V)
3. Turn off drain voltage (V_D)
4. Turn off gate voltage (V_G)

Product Dimensions (Package 440226)

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. INTERPRET DRAWING IN ACCORDANCE WITH ANSI Y14.5M–2009
2. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF .020 BEYOND EDGE OF LID
3. LID MAY BE MISALIGNED TO THE BODY OF PACKAGE BY A MAXIMUM OF .008 IN ANY DIRECTION
4. ALL PLATED SURFACES ARE GOLD OVER NICKEL



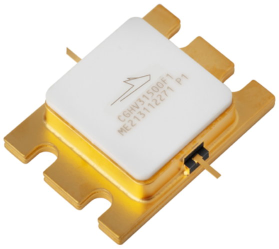
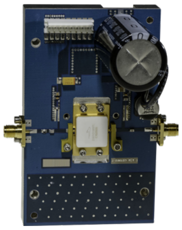
DIM	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.185	0.201	4.70	5.11	
A1	0.088	0.100	2.24	2.54	2x
A2	0.049	0.061	1.24	1.55	
b	0.022	0.026	0.56	0.66	2x
c	0.003	0.006	0.08	0.15	
D	0.935	0.955	23.75	24.26	
D1	0.797	0.809	20.24	20.55	2x
D2	0.581	0.593	14.76	15.06	
D3	0.565	0.571	14.35	14.50	
E	0.906		23.01		REF
E1	0.679	0.691	17.25	17.55	
E2	0.604	0.616	15.34	15.65	
E3	0.588	0.594	14.93	15.09	
E4	0.309	0.321	7.85	8.15	2x
J	ø0.097	ø0.107	ø2.46	ø2.72	4x
L	0.090	0.130	2.29	3.30	2x
r	0.02 TYP		0.51 TYP		12x

Pin	Description
1	GATE/RFIN
2	DRAIN/RFOUT
3	SOURCE/FLANGE

Electrostatic Discharge (ESD) Classifications

Parameter	Symbol	Class	Classification Level	Test Methodology
Human Body Model	HBM	TBD	ANSI/ESDA/JEDEC JS-001 Table 3	JEDEC JESD22 A114-D
Charge Device Model	CDM	TBD	ANSI/ESDA/JEDEC JS-002 Table 3	JEDEC JESD22 C101-C

Product Ordering Information

Order Number	Description	Unit of Measure	Image
CGHV35400F1	Packaged GaN HEMT	Each	
CGHV31500F1-AMP	Evaluation Board w/ GaN HEMT	Each	

For more information, please contact:

4600 Silicon Drive
Durham, NC 27703 USA
Tel: +1.919.313.5300
www.wolfspeed.com/RF

Sales Contact
RFSales@wolfspeed.com

RF Product Marketing Contact
RFMarketing@wolfspeed.com

Notes & Disclaimer

Specifications are subject to change without notice. “Typical” parameters are the average values expected by Wolfspeed in large quantities and are provided for information purposes only. Wolfspeed products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death. No responsibility is assumed by Wolfspeed for any infringement of patents or other rights of third parties which may result from use of the information contained herein. No license is granted by implication or otherwise under any patent or patent rights of Wolfspeed.