

Evaluating the **ADP5023/ADP5024/ADP5034/ADP5037** Micropower Management Unit (Micro PMU)

FEATURES

Full featured evaluation boards for the **ADP5023/ADP5024/ADP5034/ADP5037**

Standalone capability

Simple device measurements, including line and load regulation, demonstrable with

A single voltage supply

A voltmeter

An ammeter

Load resistors

Easy access to external components

Cascading options to supply the low dropout (LDO) regulator from either buck regulator

Dedicated enable option for each channel

Mode option to change buck regulators from power save mode (PSM) to pulse-width modulation (PWM) operation

GENERAL DESCRIPTION

This user guide describes the hardware for the evaluation of the **ADP5023/ADP5024/ADP5034/ADP5037** and includes detailed schematics and printed circuit board (PCB) layouts. The **ADP5023/ADP5024/ADP5034/ADP5037** are available in a 24-lead, 4 mm × 4 mm LFCSP package. The **ADP5023/ADP5024** are 3-channel devices that share a common PCB evaluation board. The **ADP5034/ADP5037** are 4-channel devices that share a common PCB evaluation board. The **ADP5023**, **ADP5024**, **ADP5034**, and **ADP5037** operate in the same manner. Note that this user guide covers all of these boards, but refers to the **ADP5034** for simplicity.

The **ADP5034** LFCSP evaluation board, **ADP5034-1-EVALZ**, has two step-down regulators with two LDO regulators that enable evaluation of the **ADP5034**. The evaluation board is available in an adjustable voltage option.

For full details on the **ADP5023**, **ADP5024**, **ADP5034**, and **ADP5037**, consult the appropriate product data sheet available from Analog Devices, Inc., in conjunction with this evaluation board user guide.

DIGITAL PICTURE OF THE **ADP5034** EVALUATION BOARD

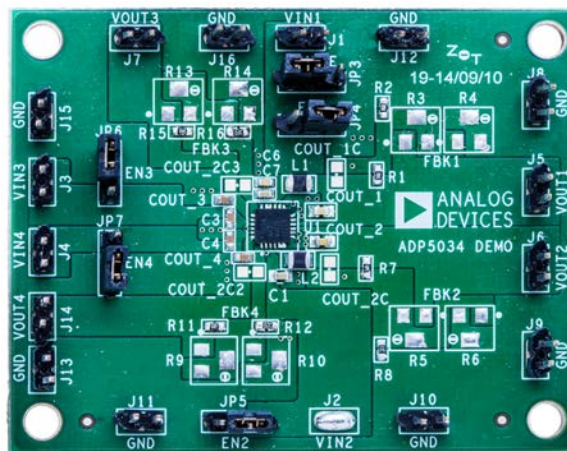


Figure 1.

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REVISION HISTORY

3/2017—Rev. B to Rev. C

Changes to Title and Figure 1	1
Changes to Enable Section, Jumper JP3 (MODE) Section, Input Power Source Section, Input and Output Voltmeters Section, Turning on the Evaluation Board Section, and Setting the Output Voltage of the Buck Regulators and LDO Regulators Section.....	3
Deleted the Setting the Output Voltage of the LDOs Section	4
Changes to Figure 6, Figure 7, Figure 8, and Figure 9	5
Added Figure 8; Renumbered Sequentially	5
Changes to Measuring Line Regulation Section, Figure 11, Measuring Efficiency of Buck Regulator Section, and Figure 13 Caption.....	6
Added Figure 10 and Figure 12.....	6
Changes to Measuring Line Regulation of LDO Regulators Section, Figure 15, Measuring Load Regulation of LDO Regulators, and Figure 17	7
Added Figure 14 and Figure 16.....	7
Moved the Measuring the Ground Current Consumption of the LDO Regulator Section.....	10
Changes to Figure 21 and Figure 22.....	11
Changes to Figure 25 and Figure 26.....	13

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6/2014—Rev. A to Rev. B

Changes to Figure 16.....	10
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Changes to Table 4.....	14

7/2012—Rev. 0 to Rev. A

Added ADP5023, ADP5024, and ADP5037 Throughout	Universal
Replaced all Figures Throughout	Universal
Changes to General Description Section	1
Replaced Powering Up the Evaluation Board Section.....	3
Replaced Evaluation Board Schematics and Artwork Section.....	10
Changes to Bill of Materials and added Related Links Section.....	14

8/2011—Revision 0: Initial Version

USING THE EVALUATION BOARD

POWERING UP THE EVALUATION BOARD

The [ADP5034-1-EVALZ](#) evaluation board is supplied fully assembled and tested. Before applying power to the evaluation board, follow the procedures in this section.

Enable

Each channel has its own enable pin (EN1, EN2, EN3, and EN4), which must be pulled high via the corresponding jumpers to enable that channel (see Table 1).

Table 1. Channels of the Enable Jumper

Channel	Enable Jumper	
	ADP5034/ADP5037	ADP5023/ADP5024
1	JP4	JP4
2	JP5	JP5
3	JP6	JP6
4	JP7	Not applicable

Jumper JP3 (MODE)

Jumper JP3, as shown in Figure 1, connects the MODE pin of the device to either ground or VIN1. To configure Buck 1 and Buck 2 into forced PWM operation, connect the center contact of Jumper JP3 (MODE) to the left pin header to pull the MODE pin high to J1 (VIN1). To allow Buck 1 and Buck 2 to operate in automatic PWM/PSM operation, connect the center contact of JP3 (MODE) to the right pin header to pull the MODE pin low to J12 (GND).

Input Power Source

If the input power source includes a current meter, use that meter to monitor the input current. Connect the positive terminal of the power source to J1 (VIN1) on the evaluation board and the negative terminal of the power source to J12 (GND).

If the power source does not include a current meter, connect a current meter in series with the input source voltage. Connect the positive lead (+) of the power source to the ammeter positive (+) connection, the negative lead (–) of the power source to J12 (GND) on the evaluation board, and the negative lead (–) of the ammeter to J1 (VIN1) on the board. Be aware that current meters add resistance to the input source, causing the input voltage at VIN1 to decrease with high output currents.

Output Load

Connect an electronic load or resistor to set the load current. If the load includes an ammeter, or if the current is not measured, connect the load directly to the evaluation board, with the positive (+) load connected to one of the channels. For example, connect Buck 1, J5 (VOUT1), and the negative (–) load connection to J8 (GND).

If an ammeter is used, connect it in series with the load. Connect the positive (+) ammeter terminal to the evaluation board for Buck 1, J5 (VOUT1), the negative (–) ammeter terminal to the

positive (+) load terminal, and the negative (–) load terminal to the evaluation board at J8 (GND).

Input and Output Voltmeters

Measure the input and output voltages with voltmeters. Ensure that the voltmeters are connected to the appropriate evaluation board terminals and not to the load or power sources themselves.

If the voltmeters are not connected directly to the evaluation board, the measured voltages may be incorrect due to the voltage drop across the leads and/or connections between the evaluation board, the power source, and/or the load.

Connect the input voltage measuring voltmeter positive terminal (+) to the evaluation board at J1 (VIN1), and input voltage measuring voltmeter negative (–) terminal to the evaluation board at J12 (GND).

Connect the output voltage measuring voltmeter positive (+) terminal to the evaluation board at J5 (VOUT1) to measure the output voltage of Buck 1, and connect the output voltage measuring voltmeter negative (–) terminal to the evaluation board at J8 (GND).

Turning On the Evaluation Board

When the power source and load are connected to the evaluation board, the board can be powered for operation. Ensure the following:

- The power source voltage for the buck regulators (VIN1) is from 2.3 V to 5.5 V. The power source voltage for the LDO regulators (VIN3, VIN4) is from the LDO output voltage + 0.5 V or 1.7 V (whichever is greater) to 5.5 V.
- The desired channel is enabled to monitor the output voltage.

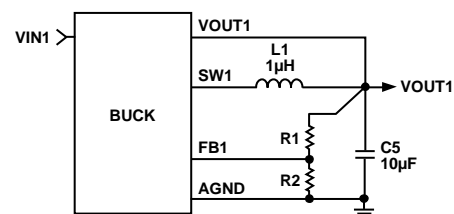
If the load is not enabled, enable the load; check that it is drawing the proper current and that the output voltage maintains voltage regulation.

Setting the Output Voltage of the Buck Regulators and LDO Regulators

The buck output voltage, V_{OUT1} , is set through external resistor dividers, shown in Figure 2 for Buck 1.

The output voltage for Buck 1 is set by

$$V_{OUT1} = V_{FB1} \times (R1/R2 + 1)$$



$$V_{OUT1} = V_{FB1} \left(\frac{R1}{R2} + 1 \right)$$

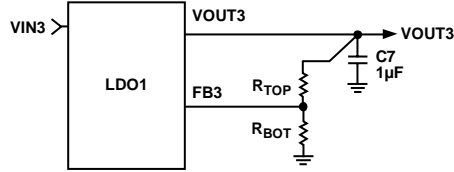
Figure 2. Buck 1 External Output Voltage Setting

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Each LDO regulator output voltage is also set through external resistor dividers as shown in Figure 3 for LDO1.

The output voltage for LDO1 is set by

$$V_{OUT3} = V_{FB3} \times (R_{TOP}/R_{BOT} + 1)$$



$$V_{OUT3} = V_{FB3} \left(\frac{R_{TOP}}{R_{BOT}} + 1 \right)$$

Figure 3. LDO1 External Output Voltage Setting

External Resistor Divider Setting for Buck and LDO Regulators

The [ADP5023CP-EVALZ/ADP5024CP-EVALZ/ADP5034-1-EVALZ/ADP5037CP-EVALZ](#) evaluation boards are supplied with fixed resistor dividers with values chosen for a target output voltage. Varying the resistor values of the resistor divider networks varies the output voltage accordingly.

Table 2. External Resistor Dividers (Fixed)

Resistor Divider	Buck 1	Buck 2	LDO1	LDO2
R _{TOP}	R1	R7	R15	R11
R _{BOT}	R2	R8	R16	R12

In addition to the fixed resistor divider shown in Table 2, the evaluation boards also have footprints for trimmer resistors as listed in Table 3. The trimmer resistors provide easier adjustments of the output voltage by allowing the user to turn the adjustment slots on top of the resistors as shown in Figure 4.

Turning the adjustment slot clockwise increases the resistance and vice versa; adjust accordingly to obtain the desired output voltage. The footprints are designed for 3214W-1-204E parts, which are 200 kΩ trimmer resistors. The trimmers are for quick evaluation purposes and are not recommended for final application due to the potential mechanical issues and complex impedance. When the desired output voltage is obtained, replace the trimmers with fixed value resistors.

Table 3. External Resistor Dividers (Trimmer Resistors)

Resistor Divider	Buck 1	Buck 2	LDO1	LDO2
R _{TOP}	R3	R5	R13	R9
R _{BOT}	R4	R6	R14	R10

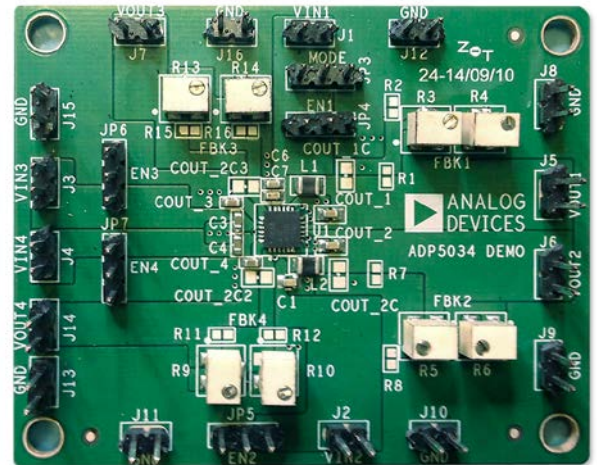


Figure 4. Evaluation Board with Trimmer Resistors

MEASURING EVALUATION BOARD PERFORMANCE

Measuring the Output Voltage Ripple of the Buck Regulator

To observe the output voltage ripple of Buck 1, place an oscilloscope probe across the output capacitor (COUT_1) with the probe ground lead at the negative (-) capacitor terminal and the probe tip at the positive (+) capacitor terminal.

Set the oscilloscope to ac, 10 mV/division, and 2 μs/division time base, with the bandwidth set to 20 MHz to prevent noise from interfering with the measurements. Shorten the ground loop of the oscilloscope probe to minimize coupling. To measure the output voltage ripple, solder a wire to the negative (-) capacitor terminal and wrap it around the barrel of the probe, while the tip directly connects to the positive (+) capacitor terminal as shown in Figure 5.

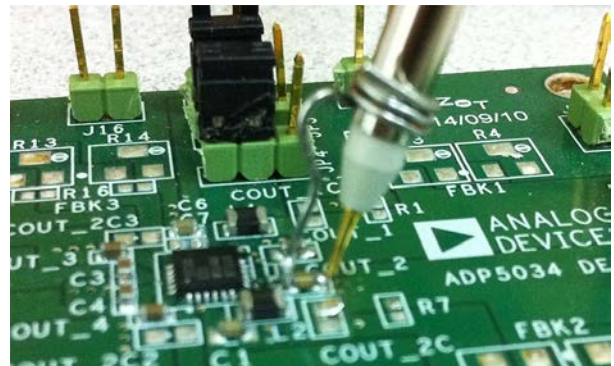


Figure 5. Measuring Output Voltage Ripple

Measuring the Switching Waveform of the Buck Regulator

To observe the switching waveform with an oscilloscope, place the oscilloscope probe tip at the end of the inductor and the probe ground at any GND header (for example, J8, J9, J12, or J13). Set the oscilloscope to dc, 2 V/division, and 200 ns/division time base.

When the MODE pin is set to high, the buck regulators operate in forced PWM mode. When the MODE pin is set to low, the buck regulators operate in PWM mode when the load is above a predefined threshold. When the load current falls below a predefined threshold, the regulator operates in PSM, improving the light load efficiency. Typical PSM and PWM switching waveforms are shown in Figure 6 and Figure 7.

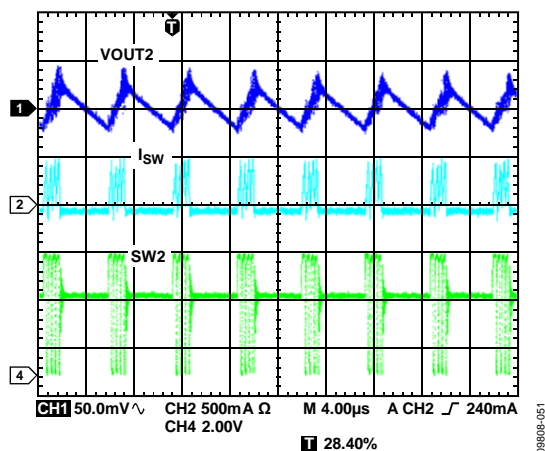


Figure 6. Typical Switching Waveforms, $V_{OUT2} = 3.3\text{ V}$, $I_{OUT2} = 30\text{ mA}$, PSM Mode

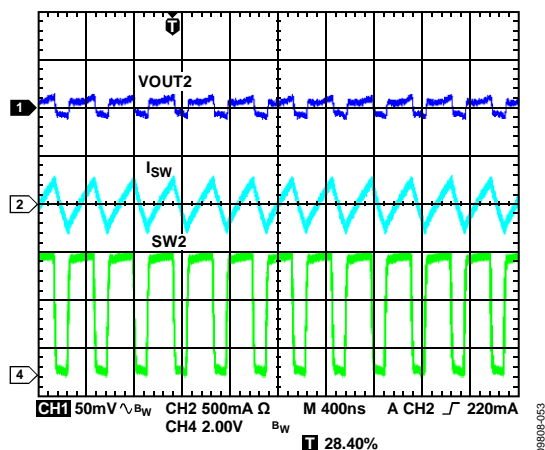


Figure 7. Typical Switching Waveforms, $V_{OUT2} = 3.3\text{ V}$, $I_{OUT2} = 30\text{ mA}$, PWM Mode

Measuring Load Regulation of the Buck Regulator

Test the load regulation by increasing the load at the output and looking at the change in output voltage. The input voltage must be held constant during this measurement. To minimize voltage drop, use short, low resistance wires, especially for loads approaching maximum current. The buck regulator load regulation for $V_{OUT2} = 3.3\text{ V}$ and $V_{OUT2} = 1.8\text{ V}$ are shown in Figure 8 and Figure 9, respectively.

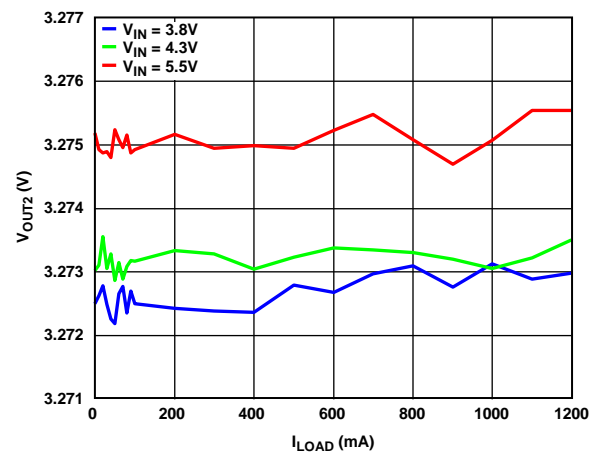


Figure 8. Buck Load Regulation, $V_{OUT2} = 3.3\text{ V}$

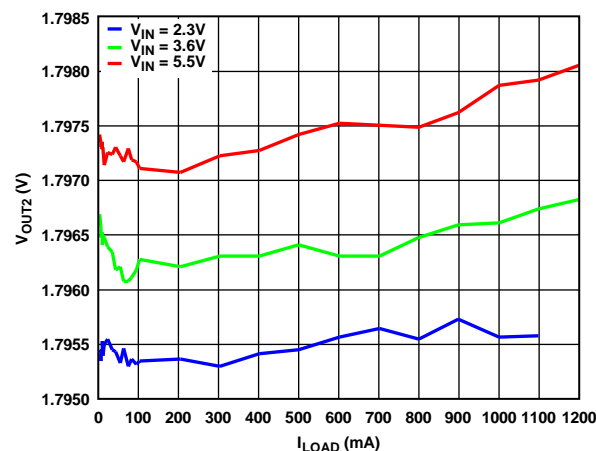


Figure 9. Buck Load Regulation, $V_{OUT2} = 1.8\text{ V}$

Measuring Line Regulation

Vary the input voltage and examine the change in the output voltage. The buck regulator line regulation for $V_{OUT2} = 3.3\text{ V}$ and $V_{OUT2} = 1.8\text{ V}$ are shown in Figure 10 and Figure 11, respectively.

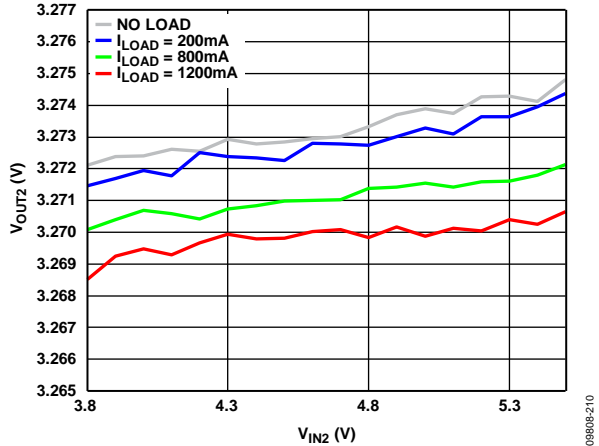


Figure 10. Buck Regulator Line Regulation, $V_{OUT2} = 3.3\text{ V}$

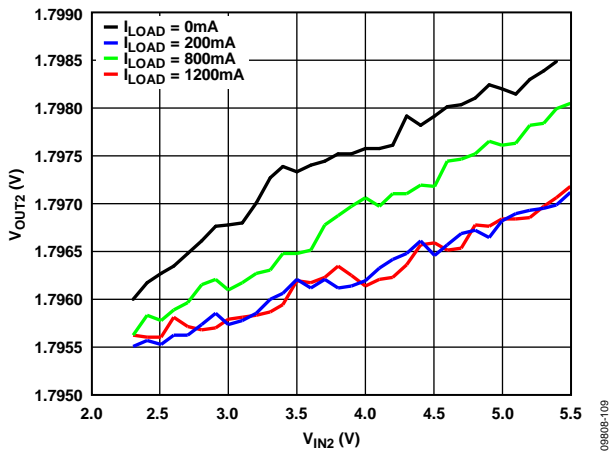


Figure 11. Buck Regulator Line Regulation, $V_{OUT2} = 1.8\text{ V}$

Measuring Efficiency of the Buck Regulator

Measure the efficiency, η , by comparing the input power with the output power.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

Measure the input and output voltages as close as possible to the input and output capacitors to reduce the effect of IR drops.

The buck regulator efficiency for $V_{OUT2} = 3.3\text{ V}$ and $V_{OUT2} = 1.8\text{ V}$ are shown in Figure 12 and Figure 13, respectively.

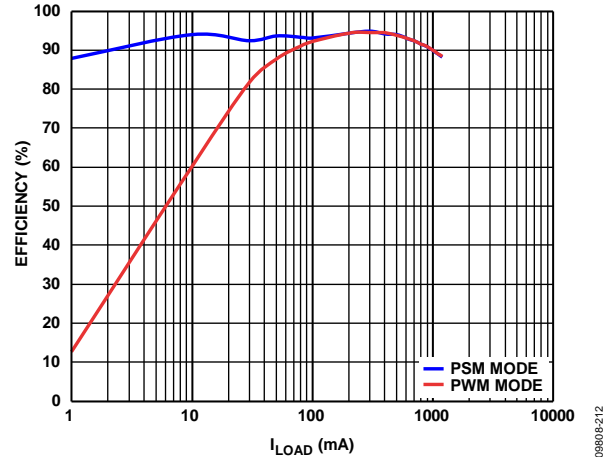


Figure 12. Buck Regulator Efficiency, $V_{IN2} = 4.2\text{ V}$, $V_{OUT2} = 3.3\text{ V}$

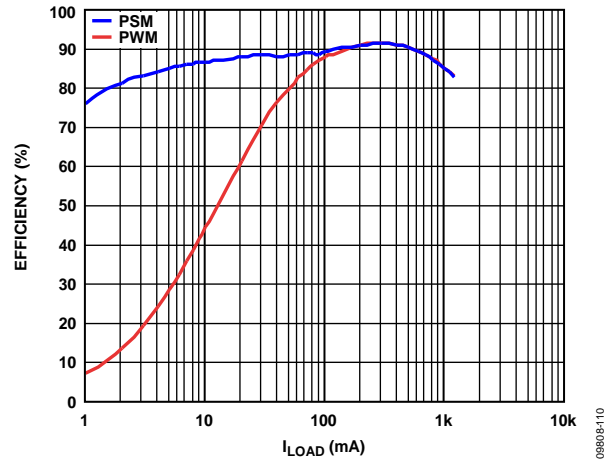


Figure 13. Buck Regulator Efficiency, $V_{IN2} = 3.6\text{ V}$, $V_{OUT2} = 1.8\text{ V}$

Measuring Inductor Current

Measure the inductor current by removing one end of the inductor from its pad and connecting a current loop in series. Connect a current probe to this wire.

Measuring Line Regulation of LDO Regulators

For line regulation measurements, the output of the regulator is monitored while its input is varied. For optimal line regulation, the output must change as little as possible with varying input levels. To ensure that the device is not in dropout mode during this measurement, V_{IN3} (or V_{IN4} for the ADP5037) must be varied between V_{OUT3} nominal + 0.5 V (or 2.3 V, whichever is greater) and V_{IN3} maximum. For example, a fixed 3.3 V output needs V_{IN3} to be varied between 3.8 V and 5.5 V. This measurement can be repeated under different load conditions. Figure 14 and Figure 15 show the typical line regulation performance of the LDO regulator for $V_{OUT3} = 2.8$ V and $V_{OUT3} = 3.3$ V.

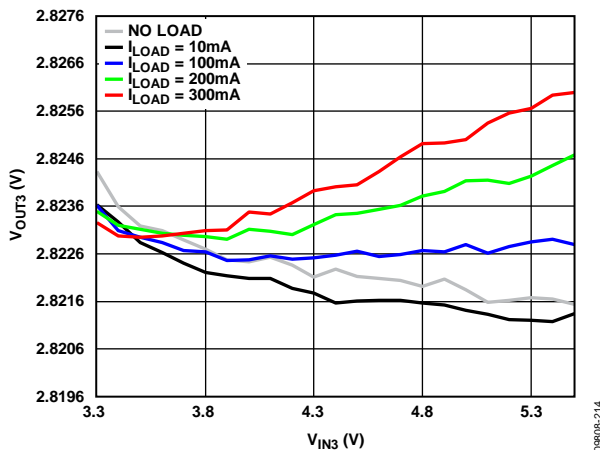


Figure 14. LDO Line Regulation, $V_{OUT3} = 2.8$ V

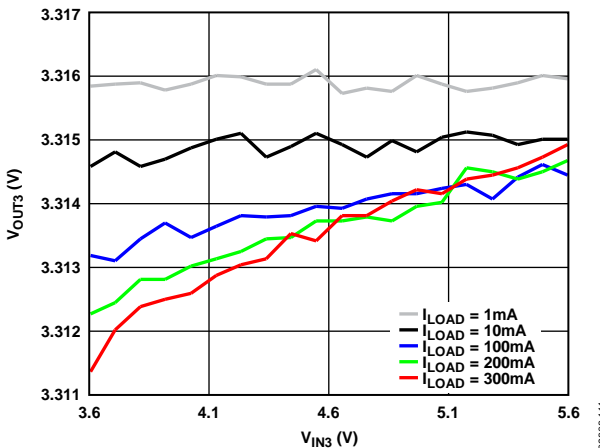


Figure 15. LDO Line Regulation, $V_{OUT3} = 3.3$ V

Measuring Load Regulation of LDO Regulators

For load regulation measurements, the regulator output is monitored while the load is varied. For optimal load regulation, the output must change as little as possible with varying loads. The input voltage must be held constant during this measurement. The load current can be varied from 0 mA to 300 mA. Figure 16 and Figure 17 show the typical load regulation performance of the LDO regulator with a 2.8 V and 3.3 V output for different input voltages.

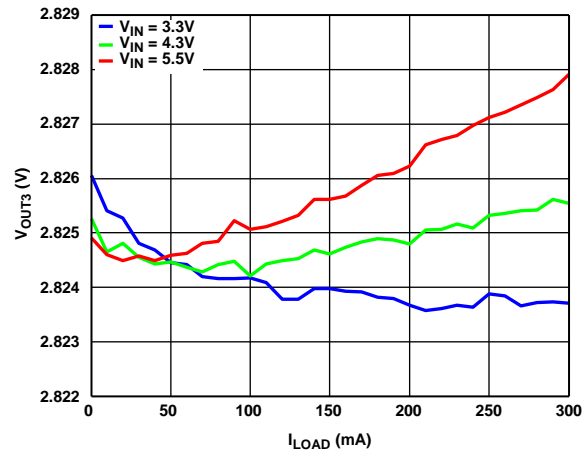


Figure 16. LDO Load Regulation, $V_{OUT3} = 2.8$ V

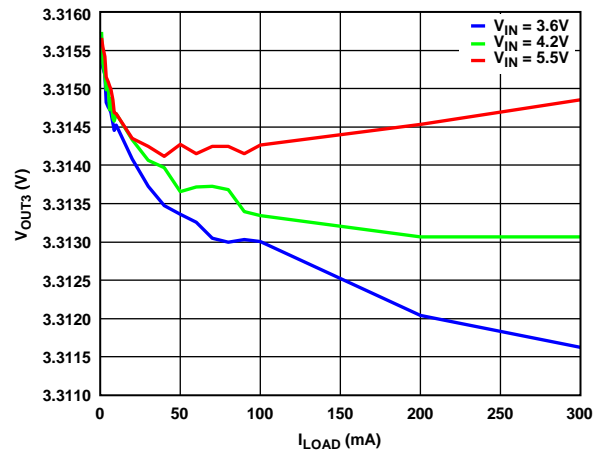


Figure 17. LDO Load Regulation, $V_{OUT3} = 3.3$ V

Measuring the Dropout Voltage of the LDO Regulator

Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. One way to measure dropout voltage is to obtain the output voltage (V_{OUTX} nominal) with V_{IN} initially set to V_{OUTX} nominal + 0.5 V; the output load can be set to 100 μ A. Then, force the input voltage equal to V_{OUTX} nominal, and measure the output voltage accordingly (V_{OUTX} dropout). Dropout voltage is then calculated as V_{OUTX} nominal - V_{OUTX} dropout. This calculation applies only for output voltages greater than 1.7 V. Dropout voltage increases with larger loads. For more accurate measurements, use a second voltmeter to monitor the input voltage across the input capacitor. The input supply voltage may need to be adjusted to account for IR drops, especially if large load currents are used.

Cascading an LDO Regulator from the Buck Regulator

For certain applications such as analog circuit supplies, the LDO regulators are preferred over the buck regulators because of improved noise performance. When none of the buck regulator outputs are being used, the input supply of the LDO regulator can be taken from these outputs. An example evaluation board connection is shown in Figure 18 wherein VOUT1 is tied to VIN3, which is the supply of LDO1. In this configuration, the output voltage of the buck regulator has enough headroom with the desired output voltage of the LDO regulator to guarantee the LDO regulator to operate within specifications.

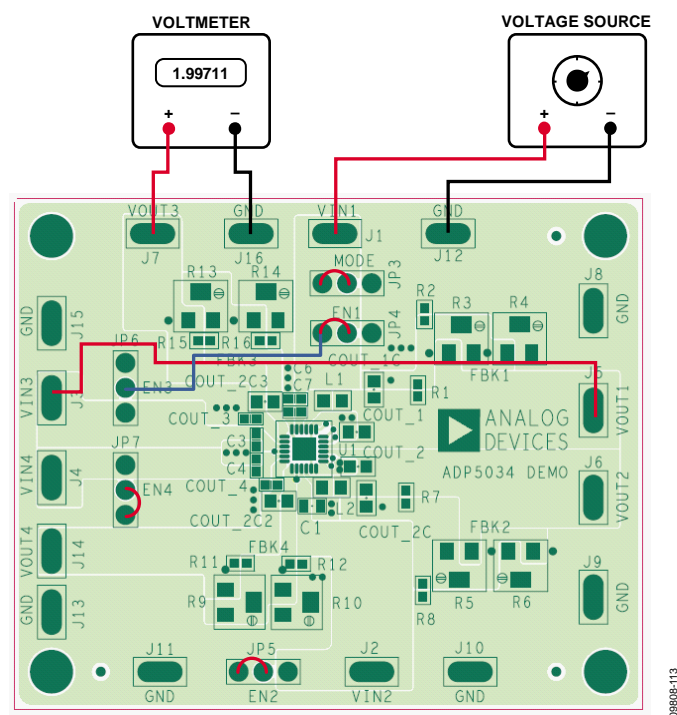


Figure 18. Cascading an LDO Regulator from the Buck Regulator

MEASURING OUTPUT VOLTAGE

Figure 19 shows how the evaluation board can be connected to a voltage source and a voltmeter for basic output voltage accuracy measurements.

Figure 19 shows a voltage source connected to VIN1 and a voltmeter connected to VOUT1, which is the output of Buck 1. EN1 is connected to VIN1 via a shunt, which enables Buck 1, and EN2, EN3, and EN4 are connected to ground, disabling the other channels. When measuring the voltages on VOUT2,

VOUT3, and VOUT4, ensure that the respective channels are enabled, and the voltmeters are connected to the respective outputs.

A resistor can be used as the load for the regulator. Ensure that the resistor has a power rating adequate to handle the power expected to be dissipated across it. An electronic load can also be used as an alternative. Ensure that the voltage source supplies enough current for the expected load levels.

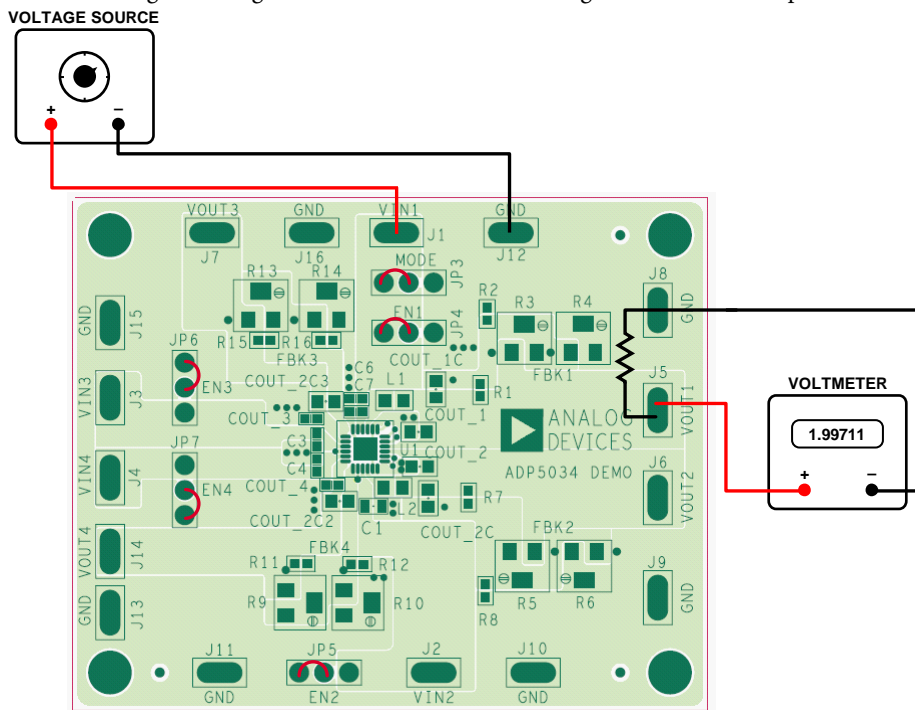


Figure 19. Output Voltage Measurement

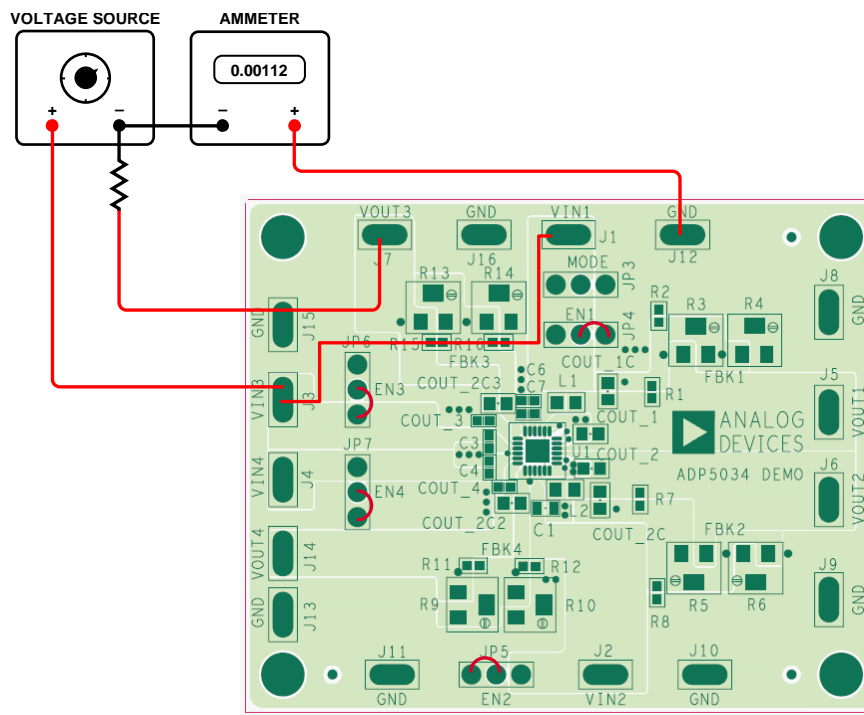
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MEASURING GROUND CURRENT

MEASURING THE GROUND CURRENT CONSUMPTION OF THE LDO REGULATOR

Ground current measurements determine how much current the internal circuits of the regulator consume while the circuits perform the regulation function. To be efficient, the regulator needs to consume as little current as possible. Typically, the regulator uses the maximum current when supplying its largest load level (300 mA). When the device is disabled, the ground current drops to less than 1 μA .

Figure 20 shows the evaluation board connected to a voltage source and an ammeter for ground current measurements. A resistor can be used as the load for the regulator. Ensure that the resistor has a power rating that is adequate to handle the power expected to be dissipated across it. An electronic load can be used as an alternative. Ensure that the voltage source used can supply enough current for the expected load levels.



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Figure 20. Ground Current Measurement

EVALUATION BOARD SCHEMATICS AND ARTWORK

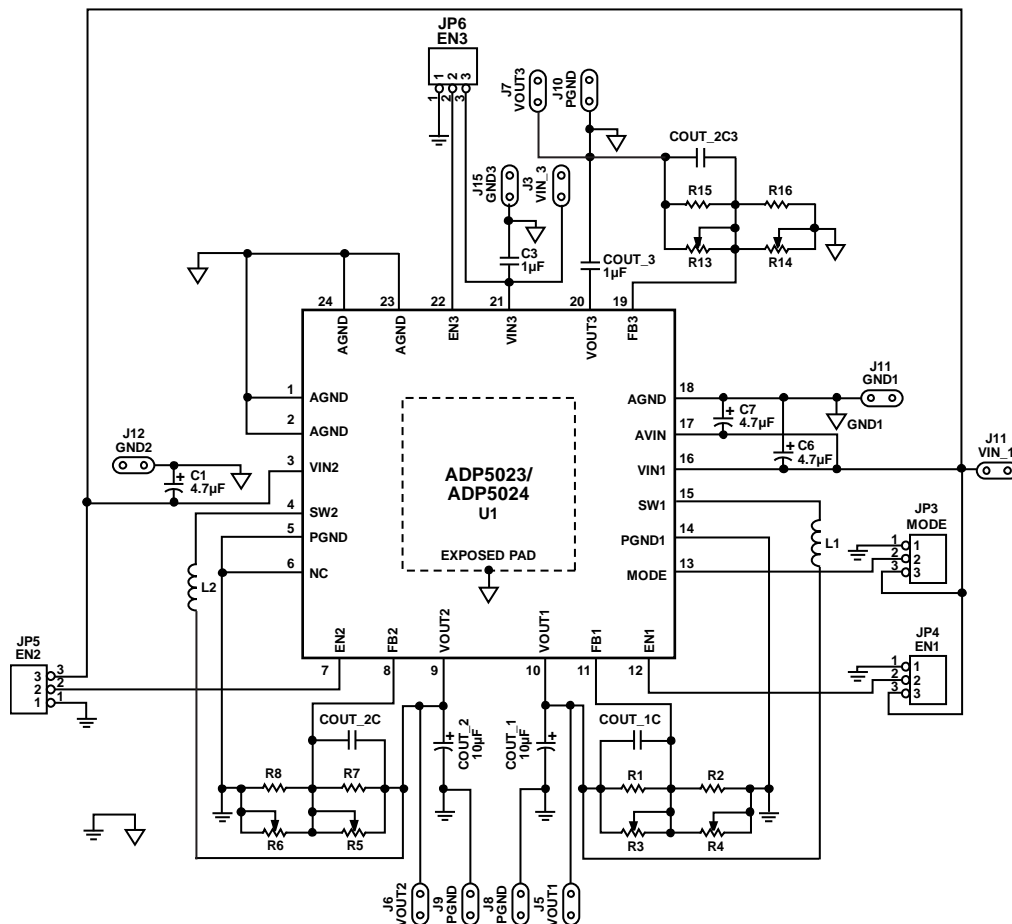


Figure 21. Evaluation Board Schematic of the ADP5023/ADP5024

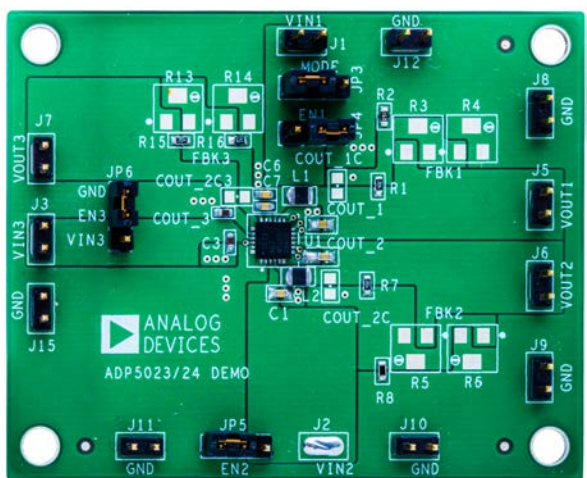


Figure 22. ADP5023/ADP5024 Evaluation Board

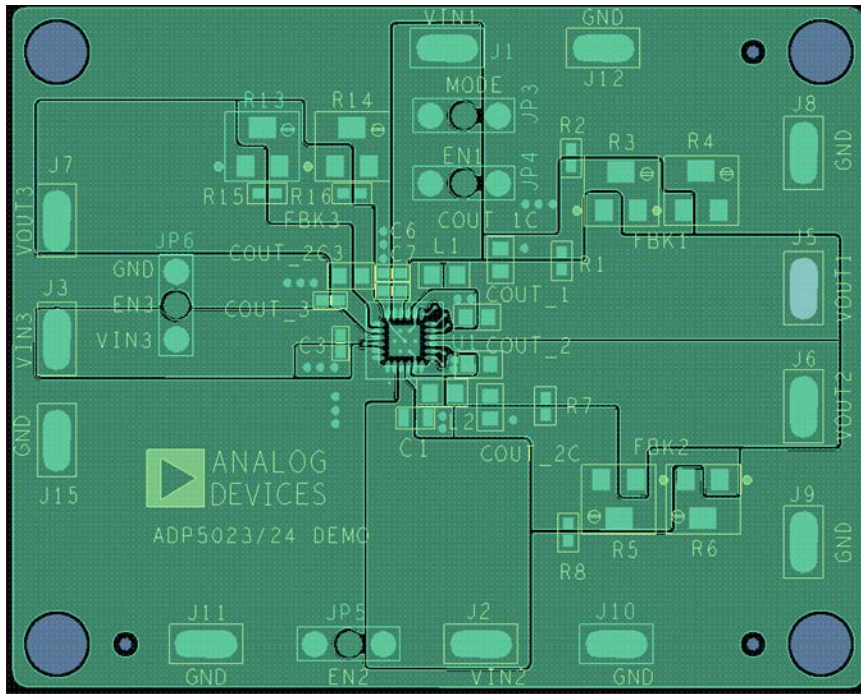


Figure 23. Top Layer, Recommended Layout for ADP5023/ADP5024

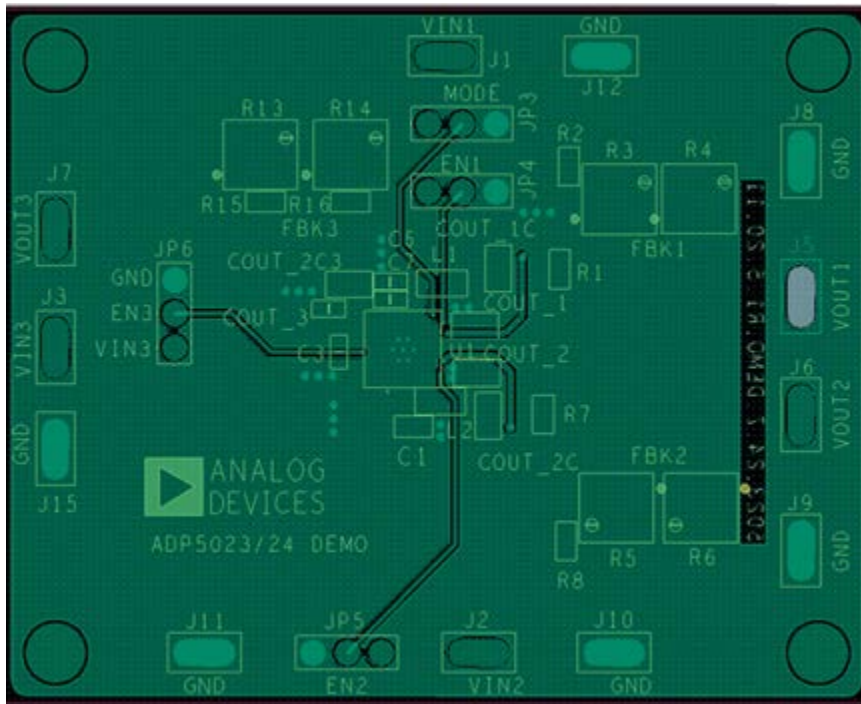


Figure 24. Bottom Layer, Recommended Layout for ADP5023/ADP5024

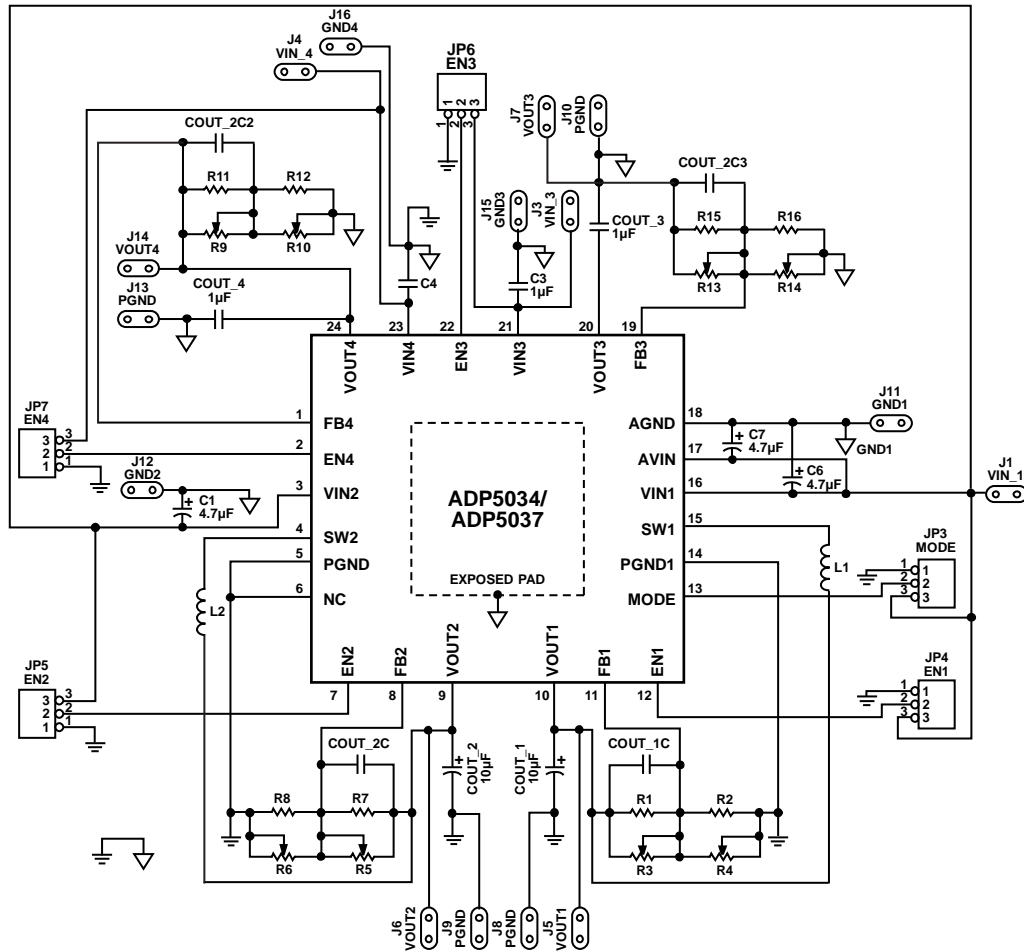


Figure 25. Evaluation Board Schematic of the ADP5034/ADP5037

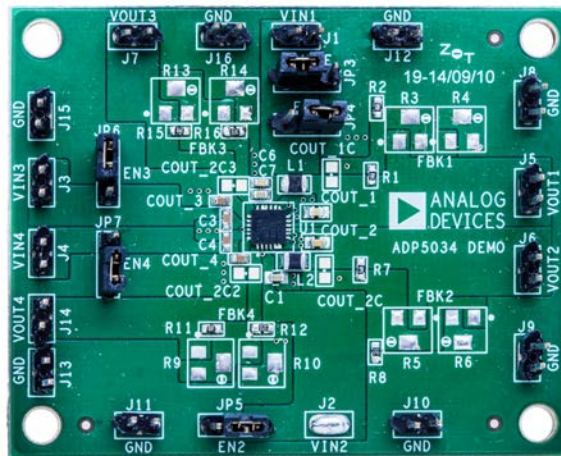
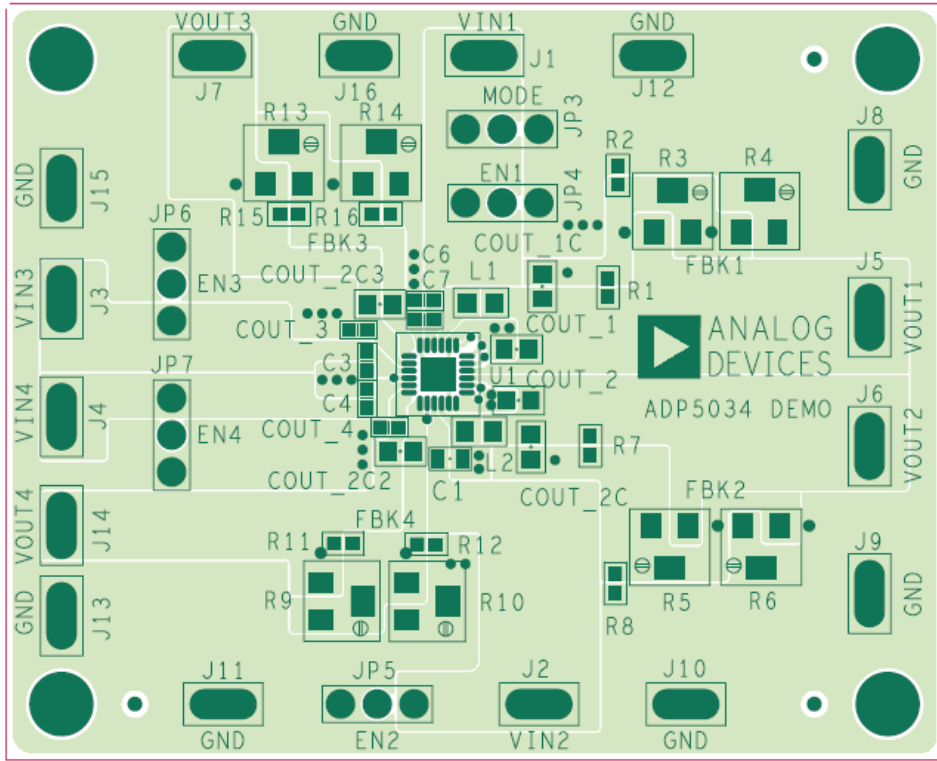
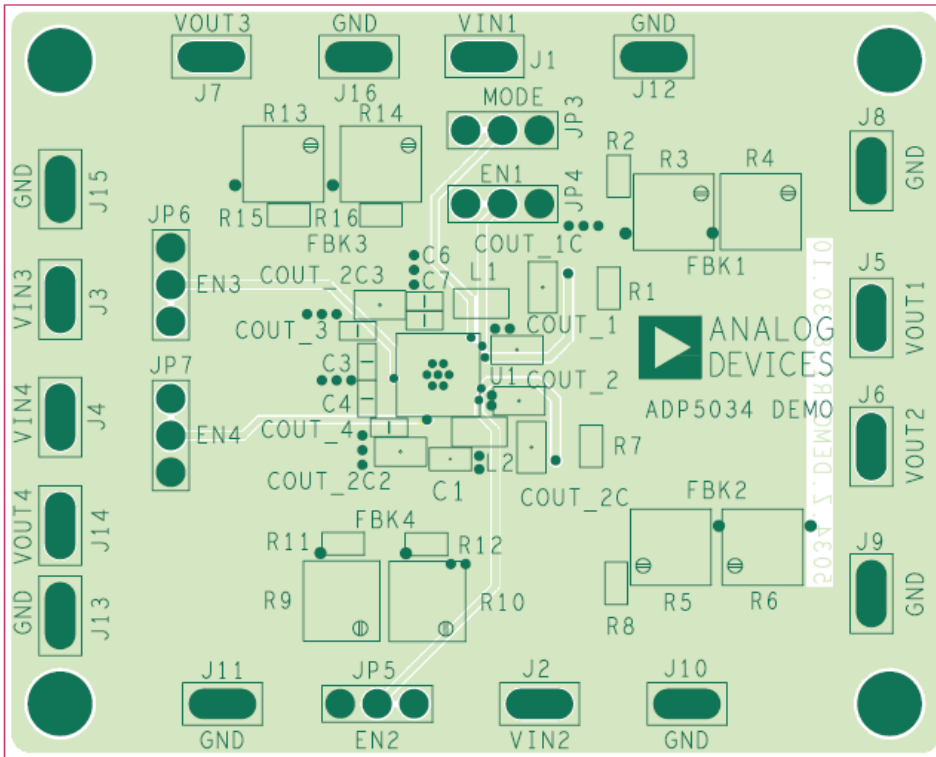


Figure 26. ADP5034/ADP5037 Evaluation Board



09808-010

Figure 27. Top Layer, Recommended Layout for ADP5034/ADP5037



09808-011

Figure 28. Bottom Layer, Recommended Layout for ADP5034/ADP5037

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. [ADP5023/ADP5024](#) Evaluation Board

Qty.	Reference Designator	Description	Manufacturer	Part Number
1	U1	Micro PMU	Analog Devices	ADP5023 or ADP5024
3	C1, C6, C7	Capacitor, MLCC, 4.7 μ F	Murata	GRM188R60J475ME19D
2	C3, COUT_3	Capacitor, MLCC, 1.0 μ F	Murata	GRM188R60J105KA01B
2	COUT_2, COUT_1	Capacitor, MLCC, 10.0 μ F	Murata	GRM188R60J106ME47D
2	L1, L2	Inductor, 1.0 μ H	Murata	LQM2HPN1R0MG0L
6	R3, R4, R5, R6, R13, R14	Not fitted	Not fitted	Not fitted
3	R1, R7, R15	Resistor, 0603, 200 k Ω	Panasonic	ERA-3AEB204V
1	R2	Resistor, 0603, 143 k Ω	Vishay	TNPW0603143KBEEA
1	R8	Resistor, 0603, 35.7 k Ω	Susumu	RG1608P-3572-B-T5
1	R16	Resistor, 0603, 76.8 k Ω	Susumu	RG1608P-7682-B-T5
3	COUT_1C, COUT_2C, COUT_2C3	Not fitted	Not fitted	Not fitted

Table 5. [ADP5034/ADP5037](#) Evaluation Board

Qty.	Reference Designator	Description	Manufacturer	Part Number
1	U1	Micro PMU	Analog Devices	ADP5034 or ADP5037
3	C1, C6, C7	Capacitor, MLCC, 4.7 μ F	Murata	GRM188R60J475ME19D
2	C3, COUT_3	Capacitor, MLCC, 1.0 μ F	Murata	GRM188R60J105KA01B
2	COUT_2, COUT_1	Capacitor, MLCC, 10.0 μ F	Murata	GRM188R60J106ME47D
2	L1, L2	Inductor, 1.0 μ H	Murata	LQM2HPN1R0MG0L
8	R3, R4, R5, R6, R9, R10, R13, R14	Not fitted	Not fitted	Not fitted
4	R1, R7, R11, R15	Resistor, 0603, 200 k Ω	Panasonic	ERA-3AEB204V
1	R2	Resistor, 0603, 143 k Ω	Vishay	TNPW0603143KBEEA
1	R8	Resistor, 0603, 35.7 k Ω	Susumu	RG1608P-3572-B-T5
1	R12	Resistor, 0603, 76.8 k Ω	Susumu	RG1608P-7682-B-T5
1	R16	Resistor, 0603, 43.2 k Ω	Yageo	RT0603DRD0743K2L
4	COUT_1C, COUT_2C, COUT2C2, COUT_2C3	Not fitted	Not fitted	Not fitted

RELATED LINKS

Resource	Description
ADP5023	Dual 3 MHz, 800 mA Buck Regulator with One 300 mA LDO
ADP5024	Dual 3 MHz, 1200 mA Buck Regulators with One 300 mA LDO
ADP5034	Dual 3 MHz, 1200 mA Buck Regulator with Two 300 mA LDOs
ADP5037	Dual 3 MHz, 800 mA Buck Regulators with Two 300 mA LDOs

NOTES

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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