

## SN74LV4046A High-Speed CMOS Logic Phase-Locked Loop With VCO

### 1 Features

- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)
- Choice of Three Phase Comparators
  - Exclusive OR
  - Edge-Triggered J-K Flip-Flop
  - Edge-Triggered RS Flip-Flop
- Excellent VCO Frequency Linearity
- VCO-Inhibit Control for ON/OFF Keying and for Low Standby Power Consumption
- Optimized Power-Supply Voltage Range From 3 V to 5.5 V
- Wide Operating Temperature Range From  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17

### 2 Applications

- Telecommunications
- Signal Generators
- Digital Phase-Locked Loop

### 3 Description

The SN74LV4046A is a high-speed silicon-gate CMOS device that is pin compatible with the CD4046B and the CD74HC4046. The device is specified in compliance with JEDEC Std 7.

The SN74LV4046A is a phase-locked loop (PLL) circuit that contains a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2, and PC3). A signal input and a comparator input are common to each comparator.

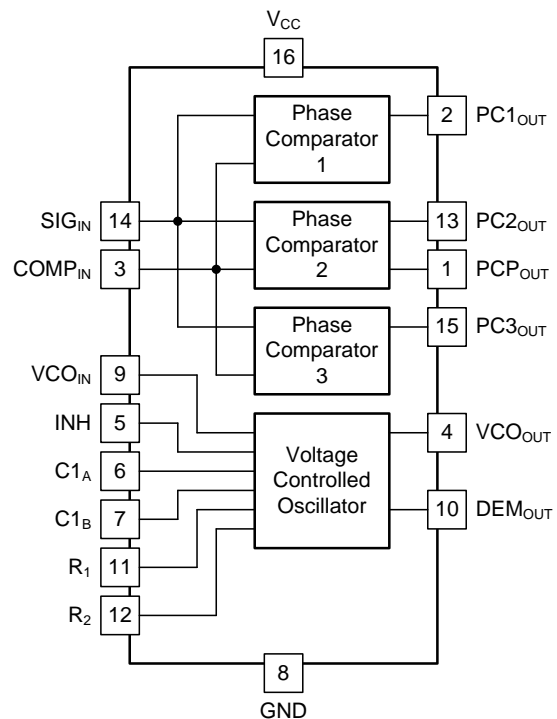
The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the SN74LV4046A forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear operational amplifier techniques. Various applications include telecommunications, digital phase-locked loop and signal generators.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV4046ANS	SO (16)	7.70 mm x 10.20 mm
SN74LV4046AD	SOIC (16)	6.00 mm x 9.90 mm
SN74LV4046APW	TSSOP (16)	6.40 mm x 5.00 mm
SN74LV4046ADGVR	TVSOP (16)	3.60 mm x 4.40 mm
SN74LV4046AN	PDIP (16)	19.30 mm x 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### SN74LV4046A Functional Block Diagram



## Table of Contents

<b>1</b>	<b>Features</b> .....	<b>1</b>	7.4	Device Functional Modes.....	<b>11</b>
<b>2</b>	<b>Applications</b> .....	<b>1</b>	<b>8</b>	<b>Application and Implementation</b> .....	<b>12</b>
<b>3</b>	<b>Description</b> .....	<b>1</b>	8.1	Application Information.....	<b>12</b>
<b>4</b>	<b>Revision History</b> .....	<b>2</b>	8.2	Typical Application .....	<b>12</b>
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	<b>9</b>	<b>Power Supply Recommendations</b> .....	<b>14</b>
<b>6</b>	<b>Specifications</b> .....	<b>4</b>	<b>10</b>	<b>Layout</b> .....	<b>14</b>
6.1	Absolute Maximum Ratings .....	<b>4</b>	10.1	Layout Guidelines .....	<b>14</b>
6.2	ESD Ratings.....	<b>4</b>	10.2	Layout Example .....	<b>14</b>
6.3	Recommended Operating Conditions.....	<b>4</b>	<b>11</b>	<b>Device and Documentation Support</b> .....	<b>15</b>
6.4	Thermal Information .....	<b>4</b>	11.1	Documentation Support .....	<b>15</b>
6.5	Electrical Characteristics.....	<b>5</b>	11.2	Receiving Notification of Documentation Updates .....	<b>15</b>
6.6	Switching Characteristics .....	<b>6</b>	11.3	Community Resources.....	<b>15</b>
6.7	Typical Characteristics .....	<b>9</b>	11.4	Trademarks .....	<b>15</b>
<b>7</b>	<b>Detailed Description</b> .....	<b>10</b>	11.5	Electrostatic Discharge Caution.....	<b>15</b>
7.1	Overview .....	<b>10</b>	11.6	Glossary .....	<b>15</b>
7.2	Functional Block Diagram .....	<b>10</b>	<b>12</b>	<b>Mechanical, Packaging, and Orderable Information</b> .....	<b>15</b>
7.3	Feature Description.....	<b>11</b>			

## 4 Revision History

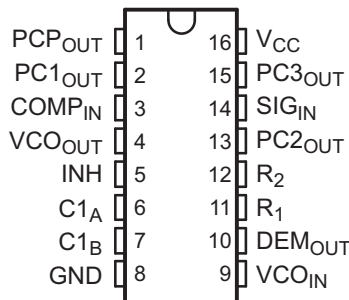
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (September 2015) to Revision E</b>	<b>Page</b>
• Deleted 200-V Machine Model (A115-A) from <i>Features</i> .....	<b>1</b>
• Added TVSOP and PDIP packages to <i>Device Information</i> table .....	<b>1</b>
• Added TVSOP, SO, and PDIP packages to pinout.....	<b>3</b>
• Changed $R_{\theta JA}$ for D package from 73°C/W to 82.8°C/W.....	<b>4</b>
• Changed $R_{\theta JA}$ for DGV package from 120°C/W to 116.8°C/W .....	<b>4</b>
• Changed $R_{\theta JA}$ for NS package from 64°C/W to 83.5°C/W .....	<b>4</b>
• Changed $R_{\theta JA}$ for PW package from 108°C/W to 108.1°C/W .....	<b>4</b>
• Added values in the <i>Thermal Information</i> table to align with JEDEC standards .....	<b>4</b>
• Changed x-axis from "–360° 0° 360°" to "0° 90° 180°" .....	<b>9</b>
• Changed " $(V_{CC}/4)$ " to " $(V_{CC}/4\pi)$ ".....	<b>9</b>
• Added <i>Receiving Notification of Documentation Updates</i> section .....	<b>15</b>

<b>Changes from Revision C (April 2007) to Revision D</b>	<b>Page</b>
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>

## 5 Pin Configuration and Functions

**D, DGV, NS, N, or PW Package  
16-Pin SOIC, TVSOP, SO, PDIP, or TSSOP  
Top View**



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	PCP <sub>OUT</sub>	O	Phase comparator pulse output
2	PC1 <sub>OUT</sub>	O	Phase comparator 1 output
3	COMP <sub>IN</sub>	I	Comparator input
4	VCO <sub>OUT</sub>	O	VCO output
5	INH	I	Inhibit input
6	C1 <sub>A</sub>	—	Capacitor C1 connection A
7	C1 <sub>B</sub>	—	Capacitor C1 connection B
8	GND	—	Ground (0 V)
9	VCO <sub>IN</sub>	I	VCO input
10	DEM <sub>OUT</sub>	O	Demodulator output
11	R <sub>1</sub>	—	Resistor R1 connection
12	R <sub>2</sub>	—	Resistor R2 connection
13	PC2 <sub>OUT</sub>	O	Phase comparator 2 output
14	SIG <sub>IN</sub>	I	Signal input
15	PC3 <sub>OUT</sub>	O	Phase comparator 3 output
16	V <sub>CC</sub>	—	Positive supply voltage

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	DC supply voltage	–0.5	7	V
V <sub>I</sub>	Input voltage	–0.5	V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	Output voltage	–0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	–20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	–50	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>	±35	mA
I <sub>CC</sub>	DC V <sub>CC</sub> or ground current		±70	mA
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T <sub>A</sub>	Operating free-air temperature	–40	125	°C
V <sub>CC</sub>	Supply voltage	3	5.5	V
V <sub>I</sub> , V <sub>O</sub>	DC input or output voltage	0	V <sub>CC</sub>	V

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74LV4046A					UNIT	
	D (SOIC)	DGV (TVSOP)	NS (SO)	PW (TSSOP)	N (PDIP)		
	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	82.8	116.8	83.5	108.1	49.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	44.0	43.3	41.7	42.7	36.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	40.3	48.3	43.8	53.1	29.3	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	11.1	3.7	9.3	4.2	21.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	40.0	47.8	43.5	52.5	29.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		$V_{CC}$ (V)	MIN	TYP	MAX	UNIT
			$V_I$ (V)	$I_o$ (mA)					
<b>VCO</b>									
$V_{IH}$	High-level input voltage	INH			3 to 3.6	$V_{CC} \times 0.7$		V	
					4.5 to 5.5	$V_{CC} \times 0.7$			
$V_{IL}$	Low-level input voltage	INH			3 to 5.5	$V_{CC} \times 0.3$		V	
					4.5 to 5.5	$V_{CC} \times 0.3$			
$V_{OH}$	High-level output voltage	$V_{CO\_OUT}$	CMOS	$V_{IL}$ or $V_{IH}$	-0.05	3 to 3.6	$V_{CC} - 0.1$		V
			TTL			4.5 to 5.5	3.8		
$V_{OL}$	Low-level output voltage	$V_{CO\_OUT}$	CMOS	$V_{IL}$ or $V_{IH}$	0.05	3 to 3.6	0.1		V
			TTL			4.5 to 5.5	0.1		
			C1A, C1B (test purposes only)			12	4.5 to 5.5	0.55	
$I_i$	Input leakage current	INH, $V_{CO\_IN}$	$V_{CC}$ or GND		5.5			$\pm 1$	$\mu A$
						R1 range <sup>(1)</sup>		3	50
R2 range <sup>(1)</sup>					3 to 5.5	3		50	k $\Omega$
C1 capacitance range					3 to 3.6	40		No Limit	pF
					4.5 to 5.5	40		No Limit	
Operating voltage range		$V_{CO\_IN}$	Over the range specified for R1 for linearity <sup>(2)</sup>		3 to 3.6	1.1		1.9	V
					4.5 to 5.5	1.1		3.2	
<b>PHASE COMPARATOR</b>									
$V_{IH}$	DC-coupled high-level input voltage	$SIG_{IN}$ , $COMP_{IN}$			3 to 3.6	$V_{CC} \times 0.7$		V	
					4.5 to 5.5	$V_{CC} \times 0.7$			
$V_{IL}$	DC-coupled low-level input voltage	$SIG_{IN}$ , $COMP_{IN}$			3 to 3.6	$V_{CC} \times 0.3$		V	
					4.5 to 5.5	$V_{CC} \times 0.3$			
$V_{OH}$	High-level output voltage	$PCP_{OUT}$ , $PCN_{OUT}$	CMOS	$V_{IL}$ or $V_{IH}$	-0.05	3 to 5.5	$V_{CC} - 0.1$		V
			TTL			-6	2.48		
$V_{OL}$	Low-level output voltage	$PCP_{OUT}$ , $PCN_{OUT}$	CMOS	$V_{IL}$ or $V_{IH}$	0.02	3 to 3.6	0.1		V
			TTL			4	0.4		
$I_i$	Input leakage current	$SIG_{IN}$ , $COMP_{IN}$	$V_{CC}$ or GND		3 to 3.6			$\pm 11$	$\mu A$
					4.5 to 5.5			$\pm 29$	
$I_{OZ}$	3-state off-state current	$PC2_{OUT}$	$V_{IL}$ or $V_{IH}$		3 to 5.5			$\pm 5$	$\mu A$
$R_I$	Input resistance	$SIG_{IN}$ , $COMP_{IN}$	$V_I$ at self-bias operating point, $V_I = 0.5$ V		3	800		k $\Omega$	
					4.5	250			
<b>DEMODULATOR</b>									
$R_S$	Resistor range	$R_S > 300$ k $\Omega$ , Leakage current can influence $V_{DEMOUT}$			3 to 3.6	50		300	k $\Omega$
					4.5 to 5.5	50		300	
$V_{OFF}$	Offset voltage $V_{CO\_IN}$ to $V_{DEM}$	$V_I = V_{VCO\_IN} = V_{CC2}$ , Values taken over $R_S$ range			3 to 3.6	$\pm 30$		mV	
					4.5 to 5.5	$\pm 20$			
$I_{CC}$	Quiescent device current	Pins 3, 5, and 14 at $V_{CC}$ , Pin 9 at GND, $I_i$ at pins 3 and 14 to be excluded			5.5			50	$\mu A$

(1) The value for R1 and R2 in parallel should exceed 2.7 k $\Omega$ .

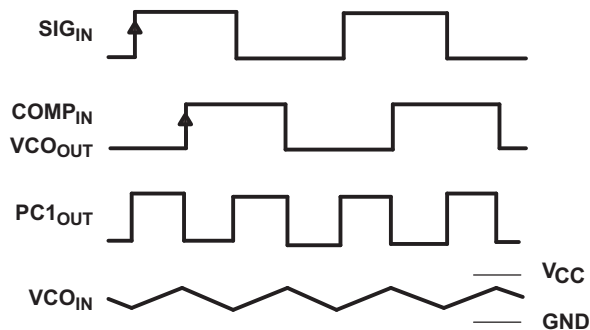
(2) The maximum operating voltage can be as high as  $V_{CC} - 0.9$  V; however, this may result in an increased offset voltage.

## 6.6 Switching Characteristics

 over operating free-air temperature range (unless otherwise noted)  $C_L = 50$  pF, Input  $t_r, t_f = 6$  ns

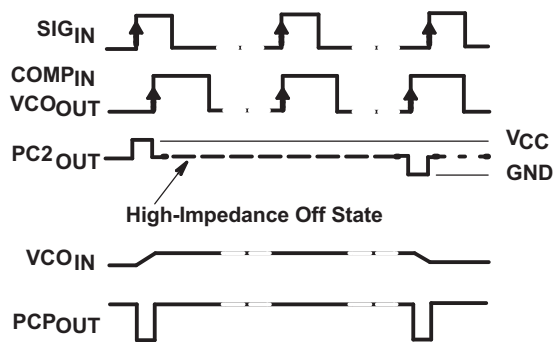
PARAMETER		TEST CONDITIONS	$V_{CC}$ (V)	MIN	TYP	MAX	UNIT
<b>PHASE COMPARATOR</b>							
$t_{PLH}, t_{PHL}$	Propagation delay	SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC1 <sub>OUT</sub>	3 to 3.6			135	ns
			4.5 to 5.5			50	
$t_{PLH}, t_{PHL}$	Propagation delay	SIG <sub>IN</sub> , COMP <sub>IN</sub> to PCP <sub>OUT</sub>	3 to 3.6			300	ns
			4.5 to 5.5			60	
$t_{PLH}, t_{PHL}$	Propagation delay	SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC3 <sub>OUT</sub>	3 to 3.6			200	ns
			4.5 to 5.5			50	
$t_{THL}, t_{TLH}$	Output transition time		3 to 3.6			75	ns
			4.5 to 5.5			15	
$t_{PZH}, t_{PZL}$	3-state output enable time	SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC2 <sub>OUT</sub>	3 to 3.6			270	ns
			4.5 to 5.5			54	
$t_{PHZ}, t_{PLZ}$	3-state output disable time	SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC2 <sub>OUT</sub>	3 to 3.6			320	ns
			4.5 to 5.5			65	
	AC-coupled input sensitivity	(P-P) at SIG <sub>IN</sub> or COMP <sub>IN</sub>	$V_{I(P-P)}$	3 to 3.6		11	mV
				4.5 to 5.5		15	
<b>VCO</b>							
$\Delta f/\Delta T$	Frequency stability with temperature change	$V_I = V_{COIN} = 1/2 V_{CC}$ , $R_1 = 100$ k $\Omega$ , $R_2 = \infty$ , $C_1 = 100$ pF	3 to 3.6		0.11		%/ $^{\circ}$ C
			4.5 to 5.5		0.11		
$f_{MAX}$	Maximum frequency	$C_1 = 50$ pF, $R_1 = 3.5$ k $\Omega$ , $R_2 = \infty$	3 to 3.6		24		MHz
			4.5 to 5.5		24		
			3 to 3.6		38		
			4.5 to 5.5		38		
	Center frequency (duty 50%)	$C_1 = 40$ pF, $R_1 = 3$ k $\Omega$ , $R_2 = \infty$ , $V_{COIN} = V_{CC}/2$	3 to 3.6	7	10		MHz
			4.5 to 5.5	12	17		
			4.5 <sup>(1)</sup>	15 <sup>(1)</sup>	17.5 <sup>(1)</sup>		
$\Delta f_{VCO}$	Frequency linearity	$C_1 = 100$ pF, $R_1 = 100$ k $\Omega$ , $R_2 = \infty$	3 to 3.6		0.4%		
			4.5 to 5.5		0.4%		
	Offset frequency	$C_1 = 1$ nF, $R_2 = 220$ k $\Omega$	3 to 3.6		400		kHz
			4.5 to 5.5		400		
<b>DEMODULATOR</b>							
$V_{OUT}$ vs $f_{IN}$		$C_1 = 100$ pF, $C_2 = 100$ pF, $R_1 = 100$ k $\Omega$ , $R_2 = \infty$ , $R_3 = 100$ k $\Omega$	3		8		mV/kHz
			4.5		330		

 (1) Data is specified at 25 $^{\circ}$ C



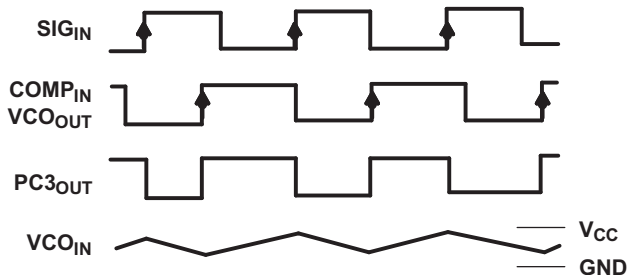
Loop Locked at  $f_o$

Figure 1. Typical Waveforms for PLL Using Phase Comparator 1



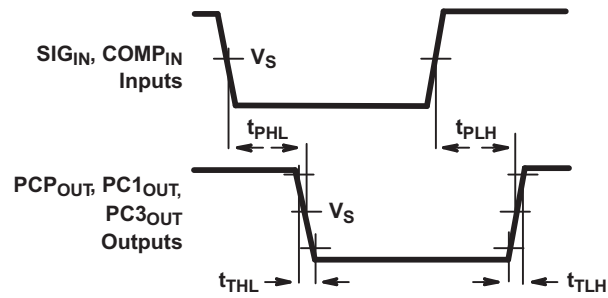
Loop Locked at  $f_o$

Figure 2. Typical Waveforms for PLL Using Phase Comparator 2

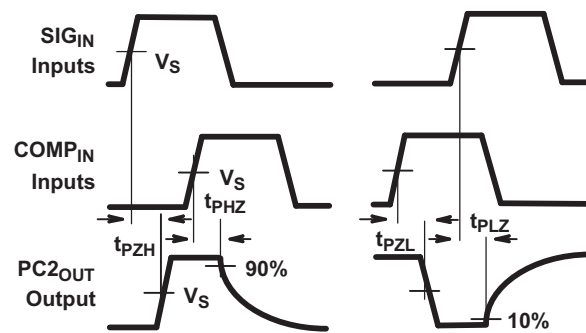


Loop Locked at  $f_o$

Figure 3. Typical Waveforms for PLL Using Phase Comparator 3



**Figure 4. Input-to-Output Propagation Delays and Output Transition Times**



**Figure 5. 3-State Enable and Disable Times for PC2<sub>OUT</sub>**



## 6.7 Typical Characteristics

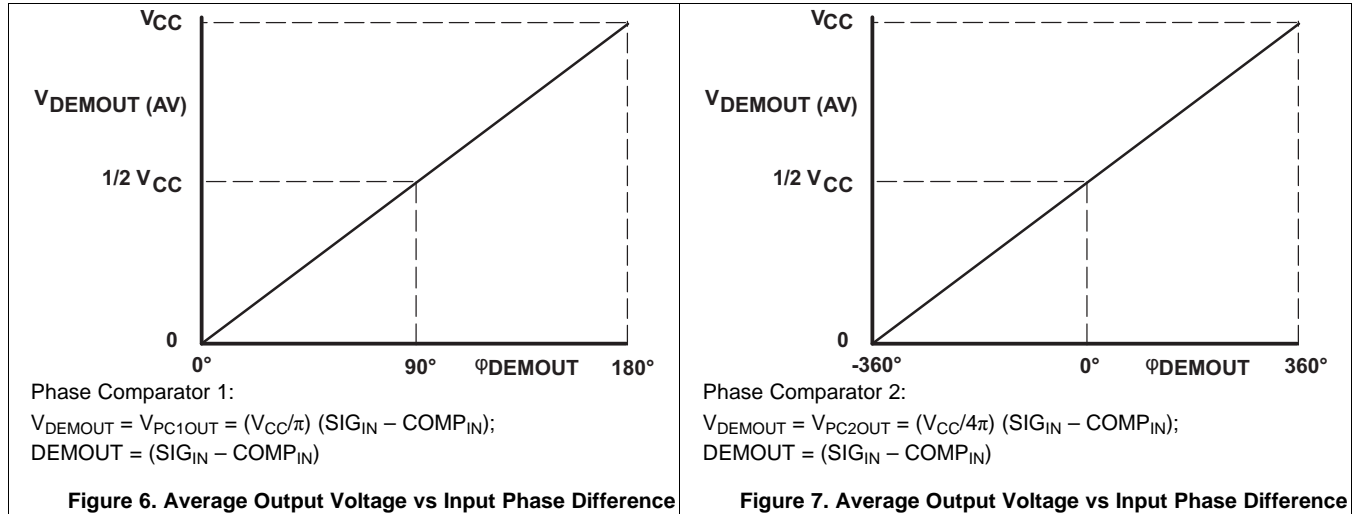


Figure 6. Average Output Voltage vs Input Phase Difference

Figure 7. Average Output Voltage vs Input Phase Difference

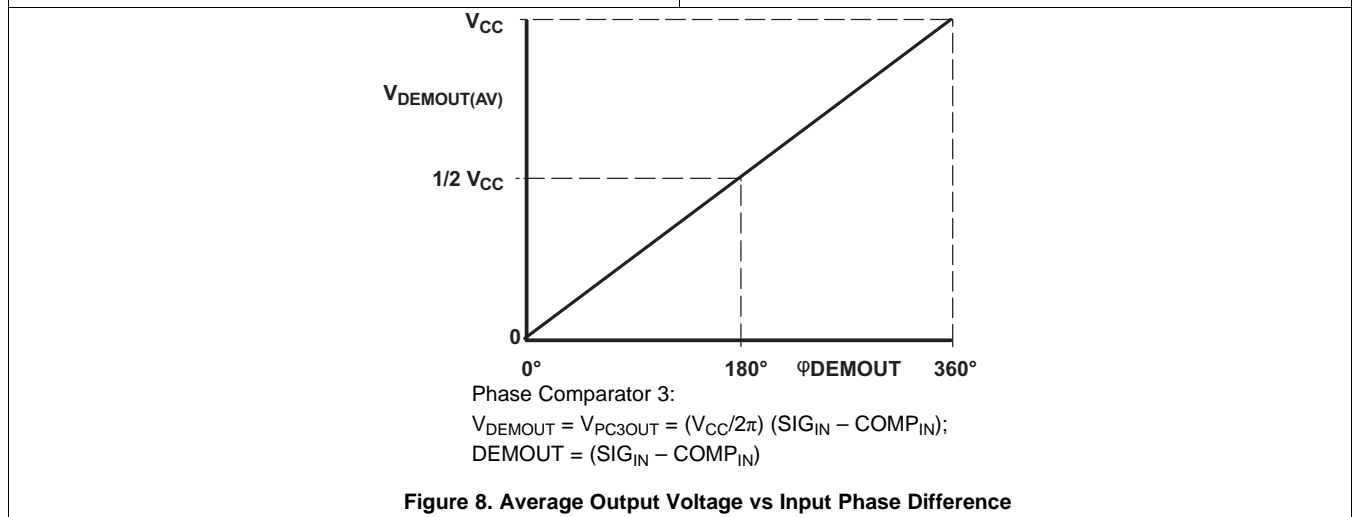


Figure 8. Average Output Voltage vs Input Phase Difference



### 7.3 Feature Description

There are three choices for the Phase Comparators in this device which are listed as follows:

- Phase comparator 1 (PC1) is an Exclusive OR network. The average output voltage from PC1, fed to VCO input through the low pass filter and seen at the demodulator output at pin 10 ( $V_{\text{DEMOUT}}$ ), is the resultant of the phase differences of signals ( $\text{SIG}_{\text{IN}}$ ) and the comparator input ( $\text{COMP}_{\text{IN}}$ ) as shown in [Figure 7](#). The average of  $V_{\text{DEM}}$  is equal to  $1/2 V_{\text{CC}}$  when there is no signal or noise at  $\text{SIG}_{\text{IN}}$ , and with this input the VCO oscillates at the center frequency ( $f_0$ ).
- Phase comparator 2 (PC2) is an Edge-Triggered Flip-Flop. This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of  $\text{SIG}_{\text{IN}}$  and  $\text{COMP}_{\text{IN}}$  are not important. PC2 comprises two D-type flip-flops, controlling and a three-state output stage. The circuit functions as an up-down counter where  $\text{SIG}_{\text{IN}}$  causes an up-count and  $\text{COMP}_{\text{IN}}$  a down-count. The average output voltage from PC2, fed to the VCO through the lowpass filter and seen at the demodulator output at pin 10 ( $V_{\text{DEMOUT}}$ ), is the resultant of the phase differences of  $\text{SIG}_{\text{IN}}$  and  $\text{COMP}_{\text{IN}}$  as in [Figure 8](#).
- Phase comparator 3 (PC3) is an positive Edge-Triggered RS Flip-Flop. This is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of  $\text{SIG}_{\text{IN}}$  and  $\text{COMP}_{\text{IN}}$  are not important. The average output from PC3, fed to the VCO through the lowpass filter and seen at the demodulator at pin 10 ( $V_{\text{DEMOUT}}$ ), is the resultant of the phase differences of  $\text{SIG}_{\text{IN}}$  and  $\text{COMP}_{\text{IN}}$  as shown in [Figure 9](#).

The excellent VCO linearity is achieved by the use of linear operational amplifier techniques. It has low standby power consumption using VCO inhibit control. Wide operating temperature range from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  along with an optimized power supply voltage range from 3 V to 5.5 V.

### 7.4 Device Functional Modes

The SN74LV4046A device does not feature any special functional modes.

## 8 Application and Implementation

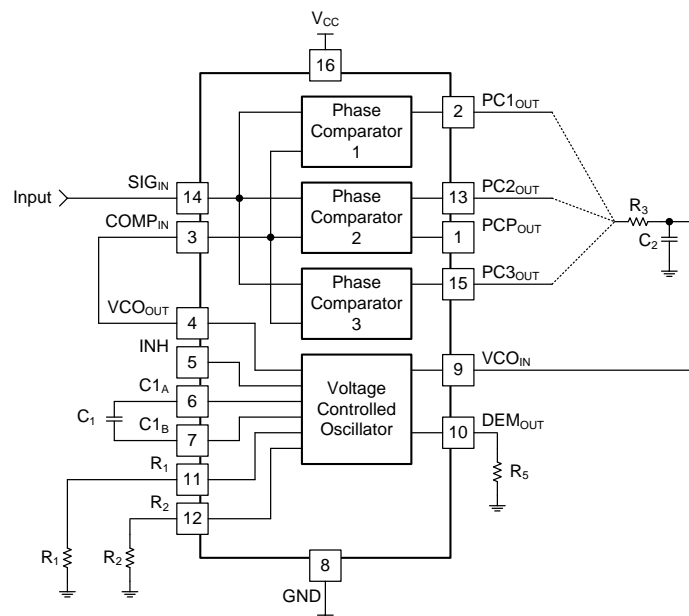
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The most common use for the digital phased-locked loop (PLL) device is to match the VCO output to the same phase as the incoming signal and produce an error signal ( $DEM_{OUT}$ ) that indicates the amount of phase shift required for the match. This can be used as part of many complex systems.

### 8.2 Typical Application



**Figure 9. SN74LV4046A Digital Clock Signal Phase Comparison Application**

## Typical Application (continued)

### 8.2.1 Design Requirements

Table 1 and Table 2 lists the design requirements of the SN74LV4046A.

**Table 1. Component Selection Criteria<sup>(1)</sup>**

COMPONENT	VALUE
R1	3 kΩ to 50 kΩ
R2	3 kΩ to 50 kΩ
R1    R2	> 2.7 kΩ
C1	> 40 pF
R3	1 kΩ
C2	1 uF
R5	50 kΩ to 300 kΩ

- (1) R1 between 3 kΩ and 50 kΩ  
R2 between 3 kΩ and 50 kΩ  
R1 + R2 parallel value > 2.7 kΩ  
C1 > 40 pF

**Table 2. C<sub>PD</sub><sup>(1)</sup>**

CHIP SECTION	C <sub>PD</sub>	UNIT
Comparator 1	120	pF
VCO	120	

- (1) R1 between 3 kΩ and 50 kΩ  
R2 between 3 kΩ and 50 kΩ  
R1 + R2 parallel value > 2.7 kΩ  
C1 > 40 pF

### 8.2.2 Detailed Design Procedure

- Recommended Input Conditions:
  - $V_{IH}$  and  $V_{IL}$  for each input can be found in [Electrical Characteristics](#).
- Recommended Output Conditions:
  - Valid load resistor values are specified in [Electrical Characteristics](#).
- Frequency Selection Criterion:
  - Frequency data is found in [Electrical Characteristics](#).

### 8.2.3 Application Curves

Table 3 lists the application curves in the [Typical Characteristics](#) section.

**Table 3. Table of Graphs**

GRAPH TITLE	FIGURE
Average Output Voltage vs Input Phase Difference	<a href="#">Figure 6</a>
Average Output Voltage vs Input Phase Difference	<a href="#">Figure 7</a>
Average Output Voltage vs Input Phase Difference	<a href="#">Figure 8</a>

## 9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage ratings located in the [Recommended Operating Conditions](#) table.

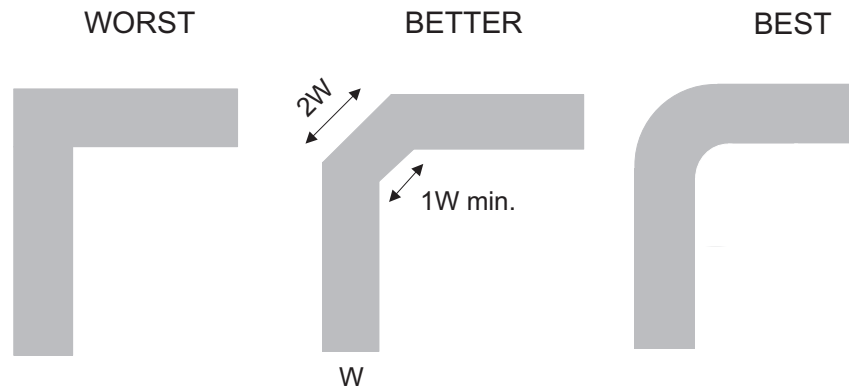
Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu\text{F}$  capacitor is recommended and if there are multiple  $V_{CC}$  pins then 0.01- $\mu\text{F}$  or 0.022- $\mu\text{F}$  capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 10 Layout

### 10.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 10](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

### 10.2 Layout Example



**Figure 10. Trace Example**

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#), SCBA004

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV4046AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4046A	<a href="#">Samples</a>
SN74LV4046ADGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	<a href="#">Samples</a>
SN74LV4046ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4046A	<a href="#">Samples</a>
SN74LV4046AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4046AN	<a href="#">Samples</a>
SN74LV4046ANS	ACTIVE	SO	NS	16	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4046A	<a href="#">Samples</a>
SN74LV4046ANSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4046A	<a href="#">Samples</a>
SN74LV4046APW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	<a href="#">Samples</a>
SN74LV4046APWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	<a href="#">Samples</a>
SN74LV4046APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4046ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4046ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4046ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV4046APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4046ADGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
SN74LV4046ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LV4046ANSR	SO	NS	16	2000	356.0	356.0	35.0
SN74LV4046APWR	TSSOP	PW	16	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LV4046AD	D	SOIC	16	40	507	8	3940	4.32
SN74LV4046AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4046AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4046ANS	NS	SOP	16	50	530	10.5	4000	4.1
SN74LV4046APW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LV4046APWG4	PW	TSSOP	16	90	530	10.2	3600	3.5

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



4220735/A 12/2021

#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.





D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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