

SN54LS640 THRU SN54LS642, SN54LS644, SN54LS645 SN74LS640 THRU SN74LS642, SN74LS644, SN74LS645 OCTAL BUS TRANSCEIVERS

SDLS189 – APRIL 1979 – REVISED MARCH 1988

- **SN74LS64X-1 Versions Rated at I_{OL} of 48 mA**
- **Bi-directional Bus Transceivers in High-Density 20-Pin Packages**
- **Hysteresis at Bus Inputs Improves Noise Margins**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**

DEVICE	OUTPUT	LOGIC
'LS640	3-State	Inverting
'LS641	Open-Collector	True
'LS642	Open-Collector	Inverting
'LS644	Open-Collector	True and inverting
'LS645	3-State	True

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (\bar{G}) can be used to disable the device so the buses are effectively isolated.

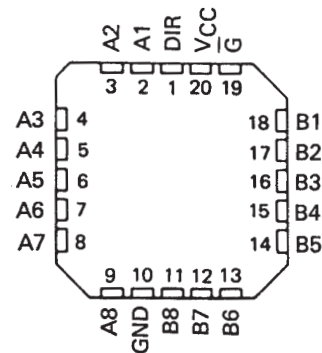
The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C .

SN54LS' . . . J PACKAGE
SN74LS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS' . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

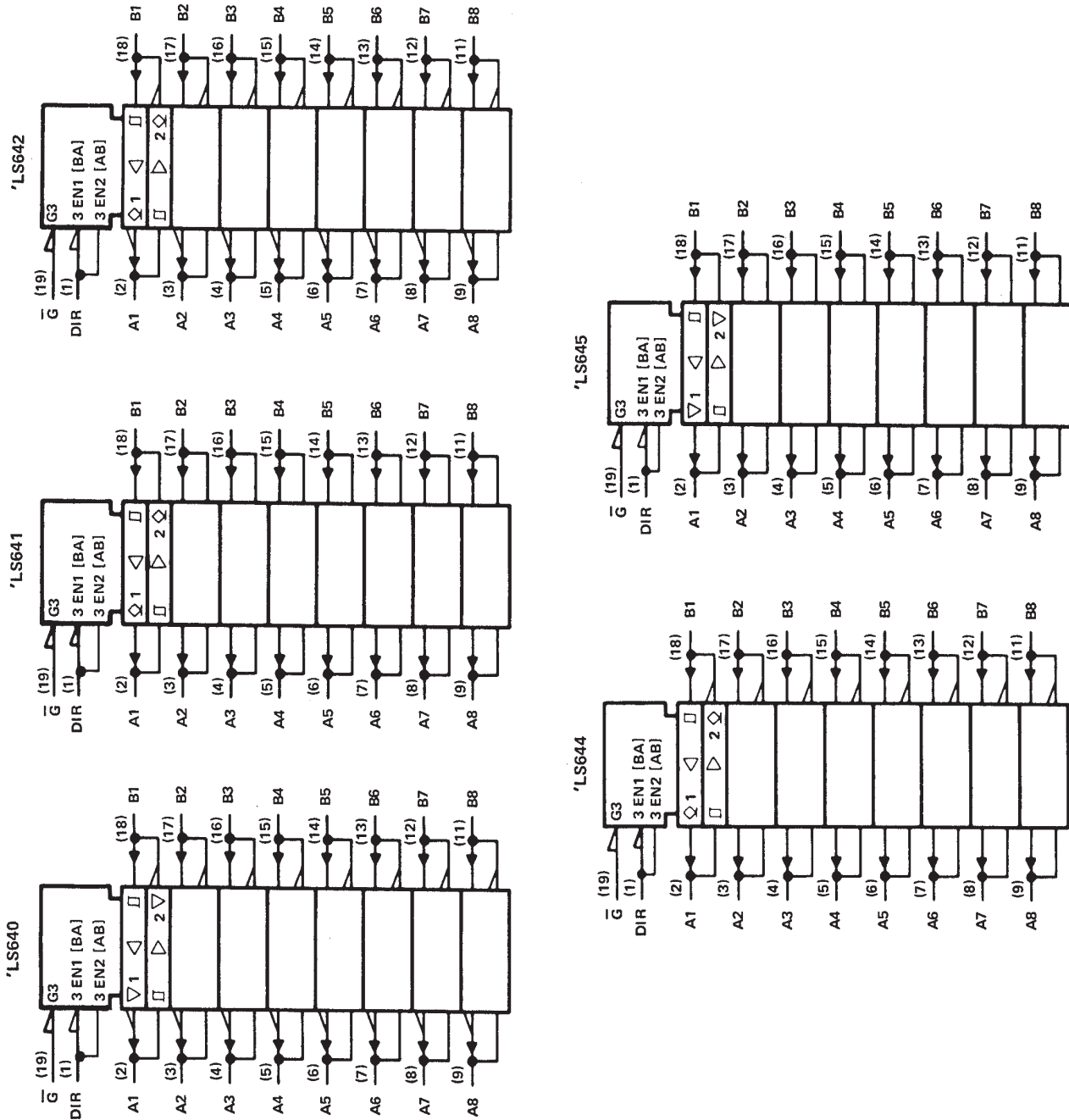
CONTROL INPUTS		OPERATION		
		'LS640 'LS642	'LS641 'LS645	'LS644
\bar{G}	DIR	B data to A bus	B data to A bus	B data to A bus
L	L	A data to B bus	A data to B bus	\bar{A} data to B bus
L	H	A data to B bus	A data to B bus	\bar{A} data to B bus
H	X	Isolation	Isolation	Isolation

H = high level, L = low level, X = irrelevant

SN54LS640 THRU SN54LS642, SN54LS644, SN54LS645 SN74LS640 THRU SN74LS642, SN74LS644, SN74LS645 OCTAL BUS TRANSCEIVERS

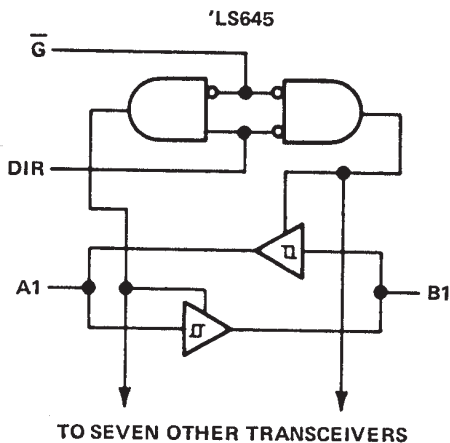
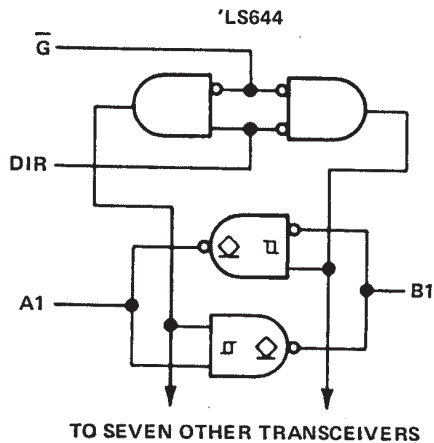
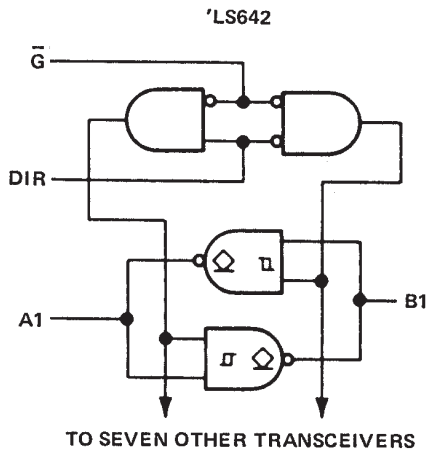
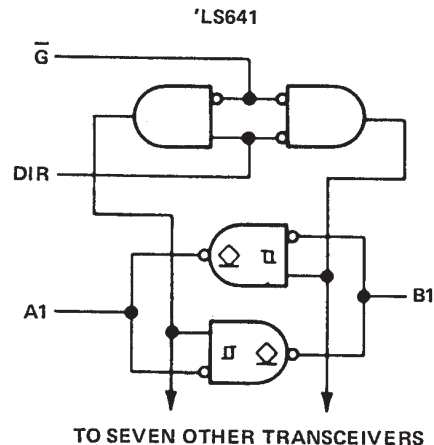
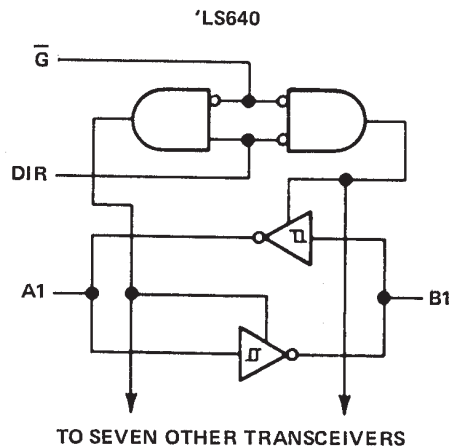
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logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagrams (positive logic)



SN54LS640, SN54LS645
SN74LS640, SN74LS645
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54LS640, SN54LS645	-55 °C to 125 °C
SN74LS640, SN74LS645	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER	SN54LS640 SN54LS645			SN74LS640 SN74LS645			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.5			0.6	V
I_{OH} High-level output current			-12			-15	mA
I_{OL} Low-level output current			12			24	mA
						48†	
T_A Operating free-air temperature	-55		125	0		70	°C

†The 48-mA limit applies for the SN74LS640-1 and SN74LS645-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS640 SN54LS645			SN74LS640 SN74LS645			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V	
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN},$ A or B input	0.1	0.4		0.2	0.4		V	
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = \text{MAX}$	$I_{OH} = -3 \text{ mA}$	2.4	3.4	2.4	3.4			
		$I_{OH} = \text{MAX}$	2		2				
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = \text{MAX}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4	0.25	0.4		V	
		$I_{OL} = 24 \text{ mA}$			0.35	0.5			
		$I_{OL} = 48 \text{ mA}^\#$			0.4	0.5			
I_{OZH}	$V_{CC} = \text{MAX}, \bar{G} \text{ at } 2 \text{ V}, V_O = 2.7 \text{ V}$			20			20	µA	
I_{OZL}	$V_{CC} = \text{MAX}, \bar{G} \text{ at } 2 \text{ V}, V_O = 0.4 \text{ V}$			-0.4			-0.4	mA	
I_I	A or B DIR or \bar{G}	$V_{CC} = \text{MAX}$	$V_I = 5.5 \text{ V}$			0.1		0.1	mA
			$V_I = 7 \text{ V}$			0.1		0.1	
I_{IH}	$V_{CC} = \text{MAX}, V_{IH} = 2.7 \text{ V}$			20			20	µA	
I_{IL}	$V_{CC} = \text{MAX}, V_{IL} = 0.4 \text{ V}$			-0.4			-0.4	mA	
I_{OS}^\ddagger	$V_{CC} = \text{MAX}$	-40		-225	-40		-225	mA	
I_{CC}	Outputs high		48	70		48	70	mA	
	Outputs low		62	90		62	90		
	Outputs at Hi-Z		64	95		64	95		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25 \text{ °C}$.

¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

#The 48-mA condition applies for the SN74LS640-1 and SN74LS645-1 only.



SN54LS640, SN54LS645
SN74LS640, SN74LS645
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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switching characteristics, $V_{CC} = 5 V$, $T_A = 25^\circ C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS640, 'LS640-1			'LS645, 'LS645-1			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	A	B	$C_L = 45 \text{ pF}$, $R_L = 667 \Omega$, See Note 2		6	10		8	15	ns
	B	A			6	10		8	15	
t_{PHL} Propagation delay time, high-to-low-level output	A	B			8	15		11	15	ns
	B	A			8	15		11	15	
t_{PZL} Output enable time to low level	\overline{G}	A			31	40		31	40	ns
	\overline{G}	B			31	40		31	40	
t_{PZH} Output enable time to high level	\overline{G}	A			23	40		26	40	ns
	\overline{G}	B			23	40		26	40	
t_{PLZ} Output disable time from low level	\overline{G}	A	$C_L = 5 \text{ pF}$, $R_L = 667 \Omega$, See Note 2		15	25		15	25	ns
	\overline{G}	B			15	25		15	25	
t_{PHZ} Output disable time from high level	\overline{G}	A			15	25		15	25	ns
	\overline{G}	B			15	25		15	25	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



TYPICAL CHARACTERISTICS

SN54LS'
 INVERTING OUTPUT VOLTAGE
 vs
 INPUT VOLTAGE

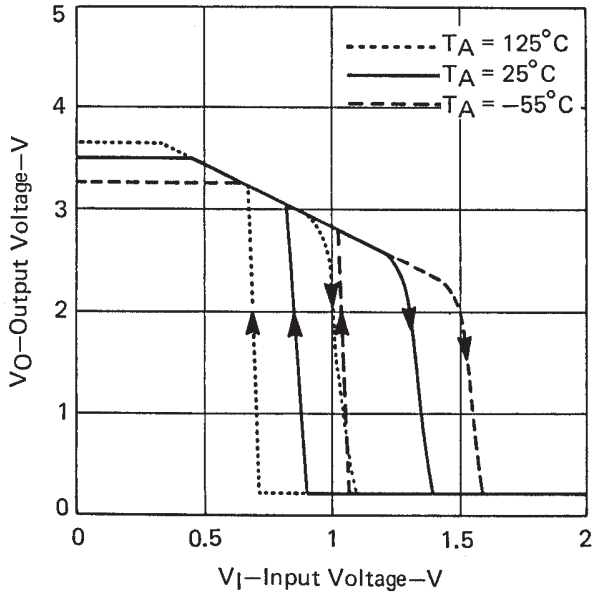


FIGURE 1

SN74LS'
 INVERTING OUTPUT VOLTAGE
 vs
 INPUT VOLTAGE



FIGURE 2

SN54LS'
 NONINVERTING OUTPUT VOLTAGE
 vs
 INPUT VOLTAGE

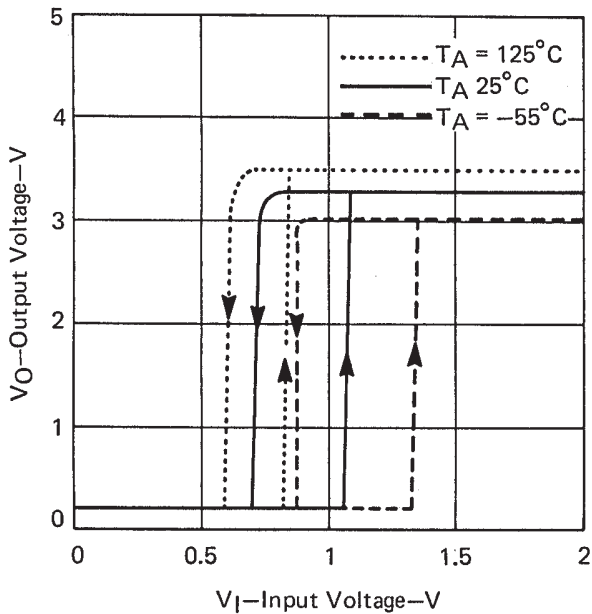


FIGURE 3

SN74LS'
 NONINVERTING OUTPUT VOLTAGE
 vs
 INPUT VOLTAGE



FIGURE 4

SN54LS641, SN54LS642, SN54LS644
SN74LS641, SN74LS642, SN74LS644
OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: All inputs and I/O ports	7 V
Operating free-air temperature range: SN54LS641, SN54LS642, SN54LS644	– 55° C to 125° C
SN74LS641, SN74LS642, SN74LS644	0° C to 70° C
Storage temperature range	– 65° C to 150° C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER	SN54LS641 SN54LS642 SN54LS644			SN74LS641 SN74LS642 SN74LS644			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
	V_{CC} Supply voltage	4.5	5	5.5	4.75	5	
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage	0.5			0.6			V
V_{OH} High-level output voltage	5.5			5.5			V
I_{OL} Low-level output current	12			24			mA
				48 §			
T_A Operating free-air temperature	– 55		125	0		70	°C

§ The 48 mA limit applies for the SN74LS641-1, SN74LS642-1, and SN74LS644-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS641 SN54LS642 SN54LS644			SN74LS641 SN74LS642 SN74LS644			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
		V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	– 1.5			– 1.5	
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}, A \text{ or } B \text{ input}$	0.1	0.4		0.2	0.4		V
I_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, V_{OH} = 5.5 \text{ V}$	0.1			0.1			mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4	0.25	0.4	V	
		$I_{OL} = 24 \text{ mA}$			0.35	0.5		
		$I_{OL} = 48 \text{ mA} §$			0.4	0.5		
I_I	A or B	$V_{CC} = \text{MAX}$	$V_I = 5.5 \text{ V}$	0.1		0.1		mA
	DIR or \bar{G}		$V_I = 7 \text{ V}$	0.1		0.1		
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	20			20			µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	– 0.4			– 0.4			mA
I_{CC}	Outputs high	$V_{CC} = \text{MAX},$ Outputs open	48	70	48	70	mA	
	Outputs low		62	90	62	90		
	Outputs at Hi-Z		64	95	64	95		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ The 48 mA condition applies for the SN74LS641-1, SN74LS642-1, and SN74LS644-1 only.



SN54LS641, SN54LS642, SN54LS644
 SN74LS641, SN74LS642, SN74LS644
 OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

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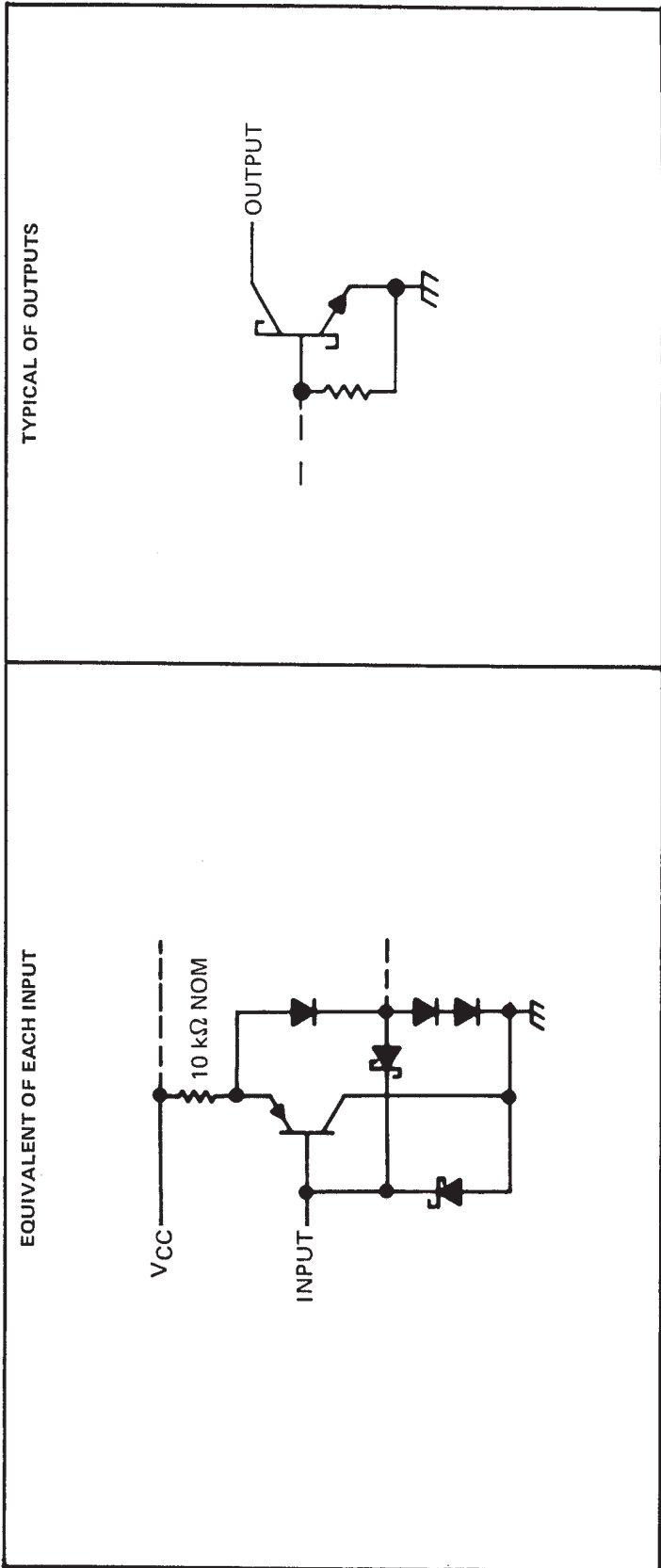
switching characteristics at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'LS641, 'LS641-1		'LS642, 'LS642-1		'LS644, 'LS644-1		UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH} Propagation delay time, low-to-high-level output	A	B	17	25	19	25	17	25	ns
	B	A	17	25	19	25	19	25	
t _{PHL} Propagation delay time, high-to-low-level output	A	B	16	25	14	25	14	25	ns
	B	A	16	25	14	25	16	25	
t _{PLH} Output disable time from low level	\bar{G} , DIR	A	23	40	26	40	26	40	ns
	\bar{G} , DIR	B	25	40	28	40	25	40	
t _{PHL} Output enable time from high level	\bar{G} , DIR	A	34	50	43	60	43	60	ns
	\bar{G} , DIR	B	37	50	39	60	37	50	

TEST CONDITIONS
 $C_L = 45\text{ pF}$,
 $R_L = 667\ \Omega$,
 See Note 2

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



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SN54LS640, OCTAL BUS TRANSCEIVERS

Device Status: Active

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- > [Features](#)
- > [Datasheets](#)
- > [Pricing/Samples/Availability](#)
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- > [Related Documents](#)

Parameter Name	SN54LS640
Voltage Nodes (V)	5
Vcc range (V)	4.5 to 5.5
Input Level	TTL
Output Level	TTL
No. of Outputs	8
Logic	Inv

Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G \setminus) can be used to disable the device so the buses are effectively isolated.

The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C.

Features

- SN74LS64X-1 Versions Rated at I_{OL} of 48 mA
- Bi-directional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

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Datasheets

Full datasheet in Acrobat PDF: [sdls189.pdf](#) (336 KB)

Full datasheet in Zipped PostScript: [sdls189.psz](#) (626 KB)

Pricing/Samples/Availability

<u>Orderable Device</u>	<u>Package</u>	<u>Pins</u>	<u>Temp (°C)</u>	<u>Status</u>	<u>Price/unit USD (100-999)</u>	<u>Pack Qty</u>	<u>DSCC Number</u>	<u>Availability / Samples</u>
SN54LS640J	J	20	-55 TO 125	ACTIVE	4.33	1		Check stock or order
SNJ54LS640FK	FK	20	-55 TO 125	ACTIVE	10.02	1	84161012A	Check stock or order
SNJ54LS640J	J	20	-55 TO 125	ACTIVE	5.09	1	8416101RA	Check stock or order
SNJ54LS640W	W	20	-55 TO 125	ACTIVE	12.78	1	8416101SA	Check stock or order

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- [LOGIC SOLUTIONS FOR IEEE STD 1284 \(SCEA013](#) - Updated: 06/27/1999)
- [LVT-TO-LVTH CONVERSION \(SCEA010](#) - Updated: 02/05/1999)

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- [DOCUMENTATION RULES \(SAP\) AND ORDERING INFORMATION \(SZZU001B](#), 4 KB - Updated: 05/06/1999)
- [LOGIC SELECTION GUIDE SECOND HALF 2000 \(SDYU001N](#), 5035 KB - Updated: 04/17/2000)
- [MORE POWER IN LESS SPACE - TECHNICAL ARTICLE \(SCAU001A](#), 850 KB - Updated: 03/01/1996)

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