FAIRCHILD SEMICONDUCTOR®

March 1994
Revised May 2005

74ABT16373
16-Bit Transparent D-Type Latch with 3-STATE Outputs

General Description

The ABT16373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the outputs are in high Z state.

Features

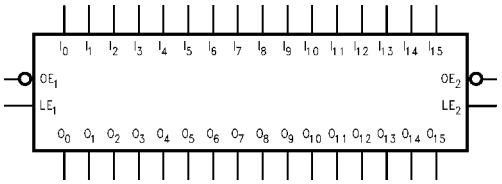
- Separate control logic for each byte
- 16-bit version of the ABT373
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Guaranteed latch-up protection

Ordering Code:

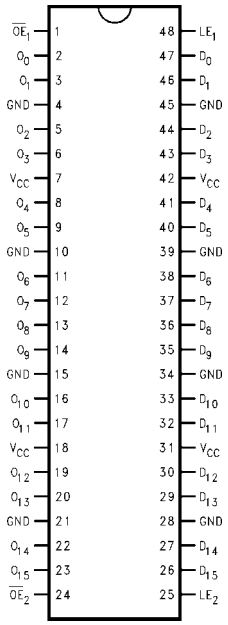
Order Number	Package Number	Package Description
74ABT16373CSSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ABT16373CMTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
LE_n	Latch Enable Input
D_0–D_{15}	Data Inputs
O_0–O_{15}	Outputs

Functional Description

The ABT16373 contains sixteen D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e., a latch output will change states each time its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The 3-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

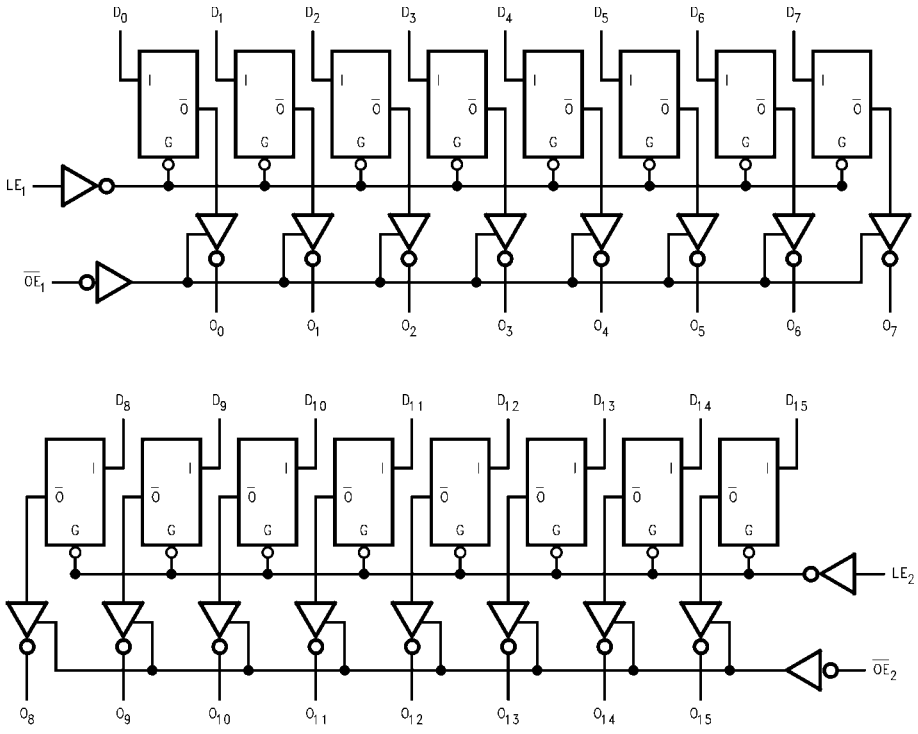
Truth Tables

Inputs			Outputs
LE_1	$\overline{OE}_1$	D_0–D_7	O_0–O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	(Previous)

Inputs			Outputs
LE_2	$\overline{OE}_2$	D_8–D_{15}	O_8–O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	(Previous)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
Previous = previous output prior to HIGH-to-LOW transition of LE

Logic Diagrams



Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current: $\overline{OE}$ Pin	−350 mA
(Across Comm Operating Range)	
Other Pins	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	−40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage		2.5				Min	I_{OH} = −3 mA
			2.0					I_{OH} = −32 mA
V_{OL}	Output LOW Voltage				0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current				1	μA	Max	V_{IN} = 2.7V (Note 3)
					1			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−1	μA	Max	V_{IN} = 0.5V (Note 3)
					−1			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA
								All Other Pins Grounded
I_{OZH}	Output Leakage Current				10	μA	0 – 5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V
I_{OZL}	Output Leakage Current				−10	μA	0 – 5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output HIGH Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				2.0	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				62	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				2.0	mA	Max	$\overline{OE}$ = V_{CC}
								All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA		V_I = V_{CC} − 2.1V
		Outputs 3-STATE			2.5	mA	Max	Enable Input V_I = V_{CC} − 2.1V
		Outputs 3-STATE			2.5	mA		Data Input V_I = V_{CC} − 2.1V
								All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC}	No Load				mA/	Max	Outputs Open, LE = V_{CC}
	(Note 3)				0.15	MHz		$\overline{OE}$ = GND, (Note 4)
								One Bit Toggling, 50% Duty Cycle

Note 3: Guaranteed, but not tested.

Note 4: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

AC Electrical Characteristics

(SOIC and SSOP Packages)

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	1.4		5.6	1.4	5.6	ns
t_{PHL}	D_n to O_n	1.4		5.6	1.4	5.6	
t_{PLH}	Propagation Delay	1.7		6.0	1.7	6.0	ns
t_{PHL}	LE to O_n	1.7		5.5	1.7	5.5	
t_{PZH}	Output Enable Time	1.1		6.1	1.1	6.1	ns
t_{PZL}		1.5		5.6	1.5	5.6	
t_{PHZ}	Output Disable Time	2.4		7.1	2.4	7.1	ns
t_{PLZ}		1.6		6.5	1.6	6.5	

AC Operating Requirements

(SOIC and SSOP Packages)

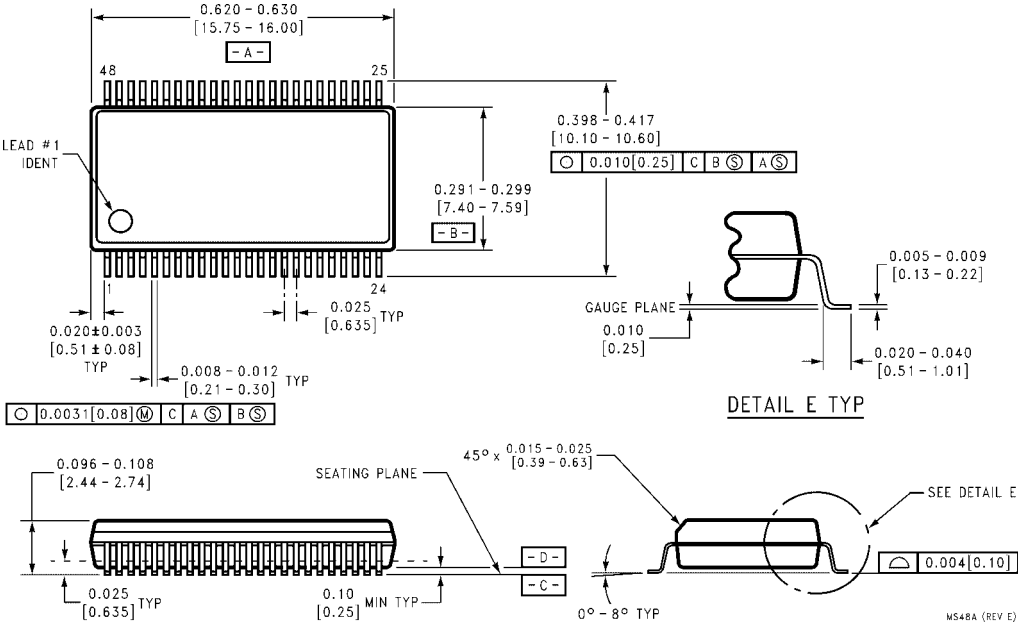
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{TOGGLE}	Maximum Toggle Frequency		100				MHz
$t_S(H)$	Setup Time, HIGH	1.5			1.5		ns
$t_S(L)$	or LOW D_n to LE	1.5			1.5		
$t_H(H)$	Hold Time, HIGH	1.0			1.0		ns
$t_H(L)$	or LOW D_n to LE	1.0			1.0		
$t_W(H)$	Pulse Width, LE HIGH	3.0			3.0		ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions ($T_A = 25°C$)
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0V$
C_{OUT} (Note 5)	Output Capacitance	11	pF	$V_{CC} = 5.0V$

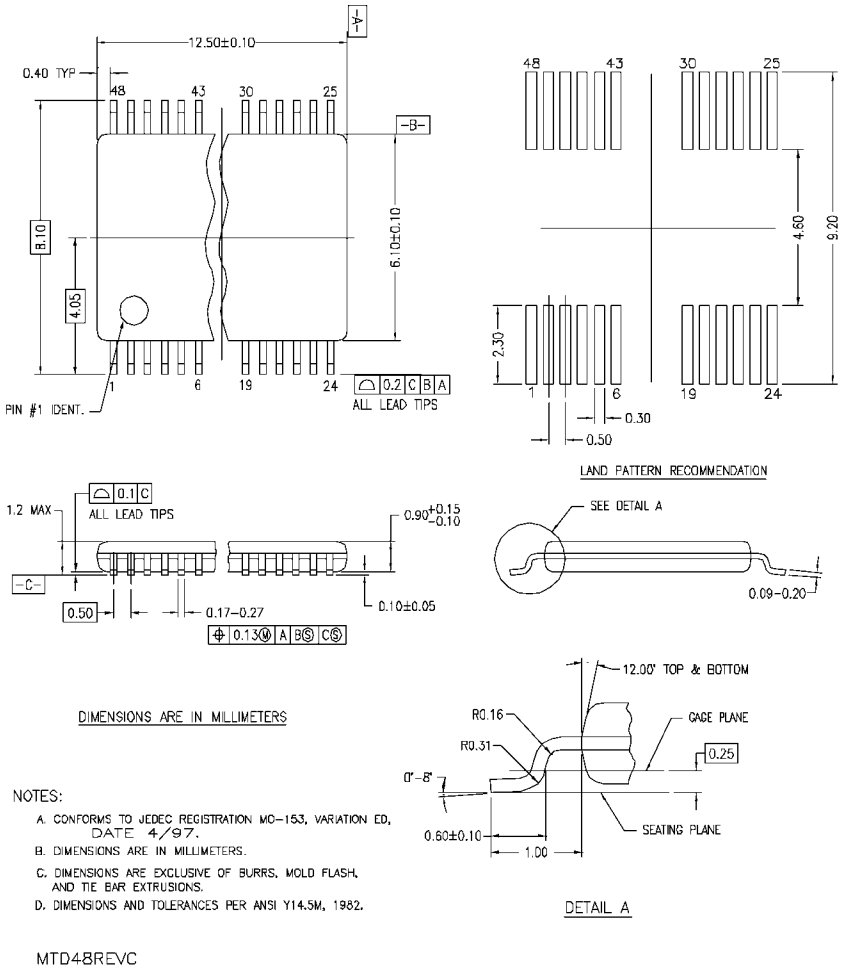
Note 5: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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