

Dual Common Base-Collector Bias Resistor Transistors

NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

UMC2NT1G, NSVUMC2NT1G, UMC3NT1G, NSVUMC3NT1G, UMC5NT1G/T2G, NSVUMC5NT1G/T2G

The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the UMC2NT1G series, two complementary BRT devices are housed in the SOT-353 package which is ideal for low power surface mount applications where board space is at a premium.

Features

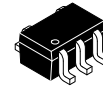
- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch/3000 Unit Tape and Reel
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant*

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q_1 and Q_2 , - minus sign for Q_1 (PNP) omitted)

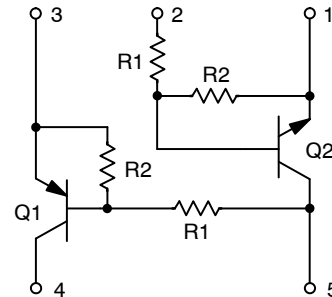
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

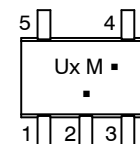
*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



SC-88A/SOT-353
CASE 419A
STYLE 6



MARKING DIAGRAM



- Ux = Device Marking
- x = 2, 3 or 5
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

UMC2NT1G, NSVUMC2NT1G, UMC3NT1G, NSVUMC3NT1G, UMC5NT1G/T2G, NSVUMC5NT1G/T2G

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q_1 and Q_2 , – minus sign for Q_1 (PNP) omitted)

Rating	Symbol	Value	Unit
THERMAL CHARACTERISTICS			
Thermal Resistance – Junction-to-Ambient (surface mounted)	$R_{\theta JA}$	833	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$
Total Package Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1)	P_D	150	mW

1. Device mounted on a FR-4 glass epoxy printed circuit board using the minimum recommended footprint.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Q1 TRANSISTOR: PNP

OFF CHARACTERISTICS

Collector-Base Cutoff Current ($V_{CB} = 50\text{ V}, I_E = 0$)	I_{CBO}	–	–	100	nAdc
Collector-Emitter Cutoff Current ($V_{CE} = 50\text{ V}, I_B = 0$)	I_{CEO}	–	–	500	nAdc
Emitter-Base Cutoff Current ($V_{EB} = 6.0, I_C = 0\text{ mA}$) UMC2NT1G, NSVUMC2NT1G UMC3NT1G, NSVUMC3NT1G UMC5NT1G/T2G, NSVUMC5NT1G/T2G	I_{EBO}	–	–	0.2 0.5 1.0	mAdc

ON CHARACTERISTICS

Collector-Base Breakdown Voltage ($I_C = 10\ \mu\text{A}, I_E = 0$)	$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage ($I_C = 2.0\text{ mA}, I_B = 0$)	$V_{(BR)CEO}$	50	–	–	Vdc
DC Current Gain ($V_{CE} = 10\text{ V}, I_C = 5.0\text{ mA}$) UMC2NT1G, NSVUMC2NT1G UMC3NT1G, NSVUMC3NT1G UMC5NT1G/T2G, NSVUMC5NT1G/T2G	h_{FE}	60 35 20	100 60 35	– – –	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ mA}, I_B = 0.3\text{ mA}$)	$V_{CE(SAT)}$	–	–	0.25	Vdc
Output Voltage (on) ($V_{CC} = 5.0\text{ V}, V_B = 2.5\text{ V}, R_L = 1.0\text{ k}\Omega$)	V_{OL}	–	–	0.2	Vdc
Output Voltage (off) ($V_{CC} = 5.0\text{ V}, V_B = 0.5\text{ V}, R_L = 1.0\text{ k}\Omega$)	V_{OH}	4.9	–	–	Vdc
Input Resistor UMC2NT1G UMC3NT1G UMC5NT1G/T2G	R1	15.4 7.0 3.3	22 10 4.7	28.6 13 6.1	k Ω
Resistor Ratio UMC2NT1G UMC3NT1G UMC5NT1G/T2G	R1/R2	0.8 0.8 0.38	1.0 1.0 0.47	1.2 1.2 0.56	

**UMC2NT1G, NSVUMC2NT1G, UMC3NT1G, NSVUMC3NT1G, UMC5NT1G/T2G,
NSVUMC5NT1G/T2G**

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Q2 TRANSISTOR: NPN
OFF CHARACTERISTICS**

Collector-Base Cutoff Current ($V_{CB} = 50\text{ V}$, $I_E = 0$)	I_{CBO}	-	-	100	nAdc
Collector-Emitter Cutoff Current ($V_{CE} = 50\text{ V}$, $I_B = 0$)	I_{CEO}	-	-	500	nAdc
Emitter-Base Cutoff Current ($V_{EB} = 6.0$, $I_C = 0\text{ mA}$) UMC2NT1G UMC3NT1G UMC5NT1G/T2G	I_{EBO}	- - -	- - -	0.2 0.5 0.1	mAdc

ON CHARACTERISTICS

Collector-Base Breakdown Voltage ($I_C = 10\text{ }\mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	50	-	-	Vdc
Collector-Emitter Breakdown Voltage ($I_C = 2.0\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	50	-	-	Vdc
DC Current Gain ($V_{CE} = 10\text{ V}$, $I_C = 5.0\text{ mA}$) UMC2NT1G UMC3NT1G UMC5NT1G/T2G	h_{FE}	60 35 80	100 60 140	- - -	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ mA}$, $I_B = 0.3\text{ mA}$)	$V_{CE(SAT)}$	-	-	0.25	Vdc
Output Voltage (on) ($V_{CC} = 5.0\text{ V}$, $V_B = 3.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	V_{OL}	-	-	0.2	Vdc
Output Voltage (off) ($V_{CC} = 5.0\text{ V}$, $V_B = 0.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	V_{OH}	4.9	-	-	Vdc
Input Resistor UMC2NT1G UMC3NT1G UMC5NT1G/T2G	R1	15.4 7.0 33	22 10 47	28.6 13 61	k Ω
Resistor Ratio UMC2NT1G UMC3NT1G UMC5NT1G/T2G	R1/R2	0.8 0.8 0.8	1.0 1.0 1.0	1.2 1.2 1.2	

UMC2NT1G, NSVUMC2NT1G, UMC3NT1G, NSVUMC3NT1G, UMC5NT1G/T2G, NSVUMC5NT1G/T2G

ORDERING INFORMATION

Device	Package	Shipping [†]
UMC2NT1G, NSVUMC2NT1G*	SC-88A/SOT-353 (Pb-Free)	3,000 / Tape & Reel
UMC3NT1G, NSVUMC3NT1G*	SC-88A/SOT-353 (Pb-Free)	3,000 / Tape & Reel
UMC3NT2G	SC-88A/SOT-353 (Pb-Free)	3,000 / Tape & Reel
UMC5NT1G, NSVUMC5NT1G*	SC-88A/SOT-353 (Pb-Free)	3,000 / Tape & Reel
UMC5NT2G, NSVUMC5NT2G*	SC-88A/SOT-353 (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

DEVICE MARKING AND RESISTOR VALUES

Device	Marking	Transistor 1 - PNP		Transistor 2 - NPN	
		R1 (K)	R2 (K)	R1 (K)	R2 (K)
UMC2NT1G, NSVUMC2NT1G	U2	22	22	22	22
UMC3NT1G, NSVUMC3NT1G	U3	10	10	10	10
UMC3NT2G	U3	10	10	10	10
UMC5NT1G, NSVUMC5NT1G	U5	4.7	10	47	47
UMC5NT2G, NSVUMC5NT2G	U5	4.7	10	47	47

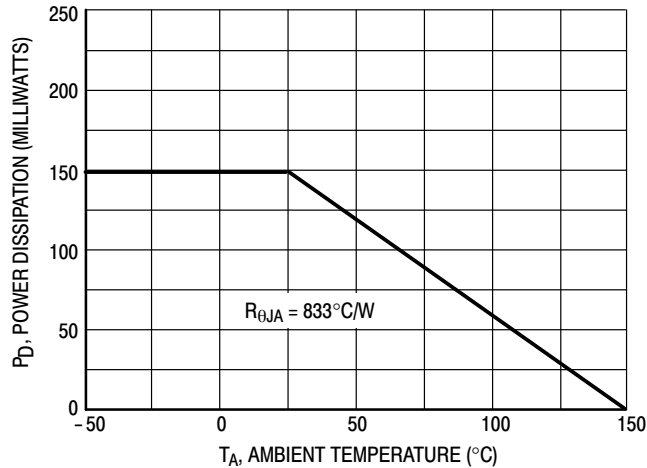


Figure 1. Derating Curve

UMC2NT1G, NSVUMC2NT1G, UMC3NT1G, NSVUMC3NT1G, UMC5NT1G/T2G, NSVUMC5NT1G/T2G

TYPICAL ELECTRICAL CHARACTERISTICS — UMC2NT1G, NSVUMC2NT1G PNP TRANSISTOR

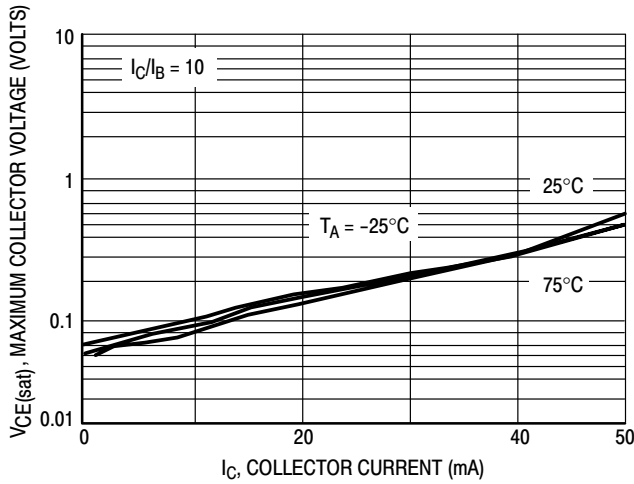


Figure 2. $V_{CE(sat)}$ versus I_C

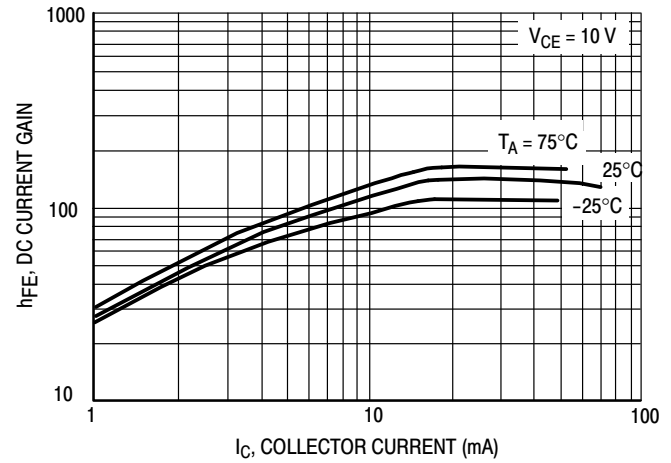


Figure 3. DC Current Gain

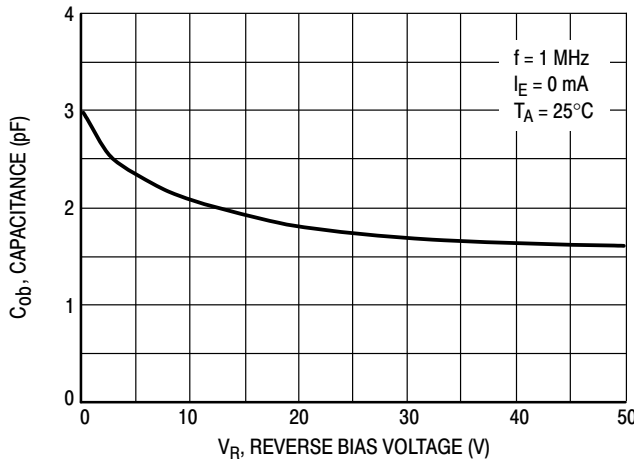


Figure 4. Output Capacitance

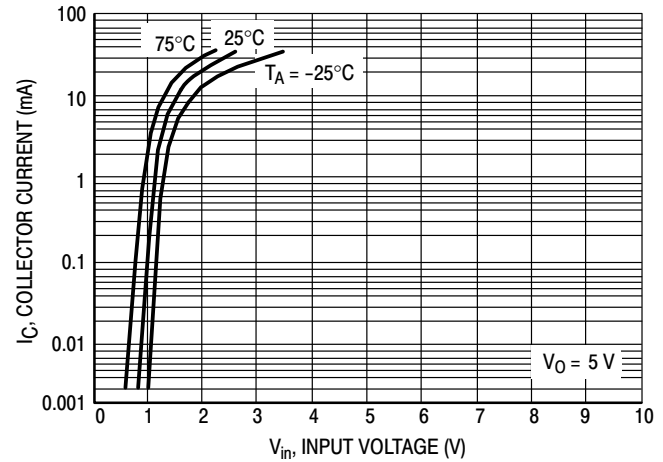


Figure 5. Output Current versus Input Voltage

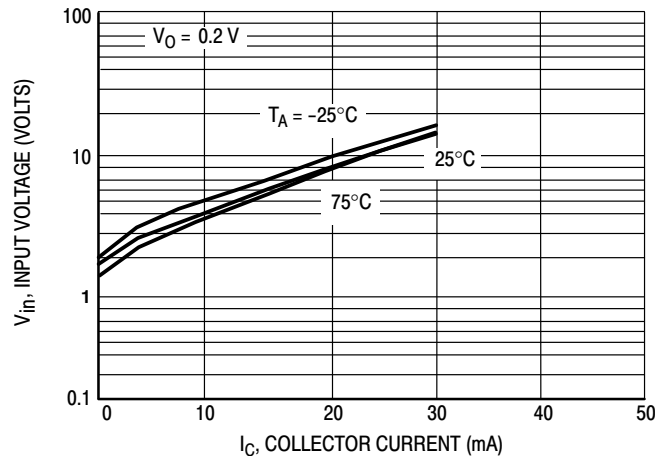


Figure 6. Input Voltage versus Output Current

UMC2NT1G, NSVUMC2NT1G, UMC3NT1G, NSVUMC3NT1G, UMC5NT1G/T2G, NSVUMC5NT1G/T2G

TYPICAL ELECTRICAL CHARACTERISTICS — UMC2NT1G, NSVUMC2NT1G NPN TRANSISTOR

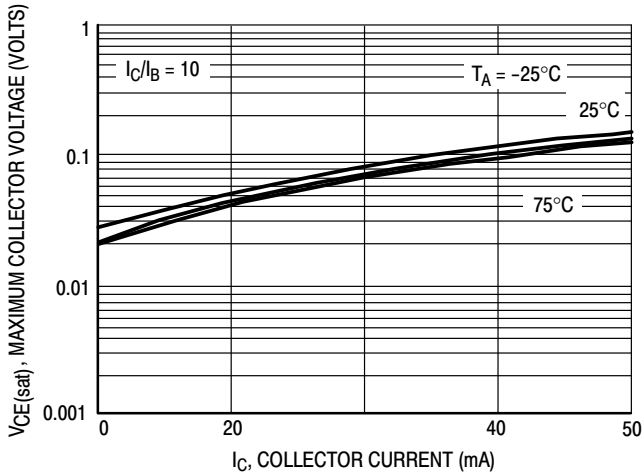


Figure 7. $V_{CE(sat)}$ versus I_C

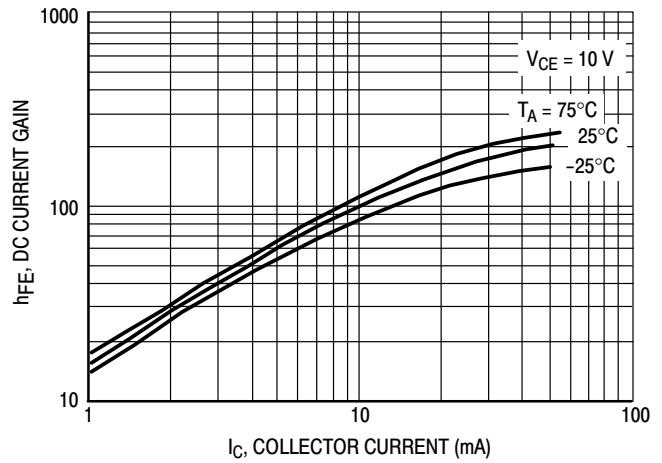


Figure 8. DC Current Gain

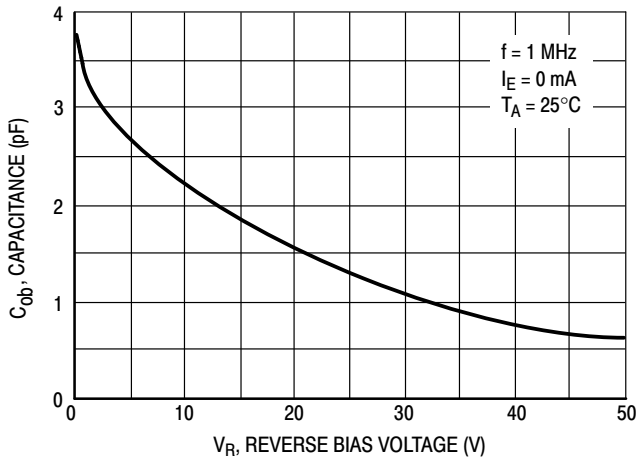


Figure 9. Output Capacitance

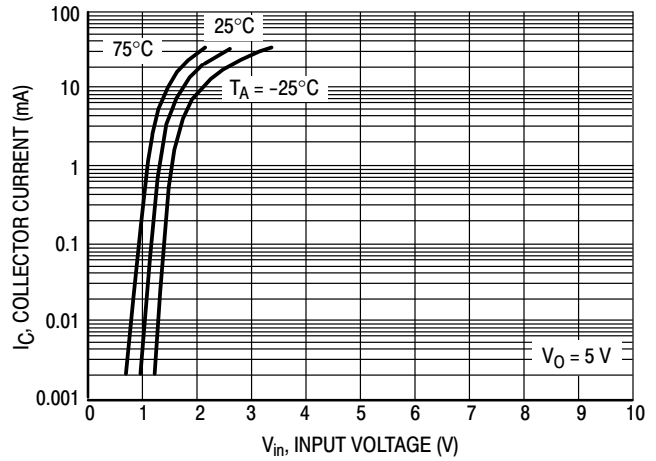


Figure 10. Output Current versus Input Voltage

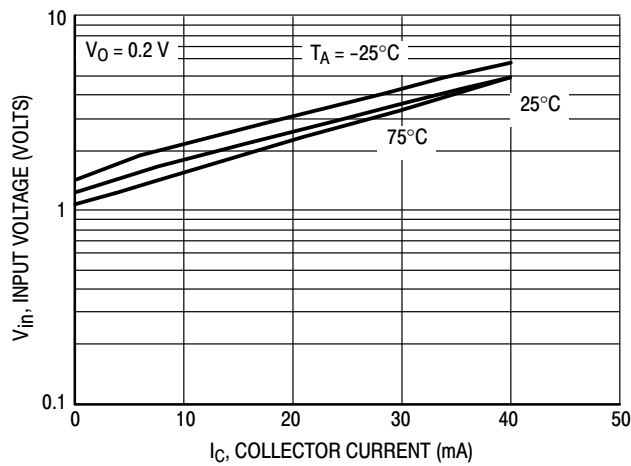


Figure 11. Input Voltage versus Output Current

UMC2NT1G, NSVUMC2NT1G, UMC3NT1G, NSVUMC3NT1G, UMC5NT1G/T2G, NSVUMC5NT1G/T2G

TYPICAL ELECTRICAL CHARACTERISTICS — UMC3NT1G PNP TRANSISTOR

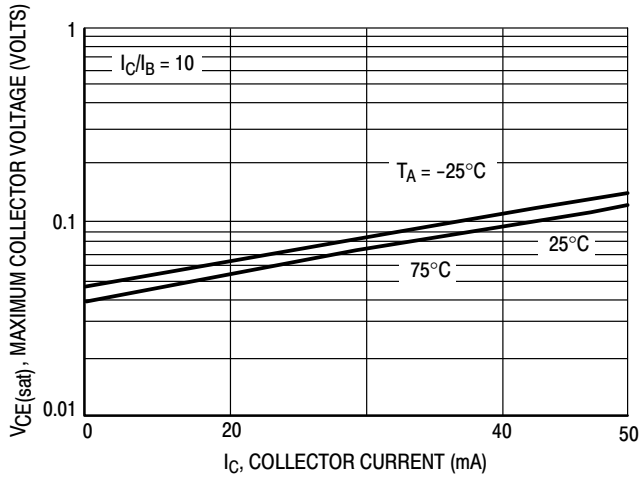


Figure 12. $V_{CE(sat)}$ versus I_C

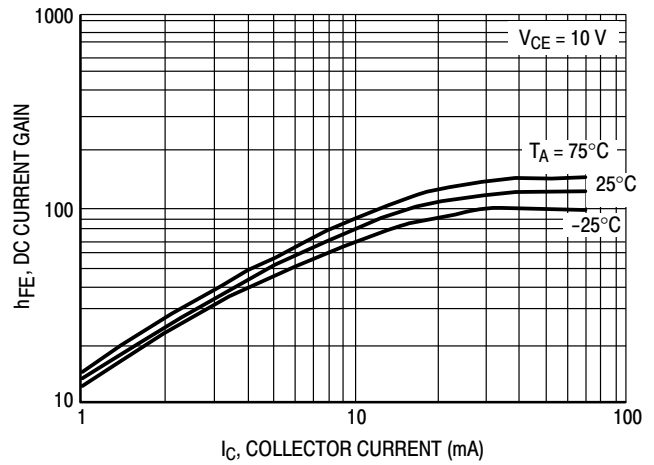


Figure 13. DC Current Gain

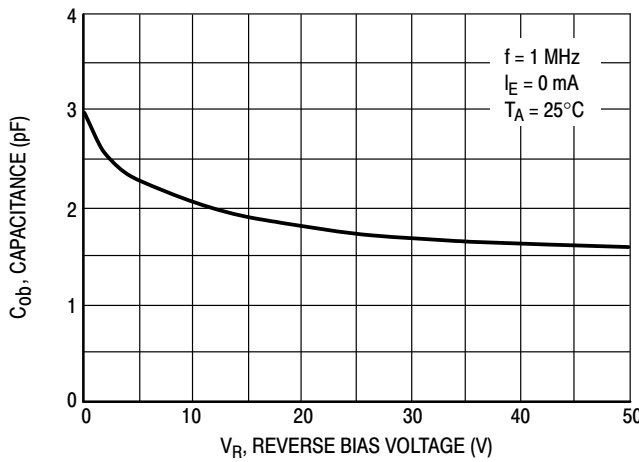


Figure 14. Output Capacitance

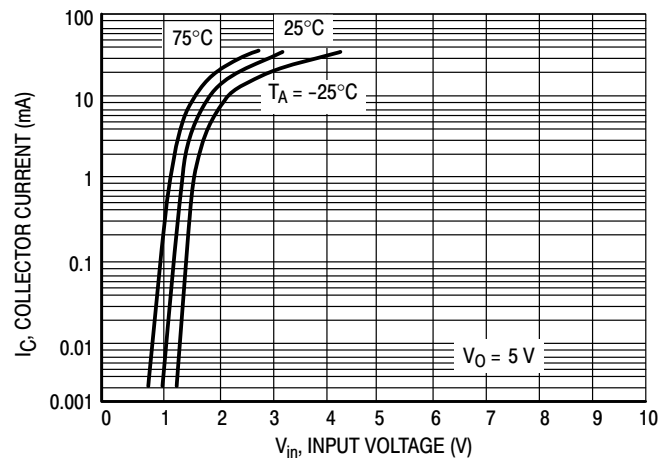


Figure 15. Output Current versus Input Voltage

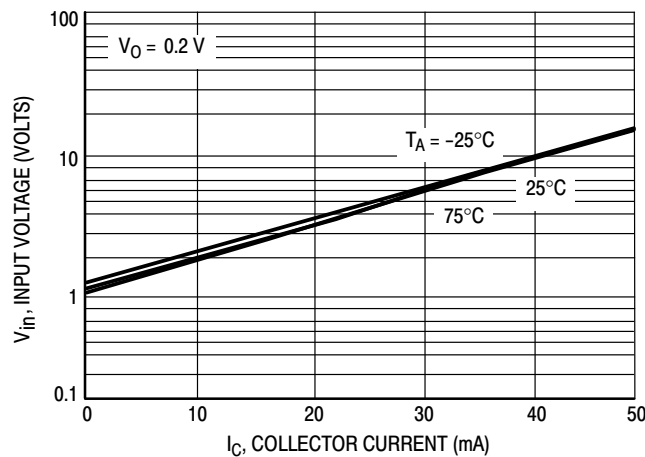


Figure 16. Input Voltage versus Output Current

UMC2NT1G, NSVUMC2NT1G, UMC3NT1G, NSVUMC3NT1G, UMC5NT1G/T2G,
NSVUMC5NT1G/T2G

TYPICAL ELECTRICAL CHARACTERISTICS — UMC3NT1G NPN TRANSISTOR

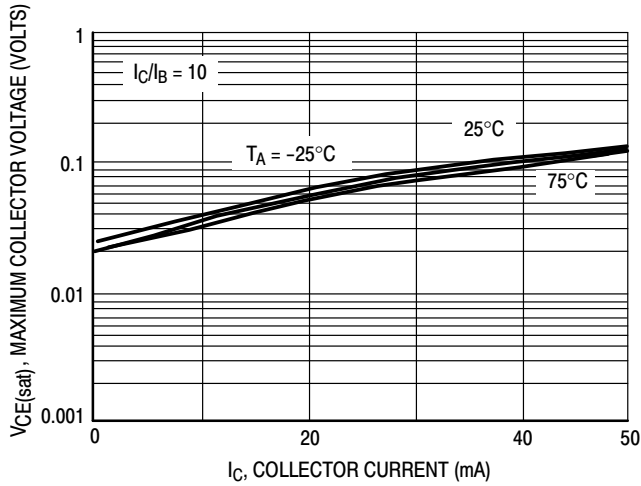


Figure 17. $V_{CE(sat)}$ versus I_C

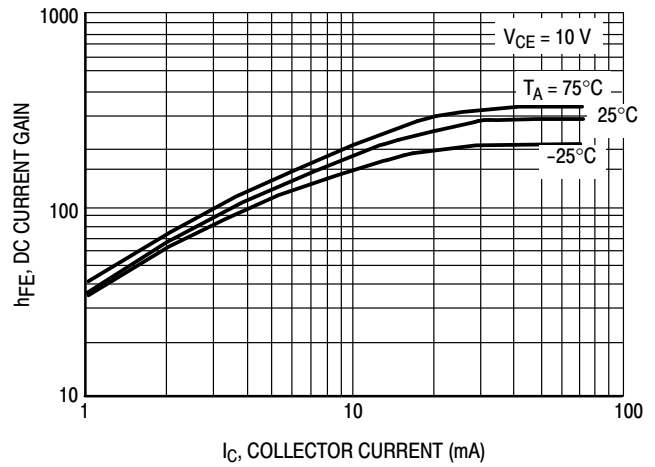


Figure 18. DC Current Gain

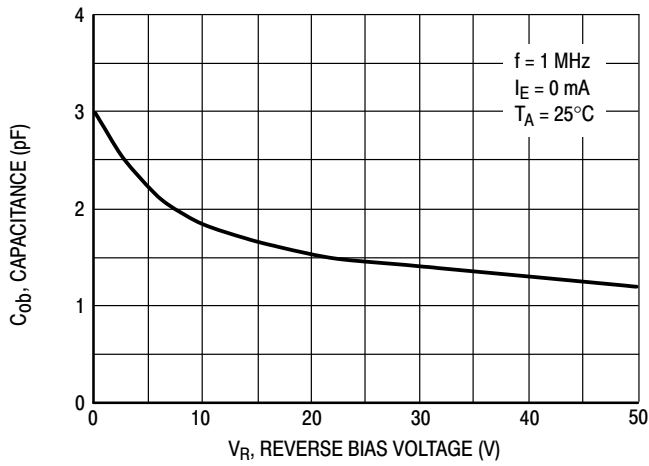


Figure 19. Output Capacitance

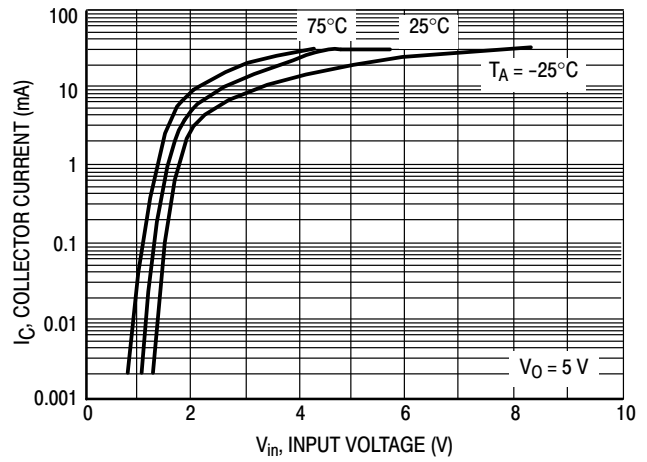


Figure 20. Output Current versus Input Voltage

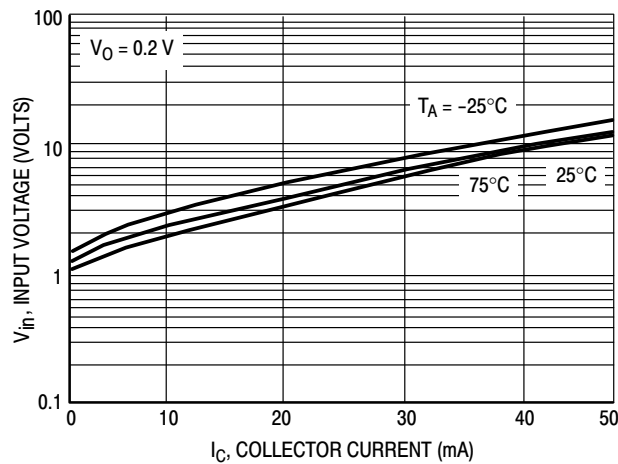


Figure 21. Input Voltage versus Output Current

UMC2NT1G, NSVUMC2NT1G, UMC3NT1G, NSVUMC3NT1G, UMC5NT1G/T2G,
NSVUMC5NT1G/T2G

TYPICAL ELECTRICAL CHARACTERISTICS — UMC5NT1G PNP TRANSISTOR

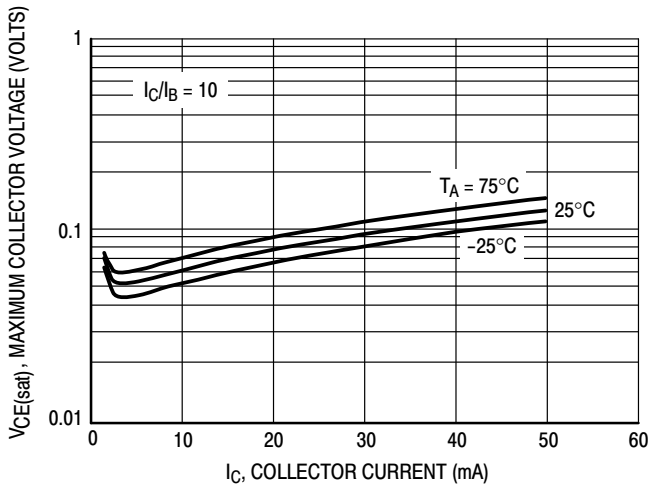


Figure 22. $V_{CE(sat)}$ versus I_C

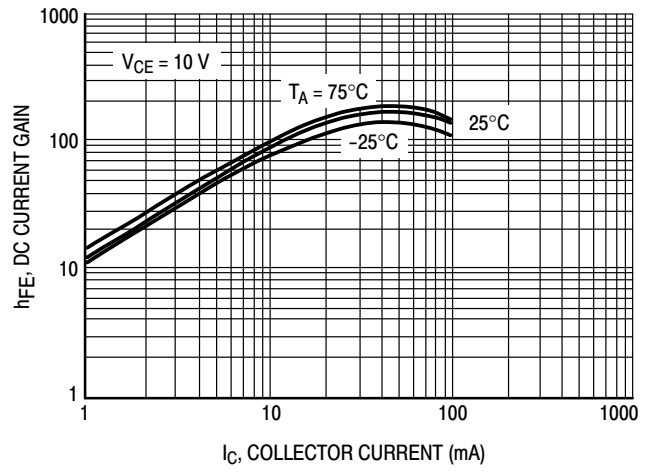


Figure 23. DC Current Gain

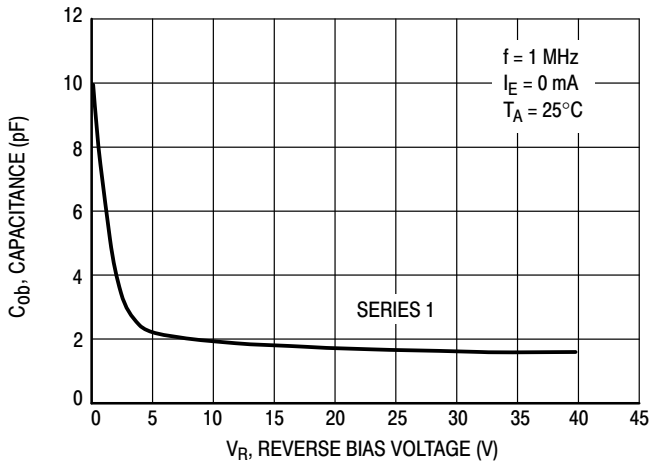


Figure 24. Output Capacitance

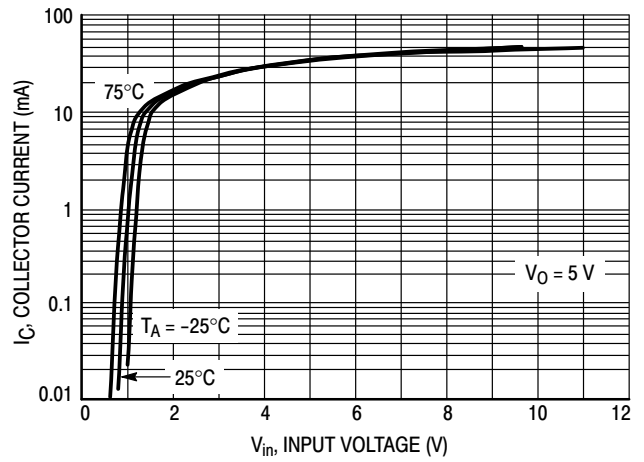


Figure 25. Output Current versus Input Voltage

UMC2NT1G, NSVUMC2NT1G, UMC3NT1G, NSVUMC3NT1G, UMC5NT1G/T2G,
NSVUMC5NT1G/T2G

TYPICAL ELECTRICAL CHARACTERISTICS — UMC5NT1G NPN TRANSISTOR

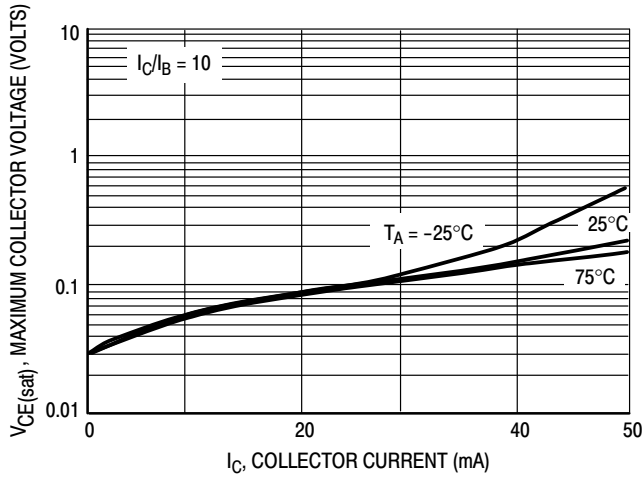


Figure 26. $V_{CE(sat)}$ versus I_C

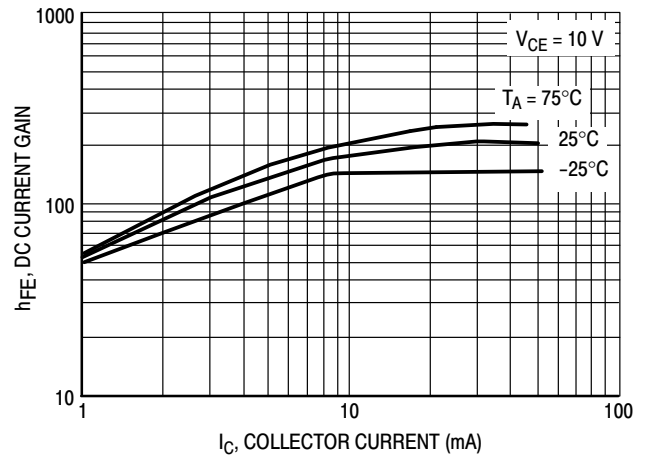


Figure 27. DC Current Gain

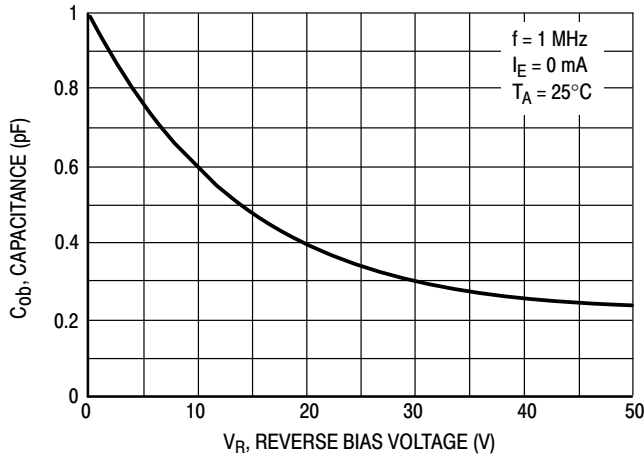


Figure 28. Output Capacitance

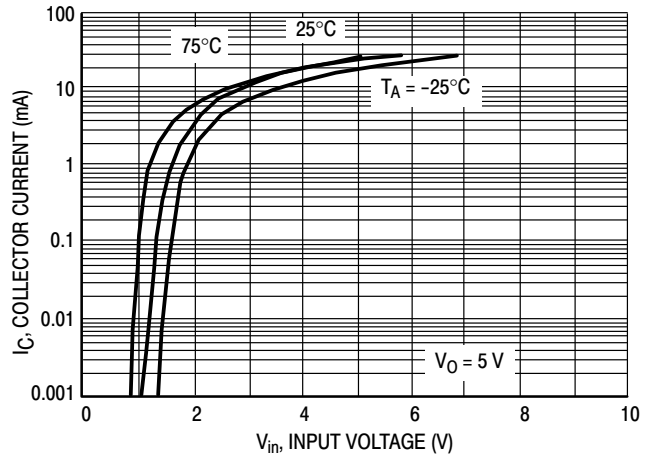


Figure 29. Output Current versus Input Voltage

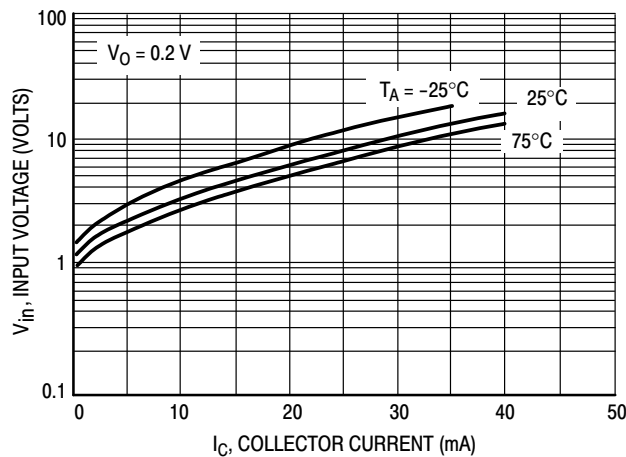


Figure 30. Input Voltage versus Output Current

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

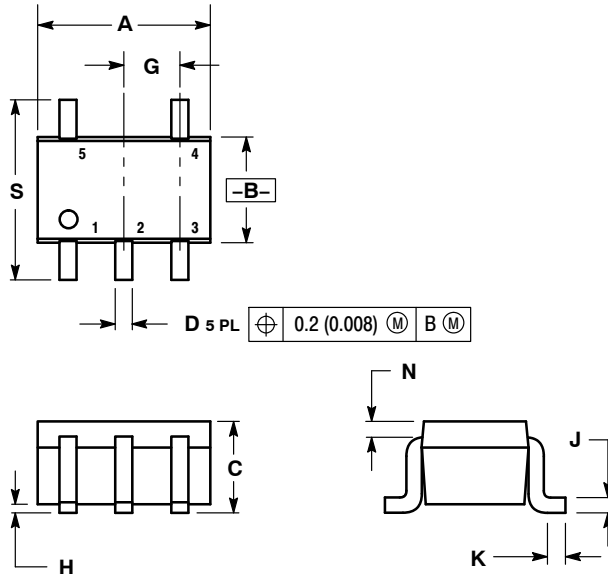
ON Semiconductor®



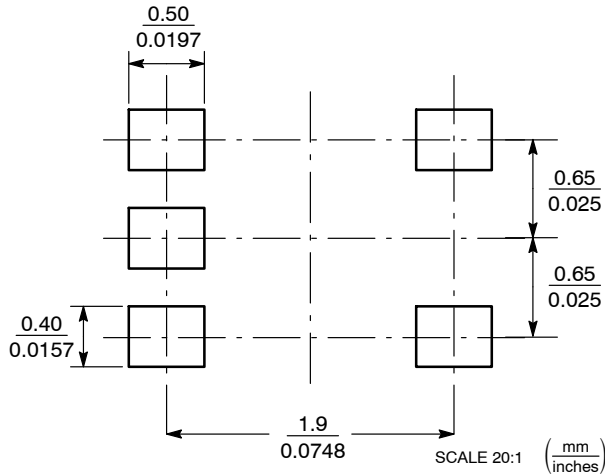
SCALE 2:1

SC-88A (SC-70-5/SOT-353)
CASE 419A-02
ISSUE L

DATE 17 JAN 2013



SOLDER FOOTPRINT

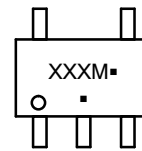


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

- | | | | | |
|----------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR</p> | <p>STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE</p> | <p>STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1</p> | <p>STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2</p> | <p>STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4</p> |
| <p>STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1</p> | <p>STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR</p> | <p>STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER</p> | <p>STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE</p> | <p>Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.</p> |

DOCUMENT NUMBER:	98ASB42984B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SC-88A (SC-70-5/SOT-353)	PAGE 1 OF 1

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