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FDD1600N10ALZ

N-Channel PowerTrench® MOSFET

100 V, 6.8 A, 160 mΩ

Features

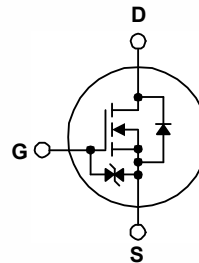
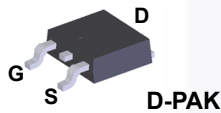
- $R_{DS(on)} = 124 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 3.4 \text{ A}$
- $R_{DS(on)} = 175 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 5 \text{ V}$, $I_D = 2.1 \text{ A}$
- Low Gate Charge (Typ. 2.78 nC)
- Low C_{rss} (Typ. 2.04 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance and maintain superior switching performance.

Application

- Consumer Appliances
- LED TV and Monitor
- Synchronous Rectification
- Uninterruptible Power Supply
- Micro Solar Inverter



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDD1600N10ALZ	Unit
V_{DSS}	Drain to Source Voltage	100	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	6.8
		- Continuous ($T_C = 100^\circ\text{C}$)	4.3
I_{DM}	Drain Current	- Pulsed (Note 1)	13.6
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	5.08
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.0
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	14.9
		- Derate Above 25°C	0.12
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDD1600N10ALZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	8.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	87	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD1600N10ALZ	1600N10ALZ	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.1	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μA
		$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_C = 125^\circ\text{C}$	-	-	500	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	± 10	μA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	1.4	-	2.8	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 3.4 \text{ A}$	-	124	160	$\text{m}\Omega$
		$V_{GS} = 5 \text{ V}, I_D = 2.1 \text{ A}$	-	175	375	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 6.8 \text{ A}$	-	19.6	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	-	169	225	pF	
C_{oss}	Output Capacitance		-	43	55	pF	
C_{rss}	Reverse Transfer Capacitance		-	2.04	-	pF	
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$	-	85	-	pF	
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{GS} = 10 \text{ V}$	$V_{DD} = 50 \text{ V},$ $I_D = 6.8 \text{ A}$	-	2.78	3.61	nC
$Q_{g(tot)}$	Total Gate Charge at 5V	$V_{GS} = 5 \text{ V}$		-	1.5	1.95	nC
Q_{gs}	Gate to Source Gate Charge			-	0.72	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	0.56	-	nC	
$V_{plateau}$	Gate Plateau Voltage	(Note 4)	-	4.02	-	V	
Q_{sync}	Total Gate Charge Sync.	$V_{DS} = 0 \text{ V}, I_D = 3.4 \text{ A}$	-	2.5	-	nC	
Q_{oss}	Output Charge	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$	-	5.2	-	nC	
ESR	Equivalent Series Resistance (G-S)	$f = 1 \text{ MHz}$	-	2.1	-	Ω	

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, I_D = 6.8 \text{ A},$ $V_{GS} = 10 \text{ V}, R_G = 4.7 \Omega$	-	7	24	ns
t_r	Turn-On Rise Time		-	2	14	ns
$t_{d(off)}$	Turn-Off Delay Time		-	13	36	ns
t_f	Turn-Off Fall Time		(Note 4)	-	2	14

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	6.8	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	13.6	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 6.8 \text{ A}$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{SD} = 6.8 \text{ A}, V_{DS} = 50 \text{ V},$ $di_F/dt = 100 \text{ A}/\mu\text{s}$	-	37	-	ns
Q_{rr}	Reverse Recovery Charge		-	42	-	nC

Notes:

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2. $L = 1 \text{ mH}, I_{AS} \approx 3.18 \text{ A}, R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 6.8 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

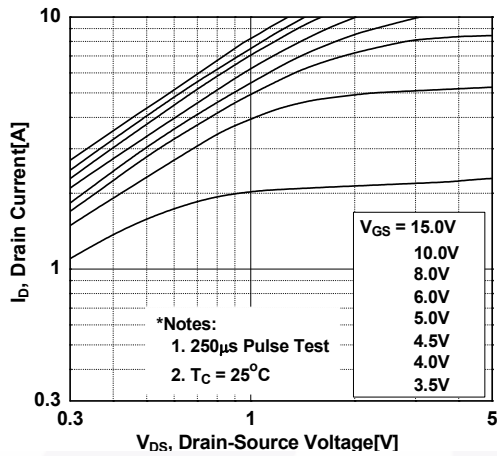


Figure 2. Transfer Characteristics

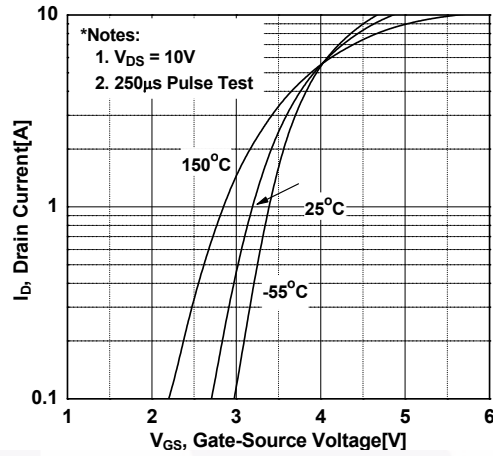


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

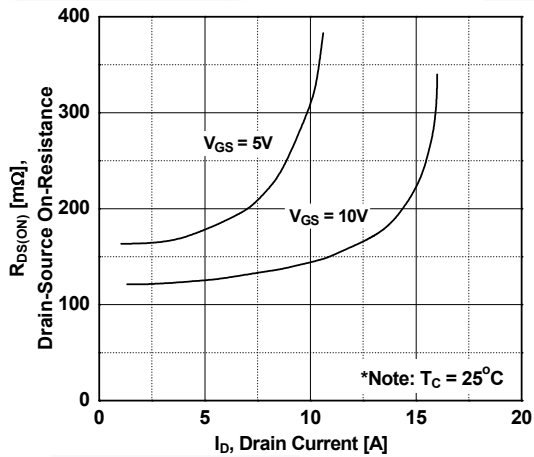


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

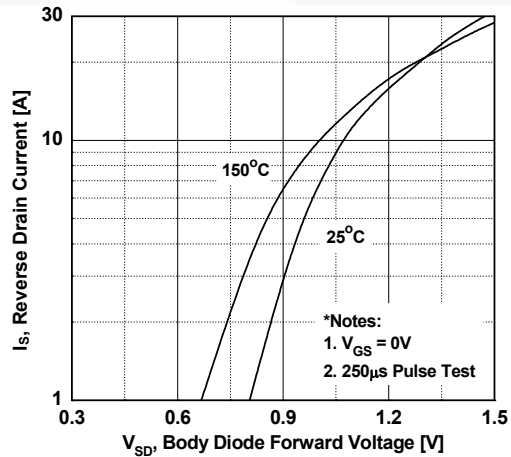


Figure 5. Capacitance Characteristics

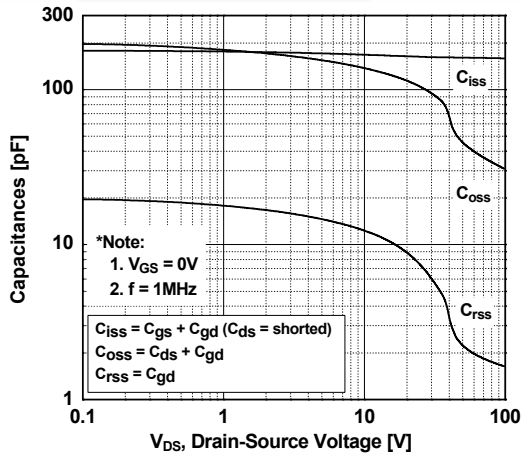
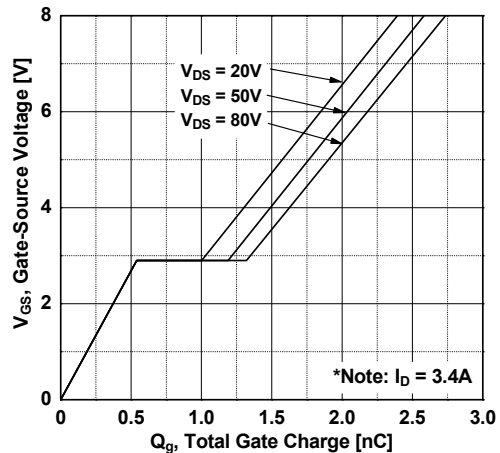


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

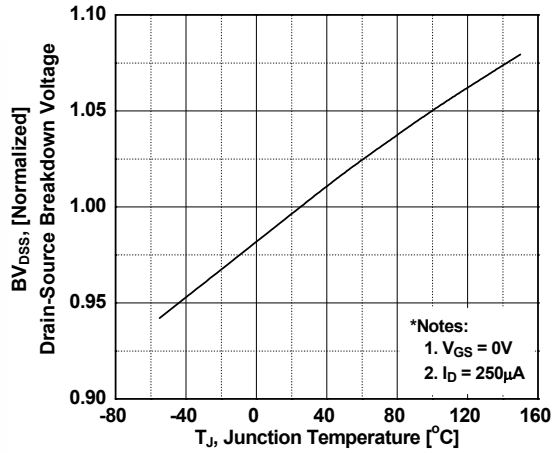


Figure 8. On-Resistance Variation vs. Temperature

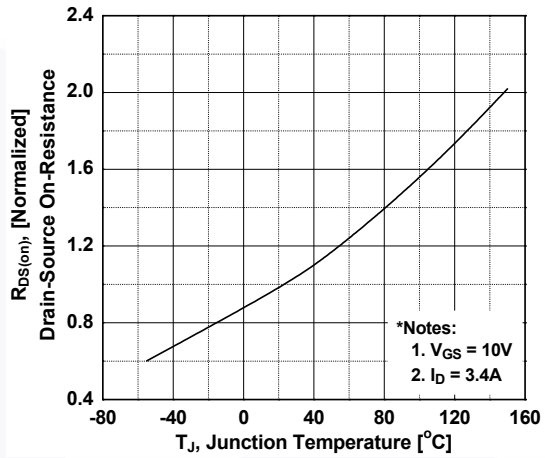


Figure 9. Maximum Safe Operating Area

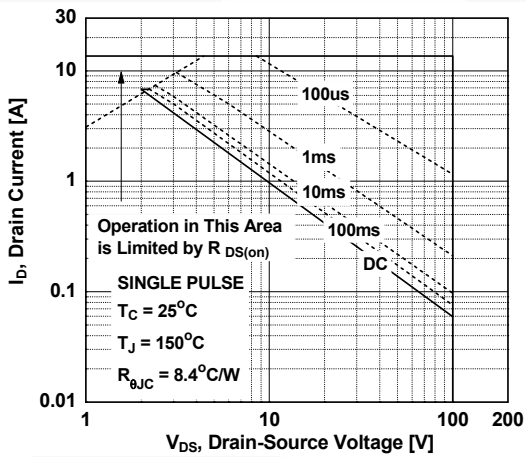


Figure 10. Maximum Drain Current vs. Case Temperature

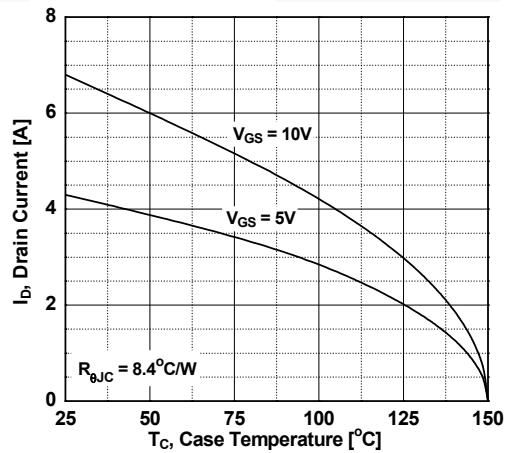


Figure 11. E_oss vs. Drain to Source Voltage

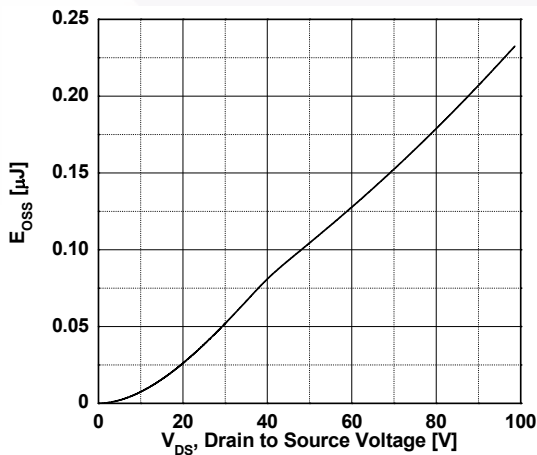
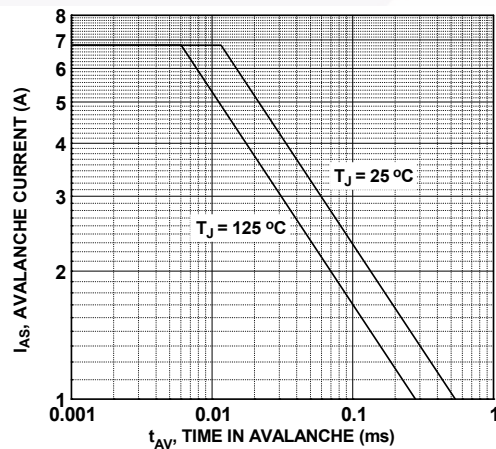


Figure 12. Unclamped Inductive Switching Capability



Typical Performance Characteristics (Continued)

Figure 13. Transient Thermal Response Curve

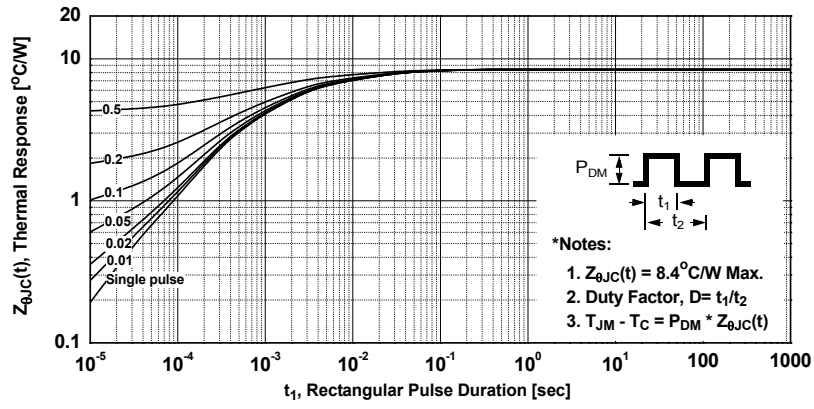




Figure 14. Gate Charge Test Circuit & Waveform



Figure 15. Resistive Switching Test Circuit & Waveforms



Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

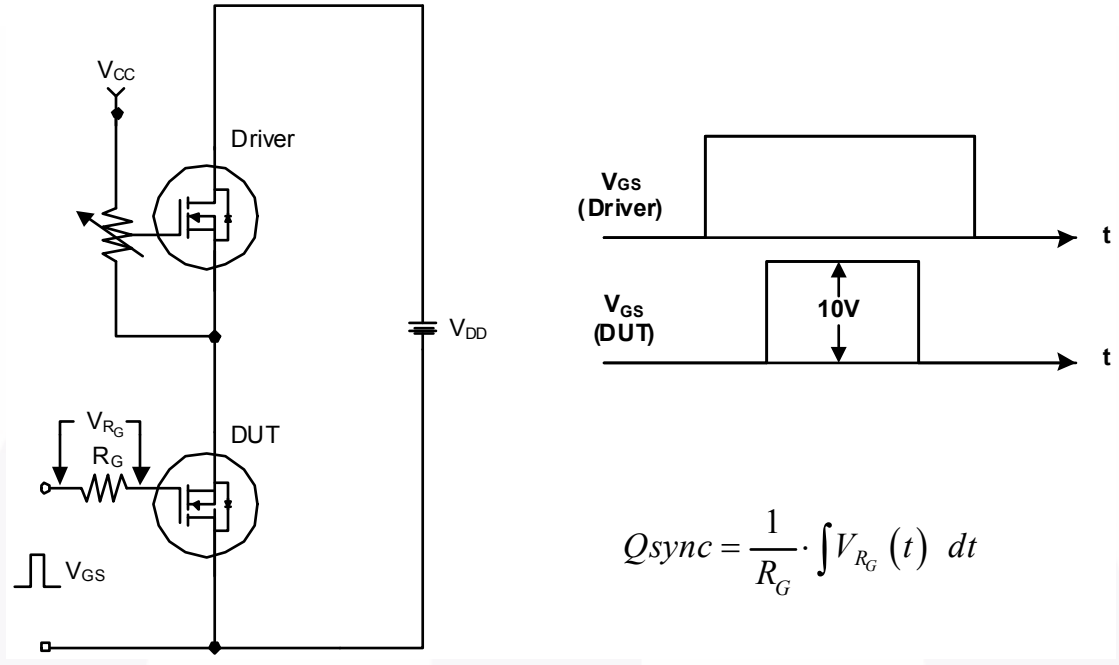


Figure 18. Total Gate Charge Q_{sync} . Test Circuit & Waveforms

Mechanical Dimensions

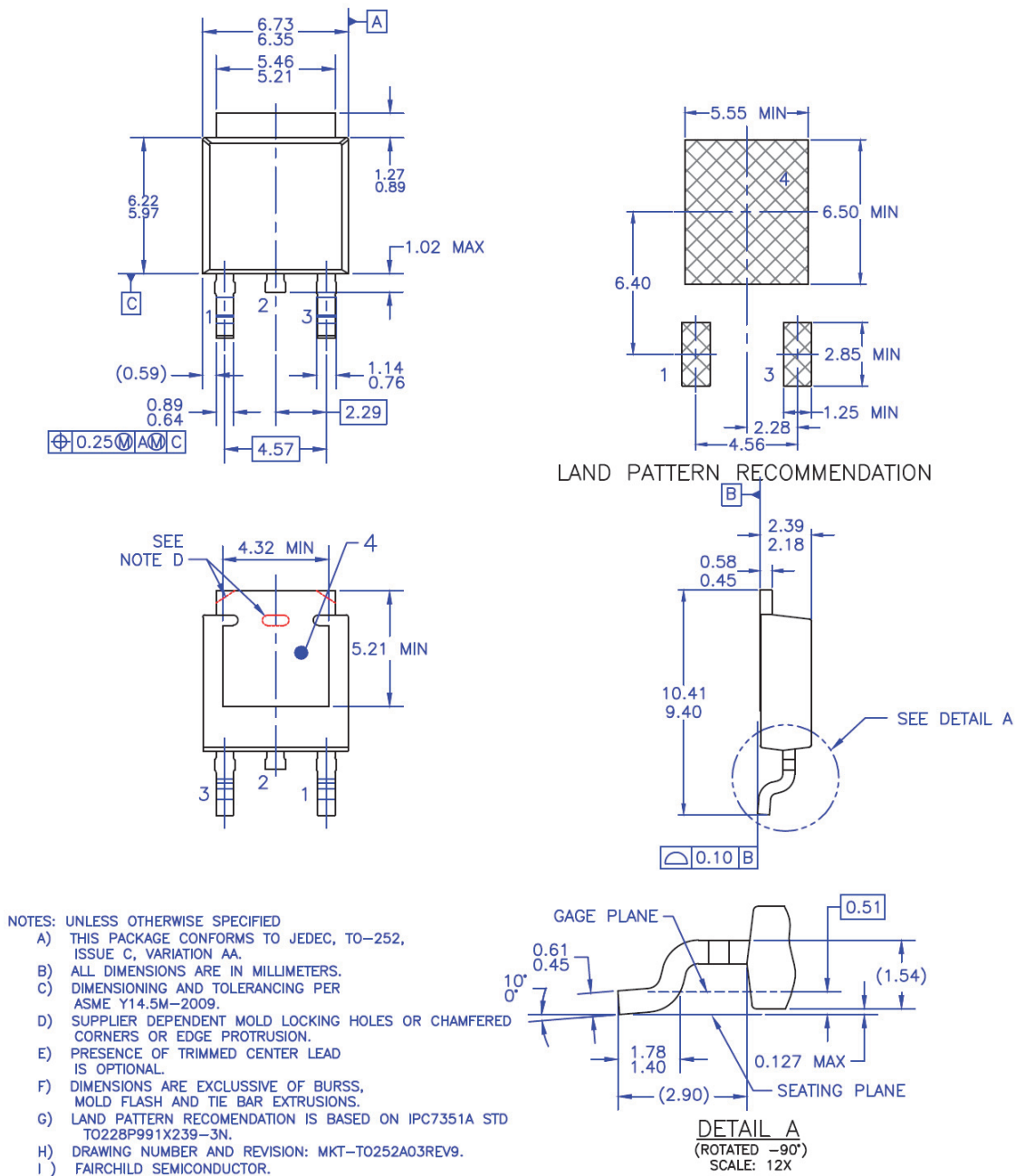


Figure 19. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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