

DT μ L 9111

PARALLEL GATED-CLOCKED FLIP-FLOP

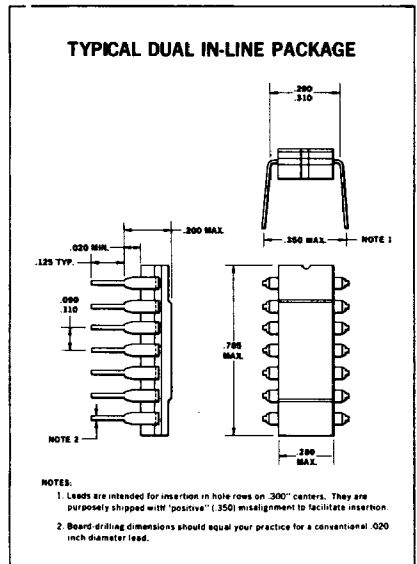
FAIRCHILD DIODE-TRANSISTOR MICROLOGIC[®] INTEGRATED CIRCUITS
INDUSTRIAL MICROCIRCUITS - 0°C TO +75°C TEMPERATURE RANGE

GENERAL DESCRIPTION - The DT μ L9111 is a Parallel Gated, Clocked Flip-Flop. It features directly coupled units operating on the "master-slave" principle. Operation is logically and electrically identical to the DT μ L9948 with the addition of another pair of two-input gates at the inputs of the flip-flop. This feature enhances the Logic design of some counters and shift-registers and can significantly reduce can count.

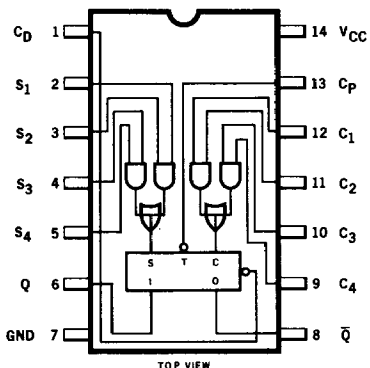
A direct clear input is provided which allows asynchronous entry irrespective of signals applied to any other inputs.

Output buffers provide isolation between the "slave" and the output load, thereby enhancing immunity to signal line noise.

The DT μ L9111 is completely compatible with all of the Fairchild 9930 Series Diode-Transistor Micrologic[®] integrated circuits.



LOGIC DIAGRAM



$$f_s = (S_1 \cdot S_2 + S_3 \cdot S_4) C_p$$

$$f_c = (C_1 \cdot C_2 + C_3 \cdot C_4) C_p + C_D$$

INPUT-OUTPUT LOADING FACTORS

$$(V_{CC} = 5.0 \text{ V})$$

Output Drive

$$\text{Pins 6 \& 8} = 11$$

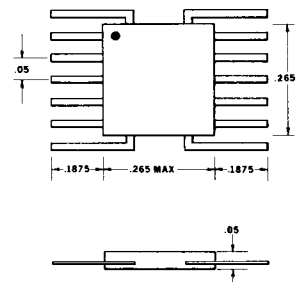
Input Loading

$$\text{Pins 2, 3, 4, 5, 9, 10, 11, 12} = 2/3$$

$$\text{Pin 1} = 2$$

$$\text{Pin 13} = 3$$

TYPICAL FLAT PACKAGE TOP VIEW



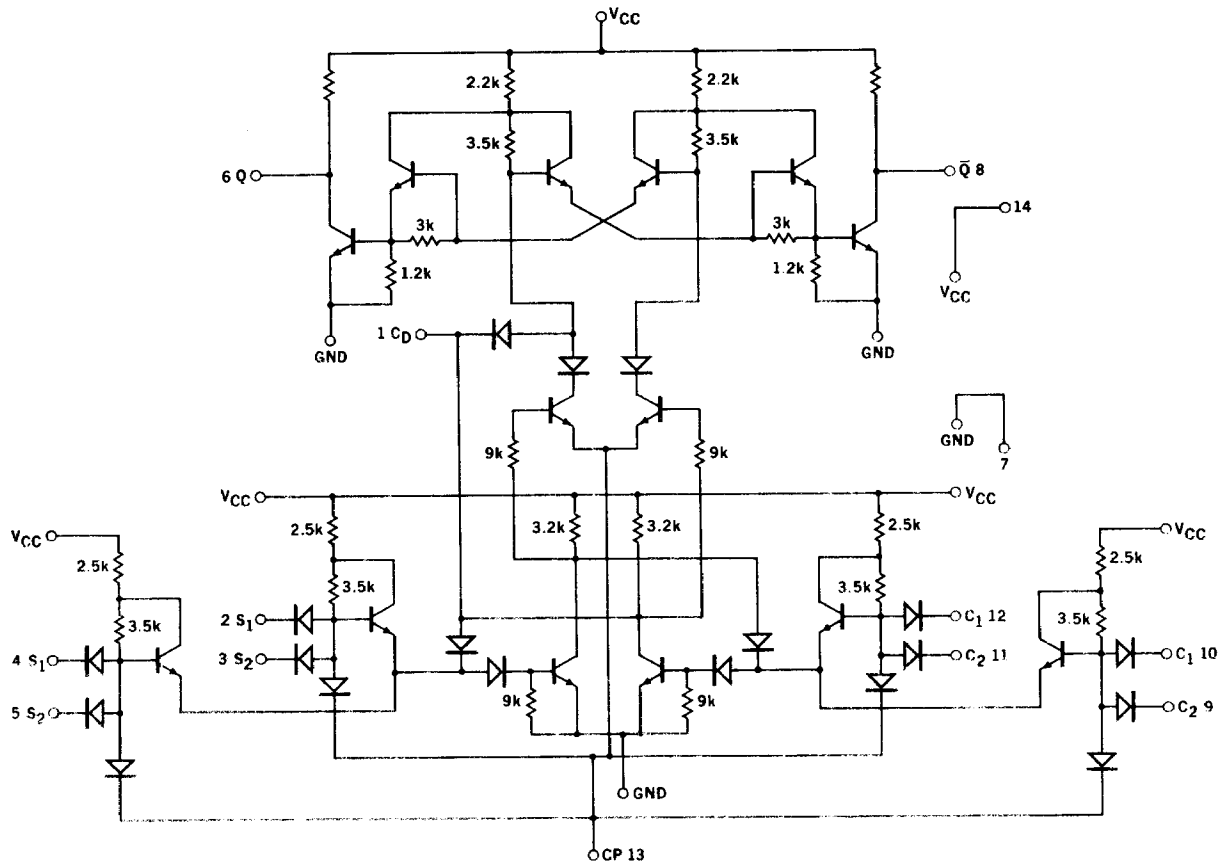
ORDER INFORMATION:

To order the DT μ L9111 element, specify the following Part Number:
U31911159X for Flat Pkg.
U6A911159X for Dual In-Line Pkg.

FAIRCHILD
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FAIRCHILD DIODE-TRANSISTOR MICROLOGIC® I.C.

SCHEMATIC DIAGRAM



TRUTH TABLE

		SYNCHRONOUS ENTRY									
		INPUTS								OUTPUTS	
		t_n								t_{n+1}	
Pin		2	3	4	5	9	10	11	12	6	8
	L	X	L	X	L	X	L	X	NC	NC	
	X	L	X	L	X	L	X	L	NC	NC	
	H	H	X	X	L	X	X	L	H	L	
	X	X	H	H	X	L	L	X	H	L	
	L	X	X	X	H	H	X	X	L	H	
	X	L	L	X	X	X	H	H	L	H	
	H	H	X	X	H	H	X	X	Undetermined		
	X	X	H	H	X	X	H	H	Undetermined		

		ASYNCHRONOUS ENTRY*			
		INPUT		OUTPUTS	
		Pin 1		6 8	
	H			NC	NC
	L			L	H

*Asynchronous entry is independent of all other inputs and overrides synchronous entry.

NOTES:

- (1) Pin numbers refer to flat package or dual in-line package.
- (2) Abbreviations used in the body of tables:
 - L = low, the more negative voltage level
 - H = high, the more positive voltage level (In all cases, unused pins have the same effect as high.)
 - X = immaterial, either H or L has equal effect
 - NC = no change, the trigger-pulse has no effect on outputs

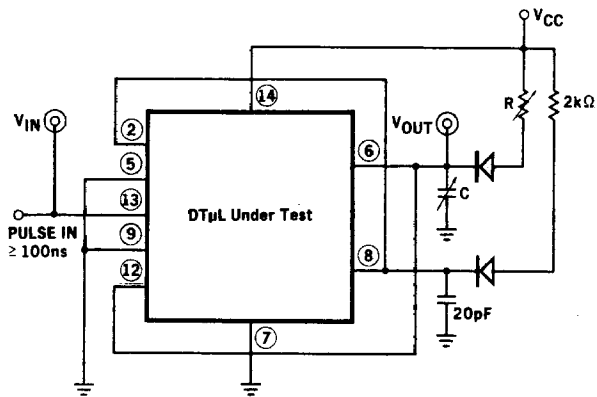
This is a partial table showing significant input-output conditions. Other conditions are similar combinations. Operation is best defined by the set and clear functions shown on Page 1.

For J-K Mode operation:

Connect 6 to 11 and 9; 8 to 3 and 5.

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tpd TEST CIRCUIT

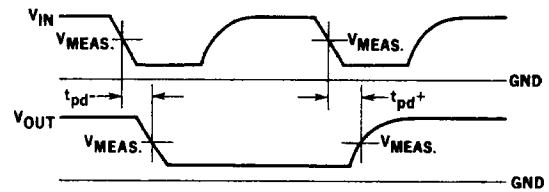


($V_{CC} = 5.0 \text{ V}$, $T = 25^\circ\text{C}$)

	R	C	Min.	Max.
t_{pd+}	2.0k	30 pF	30 ns	65 ns
t_{pd-}	330 Ω	50 pF	30 ns	75 ns

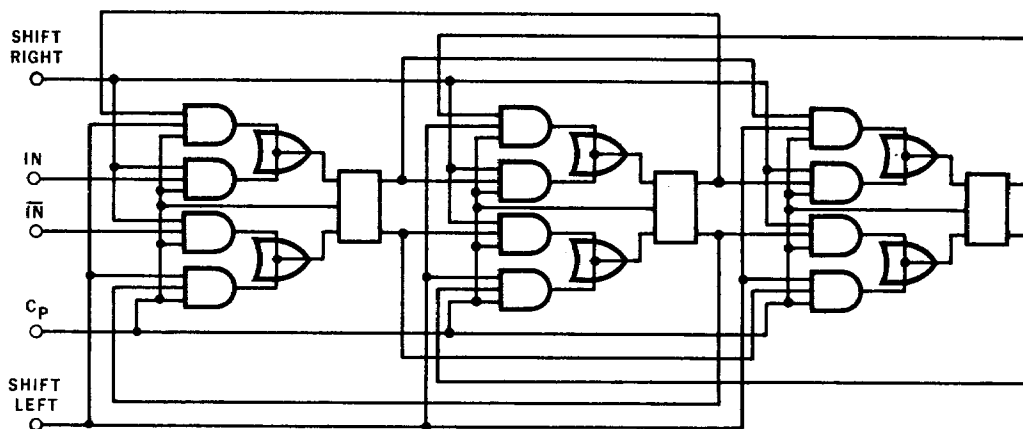
DIODES ARE FD600 OR EQUIVALENT.
ALL C's INCLUDE JIG & PROBE.

WAVE FORMS



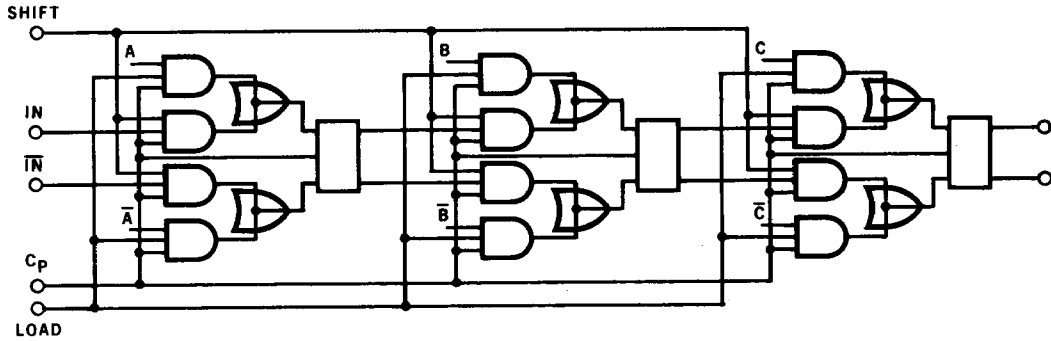
$V_{meas.} = 1.5 \text{ V at } +25^\circ\text{C}$

TYPICAL APPLICATIONS

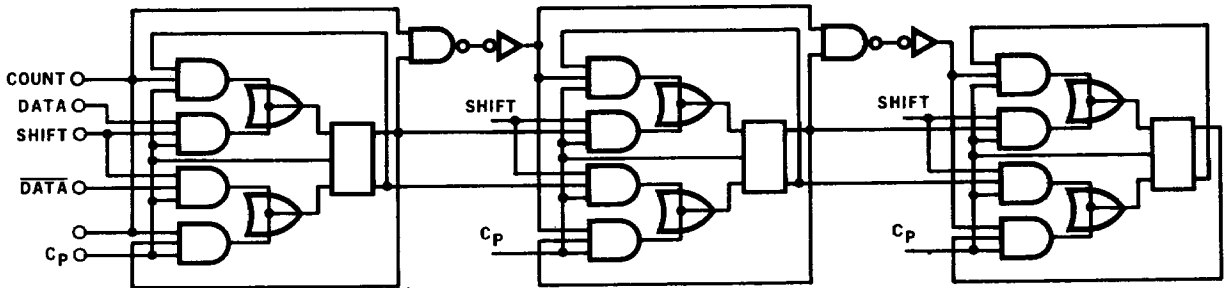


SHIFT RIGHT / SHIFT LEFT SHIFT REGISTER

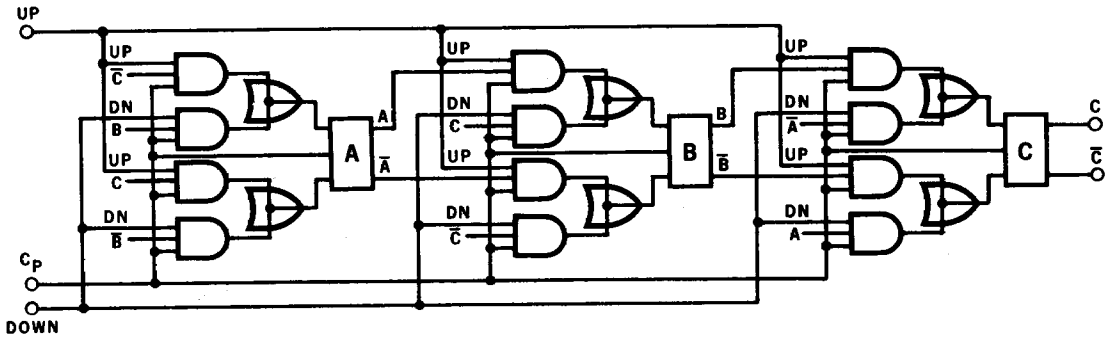
TYPICAL APPLICATIONS



SHIFT REGISTER WITH PARALLEL INPUT LOADING



SERIAL ENTRY - BINARY COUNTER



THREE STAGE MOIBUS COUNTER