NCV8501 Series

LDO Linear Regulators - Micropower, ENABLE, DELAY, $\overline{\text{RESET}}$, Monitor FLAG

150 mA

The NCV8501 is a family of precision micropower voltage regulators. Their output current capability is 150 mA. The family has output voltage options for adjustable, 2.5 V, 3.3 V, 5.0 V, 8.0 V, and 10 V.

The output voltage is accurate within ±2.0% with a maximum dropout voltage of 0.6 V at 150 mA. Low quiescent current is a feature drawing only 90 μA with a 100 μA load. This part is ideal for any and all battery operated microprocessor equipment.

Microprocessor control logic includes an active $\overline{\text{RESET}}$ (with DELAY), and a FLAG monitor which can be used to provide an early warning signal to the microprocessor of a potential impending $\overline{\text{RESET}}$ signal. The use of the FLAG monitor allows the microprocessor to finish any signal processing before the $\overline{\text{RESET}}$ shuts the microprocessor down.

The active $\overline{\text{RESET}}$ circuit operates correctly at an output voltage as low as 1.0 V. The $\overline{\text{RESET}}$ function is activated during the power up sequence or during normal operation if the output voltage drops outside the regulation limits.

The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments. The device has also been optimized for EMC conditions.

Features

- Output Voltage Options: Adjustable, 2.5 V, 3.3 V, 5.0 V, 8.0 V, 10 V
- ±2.0% Output
- Low 90 μA Quiescent Current
- Fixed or Adjustable Output Voltage
- Active $\overline{\text{RESET}}$
- ENABLE
- 150 mA Output Current Capability
- Fault Protection
  - +60 V Peak Transient Voltage
  - −15 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- Early Warning through $\overline{\text{FLAG}}$/MON Leads
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- These are Pb−Free Devices

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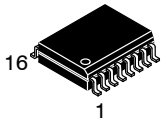
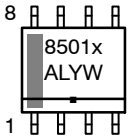
SO−8
D SUFFIX
CASE 751



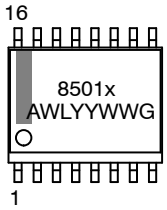
SOIC 16 LEAD
WIDE BODY
EXPOSED PAD
PDW SUFFIX
CASE 751AG

MARKING DIAGRAMS

SO−8



SOW−16
E PAD



x = Voltage Ratings as Indicated Below:
- A = Adjustable
- 2 = 2.5 V
- 3 = 3.3 V
- 5 = 5.0 V
- 8 = 8.0 V
- 0 = 10 V

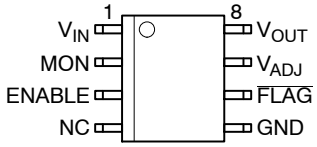
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

ORDERING INFORMATION

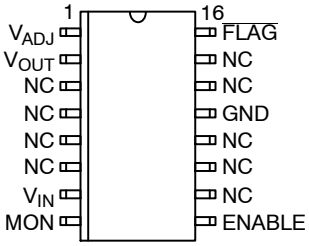
See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

PIN CONNECTIONS, ADJUSTABLE OUTPUT

SO−8

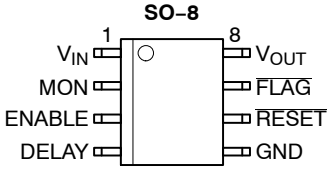


SOW−16 E PAD

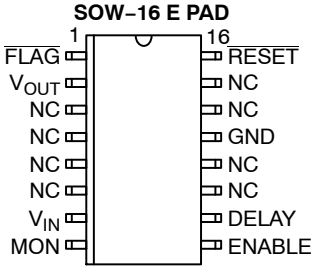


PIN CONNECTIONS, FIXED OUTPUT

SO−8



SOW−16 E PAD



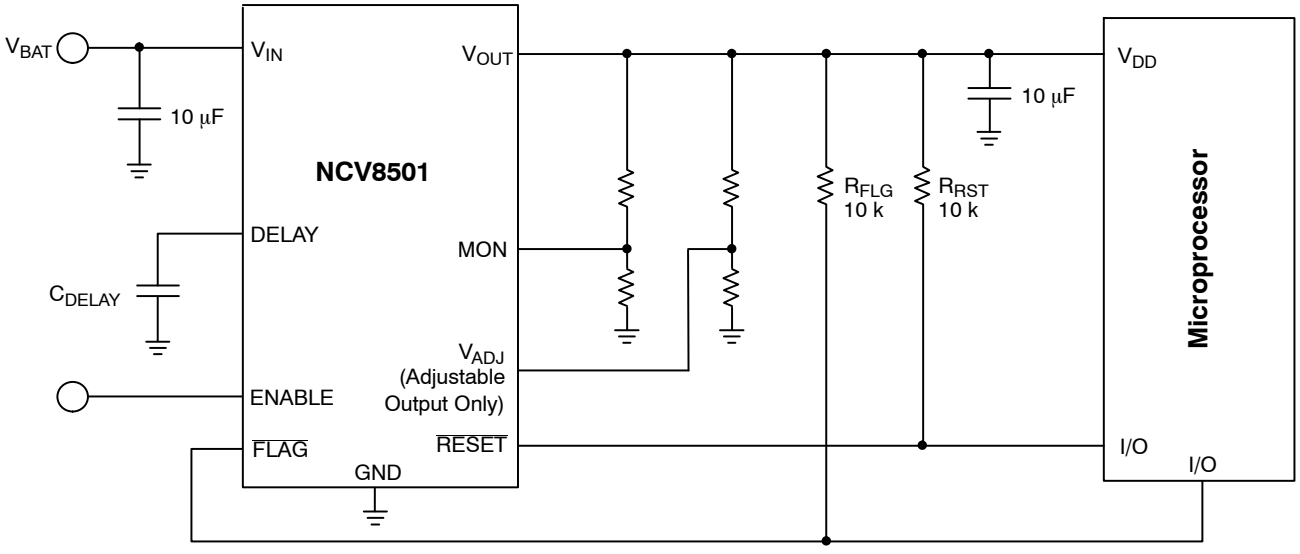


Figure 1. Application Diagram

MAXIMUM RATINGS*

Rating	Value	Unit
V_{IN} (dc)	−15 to 45	V
Peak Transient Voltage (46 V Load Dump @ V_{IN} = 14 V)	60	V
Operating Voltage	45	V
V_{OUT} (dc)	−0.3 to 16	V
Voltage Range ($\overline{RESET}$, $\overline{FLAG}$)	−0.3 to 10	V
Input Voltage Range (MON) (VAOJ)	−0.3 to 10 −0.3 to 16	V
Input Voltage Range (ENABLE)	−0.3 to 10**	V
ESD Susceptibility (Human Body Model)	2.0	kV
Junction Temperature, T_J	−40 to +150	°C
Storage Temperature, T_S	−55 to 150	°C
Package Thermal Resistance, SO−8: Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	45 165	°C/W °C/W
Package Thermal Resistance, SOW−16 E PAD: Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$ Junction−to−Pin, $R_{\theta JP}$ (Note 1)	15 56 35	°C/W °C/W °C/W
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 2)	260 Peak (Note 3)	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*During the voltage range which exceeds the maximum tested voltage of V_{IN}, operation is assured, but not specified. Wider limits may apply. Thermal dissipation must be observed closely.

**Reference Figure 15 for switched−battery ENABLE application.

1. Measured to pin 16.
2. 150 second maximum above 217°C.
3. −5°C / +0°C allowable conditions.

ELECTRICAL CHARACTERISTICS (I_{OUT} = 1.0 mA, ENABLE = 5.0 V, −40°C ≤ T_J ≤ 150°C; V_{IN} dependent on voltage option (Note 4); unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output Stage					
Output Voltage for 2.5 V Option	6.5 V < V_{IN} < 16 V, 100 μA ≤ I_{OUT} ≤ 150 mA **5.5 V < V_{IN} < 26 V**, 100 μA ≤ I_{OUT} ≤ 150 mA	2.450 2.425	2.5 2.5	2.550 2.575	V V
Output Voltage for 3.3 V Option	7.3 V < V_{IN} < 16 V, 100 μA ≤ I_{OUT} ≤ 150 mA **5.5 V < V_{IN} < 26 V**, 100 μA ≤ I_{OUT} ≤ 150 mA	3.234 3.201	3.3 3.3	3.366 3.399	V V
Output Voltage for 5.0 V Option	9.0 V < V_{IN} < 16 V, 100 μA ≤ I_{OUT} ≤ 150 mA **6.0 V < V_{IN} < 26 V**, 100 μA ≤ I_{OUT} ≤ 150 mA	4.90 4.85	5.0 5.0	5.10 5.15	V V
Output Voltage for 8.0 V Option	**9.0 V < V_{IN} < 26 V**, 100 μA ≤ I_{OUT} ≤ 150 mA	7.76	8.0	8.24	V
Output Voltage for 10 V Option	**11 V < V_{IN} < 26 V**, 100 μA ≤ I_{OUT} ≤ 150 mA	9.7	10	10.3	V
Output Voltage for Adjustable Option	V_{OUT} = V_{ADJ} (Unity Gain) 6.5 V < V_{IN} < 16 V, 100 μA < I_{OUT} < 150 mA 5.5 V < V_{IN} < 26 V, 100 μA < I_{OUT} < 150 mA	 1.254 1.242	 1.280 1.280	 1.306 1.318	 V V
Dropout Voltage (V_{IN} − V_{OUT}) (5.0 V, 8.0 V, 10 V, and Adj. > 5.0 V Options Only)	I_{OUT} = 150 mA I_{OUT} = 1.0 mA	– –	400 100	600 150	mV mV
Load Regulation	V_{IN} = 14 V, 5.0 mA ≤ I_{OUT} ≤ 150 mA	−30	5.0	30	mV
Line Regulation	[V_{OUT}(Typ) + 1.0] < V_{IN} < 26 V, I_{OUT} = 1.0 mA	–	15	60	mV
Quiescent Current, Low Load 2.5 V Option 3.3 V Option 5.0 V Option 8.0 V Option 10 V Option Adjustable Option	I_{OUT} = 100 μA, V_{IN} = 12 V, MON = V_{OUT}	 – – – – – –	 90 90 90 100 100 50	 125 125 125 150 150 75	 μA μA μA μA μA μA
Quiescent Current, Medium Load All Options	I_{OUT} = 75 mA, V_{IN} = 14 V, MON = V_{OUT}	–	4.0	6.0	mA
Quiescent Current, High Load All Options	I_{OUT} = 150 mA, V_{IN} = 14 V, MON = V_{OUT}	–	12	19	mA
Quiescent Current, (I_Q) Sleep Mode	ENABLE = 0 V, V_{IN} = 12 V	–	12	30	μA
Current Limit	–	151	300	–	mA
Short Circuit Output Current	V_{OUT} = 0 V	40	190	–	mA
Thermal Shutdown	(Guaranteed by Design)	150	180	–	°C
Reset Function (RESET)					
$\overline{\text{RESET}}$ Threshold for 2.5 V Option HIGH (V_{RH}) LOW (V_{RL})	5.5 V ≤ V_{IN} ≤ 26 V (Note 5) V_{OUT} Increasing V_{OUT} Decreasing	 2.28 2.25	 2.350 2.300	 0.98 × V_{OUT} 0.97 × V_{OUT}	 V V
$\overline{\text{RESET}}$ Threshold for 3.3 V Option HIGH (V_{RH}) LOW (V_{RL})	5.5 V ≤ V_{IN} ≤ 26 V (Note 5) V_{OUT} Increasing V_{OUT} Decreasing	 3.00 2.97	 3.102 3.036	 0.98 × V_{OUT} 0.97 × V_{OUT}	 V V
$\overline{\text{RESET}}$ Threshold for 5.0 V Option HIGH (V_{RH}) LOW (V_{RL})	 V_{OUT} Increasing V_{OUT} Decreasing	 4.55 4.50	 4.70 4.60	 0.98 × V_{OUT} 0.97 × V_{OUT}	 V V
$\overline{\text{RESET}}$ Threshold for 8.0 V Option HIGH (V_{RH}) LOW (V_{RL})	 V_{OUT} Increasing V_{OUT} Decreasing	 7.05 7.00	 7.52 7.36	 0.98 × V_{OUT} 0.97 × V_{OUT}	 V V

4. Voltage range specified in the Output Stage of the Electrical Characteristics in boldface type.
5. For V_{IN} ≤ 5.5 V, a $\overline{\text{RESET}}$ = Low may occur with the output in regulation.

ELECTRICAL CHARACTERISTICS (I_{OUT} = 1.0 mA, ENABLE = 5.0 V, −40°C ≤ T_J ≤ 150°C; V_{IN} dependent on voltage option (Note 4); unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Reset Function (RESET)					
$\overline{\text{RESET}}$ Threshold for 10 V Option HIGH (V_{RH}) LOW (V_{RL})	 V_{OUT} Increasing V_{OUT} Decreasing	 8.60 8.50	 9.40 9.20	 0.98 × V_{OUT} 0.97 × V_{OUT}	 V V
Output Voltage Low (V_{RLO})	1.0 V ≤ V_{OUT} ≤ V_{RL}, $R_{\overline{\text{RESET}}}$ = 10 k	–	0.1	0.4	V
DELAY Switching Threshold (V_{DT})	–	1.4	1.8	2.2	V
DELAY Low Voltage	V_{OUT} < $\overline{\text{RESET}}$ Threshold Low(min)	–	–	0.1	V
DELAY Charge Current	DELAY = 1.0 V, V_{OUT} > V_{RH}	1.5	2.5	3.5	μA
DELAY Discharge Current	DELAY = 1.0 V, V_{OUT} = 1.5 V	5.0	–	–	mA
$\overline{\text{FLAG}}$/Monitor					
Monitor Threshold	Increasing and Decreasing	1.10	1.20	1.31	V
Hysteresis	–	20	50	100	mV
Input Current	MON = 2.0 V	−0.5	0.1	0.5	μA
Output Saturation Voltage	MON = 0 V, I_{FLAG} = 1.0 mA	–	0.1	0.4	V
Voltage Adjust (Adjustable Output only)					
Input Current	V_{ADJ} = 1.28 V	−0.5	–	0.5	μA
ENABLE					
Input Threshold	Low High	– 3.0	– –	0.5 –	V V
Input Current	ENABLE = 5.0 V	–	1.0	5.0	μA

4. Voltage range specified in the Output Stage of the Electrical Characteristics in boldface type.
5. For V_{IN} ≤ 5.5 V, a $\overline{\text{RESET}}$ = Low may occur with the output in regulation.

PACKAGE PIN DESCRIPTION, ADJUSTABLE OUTPUT

Package Pin Number		Pin Symbol	Function
SO−8	SOW−16 E PAD		
1	7	V_{IN}	Input Voltage.
2	8	MON	Monitor. Input for early warning comparator. If not needed connect to V_{OUT}.
3	9	ENABLE	ENABLE control for the IC. A high powers the device up.
4	3−6, 10−12, 14, 15	NC	No connection.
5	13	GND	Ground. All GND leads must be connected to Ground.
6	16	$\overline{FLAG}$	Open collector output from early warning comparator.
7	1	V_{ADJ}	Voltage Adjust. A resistor divider from V_{OUT} to this lead sets the output voltage.
8	2	V_{OUT}	±2.0%, 150 mA output.

PACKAGE PIN DESCRIPTION, FIXED OUTPUT

Package Pin Number		Pin Symbol	Function
SO−8	SOW−16 E PAD		
1	7	V_{IN}	Input Voltage.
2	8	MON	Monitor. Input for early warning comparator. If not needed connect to V_{OUT}.
3	9	ENABLE	ENABLE control for the IC. A high powers the device up.
4	10	DELAY	Timing capacitor for $\overline{RESET}$ function.
5	13	GND	Ground. All GND leads must be connected to Ground.
6	16	$\overline{RESET}$	Active reset (accurate to $V_{OUT} \geq 1.0$ V)
7	1	$\overline{FLAG}$	Open collector output from early warning comparator.
8	2	V_{OUT}	±2.0%, 150 mA output.
−	3−6, 11, 12, 14, 15	NC	No connection.

TYPICAL PERFORMANCE CHARACTERISTICS

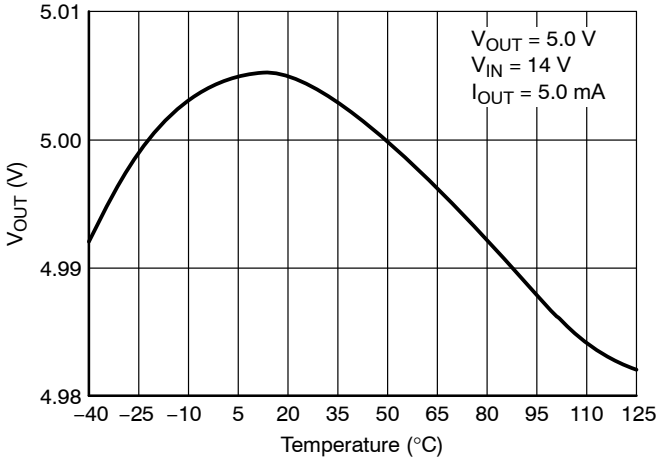


Figure 2. Output Voltage vs. Temperature

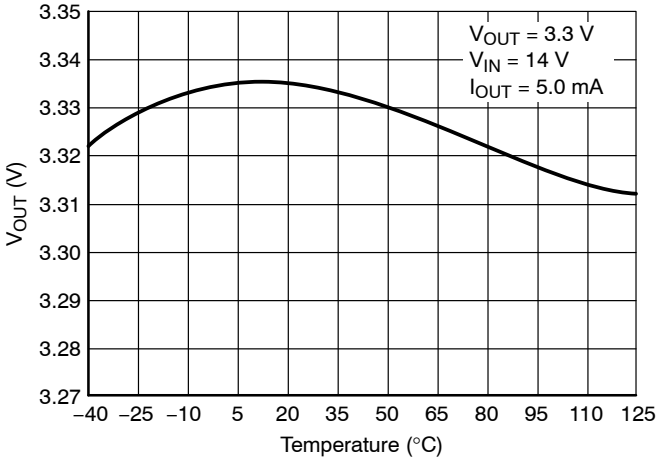


Figure 3. Output Voltage vs. Temperature

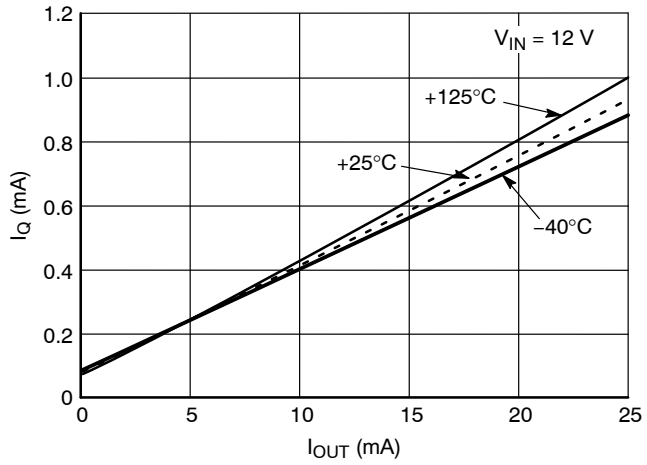


Figure 4. Quiescent Current vs. Output Current

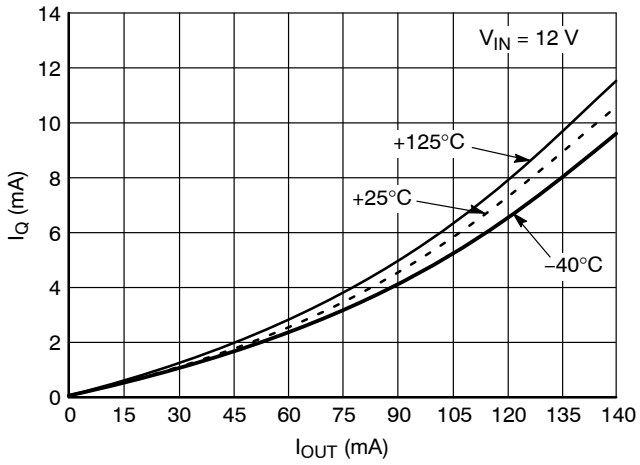


Figure 5. Quiescent Current vs. Output Current

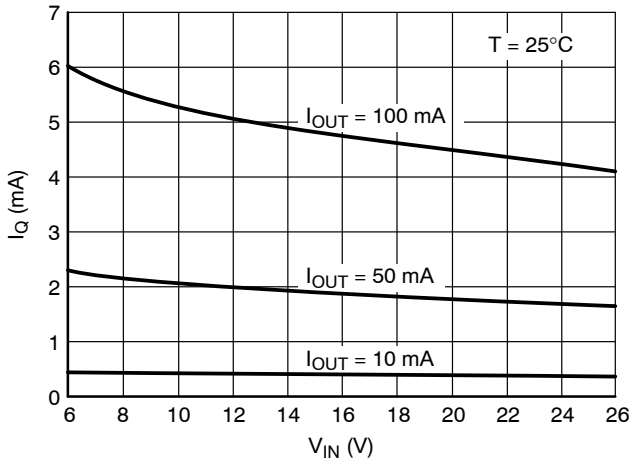


Figure 6. Quiescent Current vs. Input Voltage

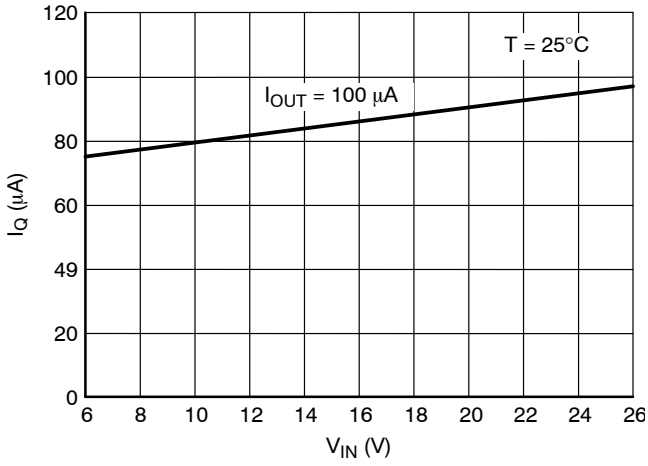


Figure 7. Quiescent Current vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

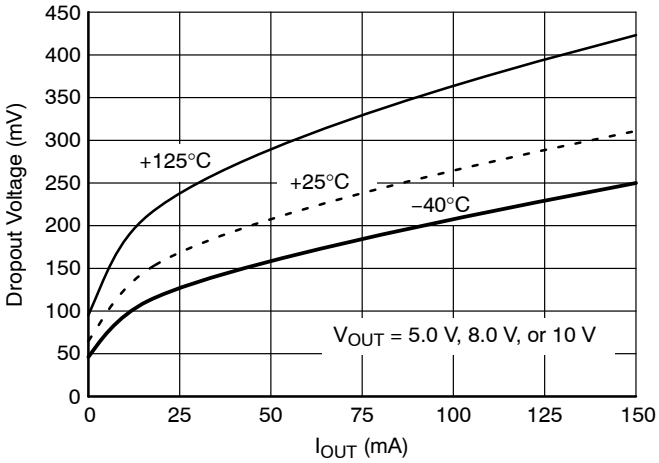


Figure 8. Dropout Voltage vs. Output Current

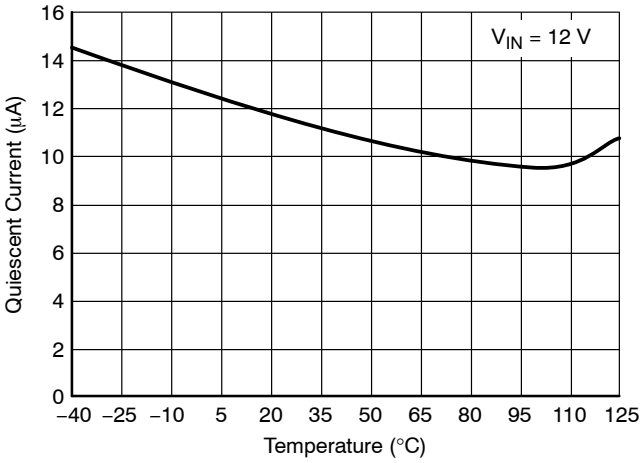


Figure 9. Sleep Mode I_Q vs. Temperature

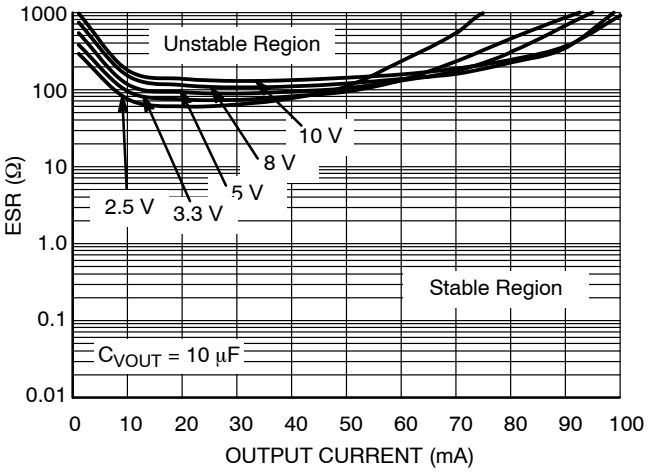


Figure 10. Output Stability with Output Voltage Change

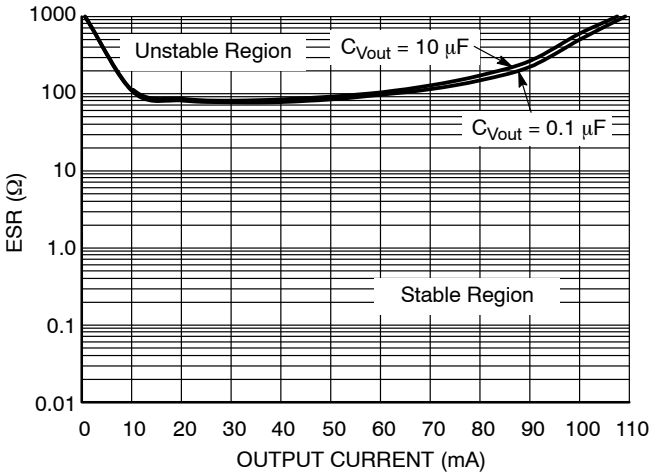


Figure 11. Output Stability with Output Capacitor Change

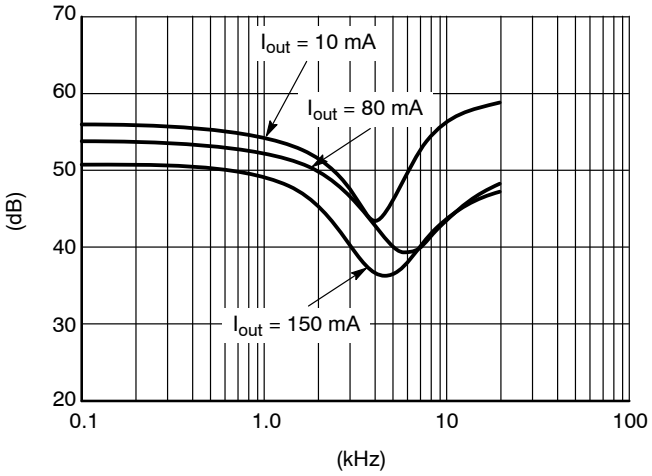


Figure 12. Audio Frequency Power Supply Rejection Ratio

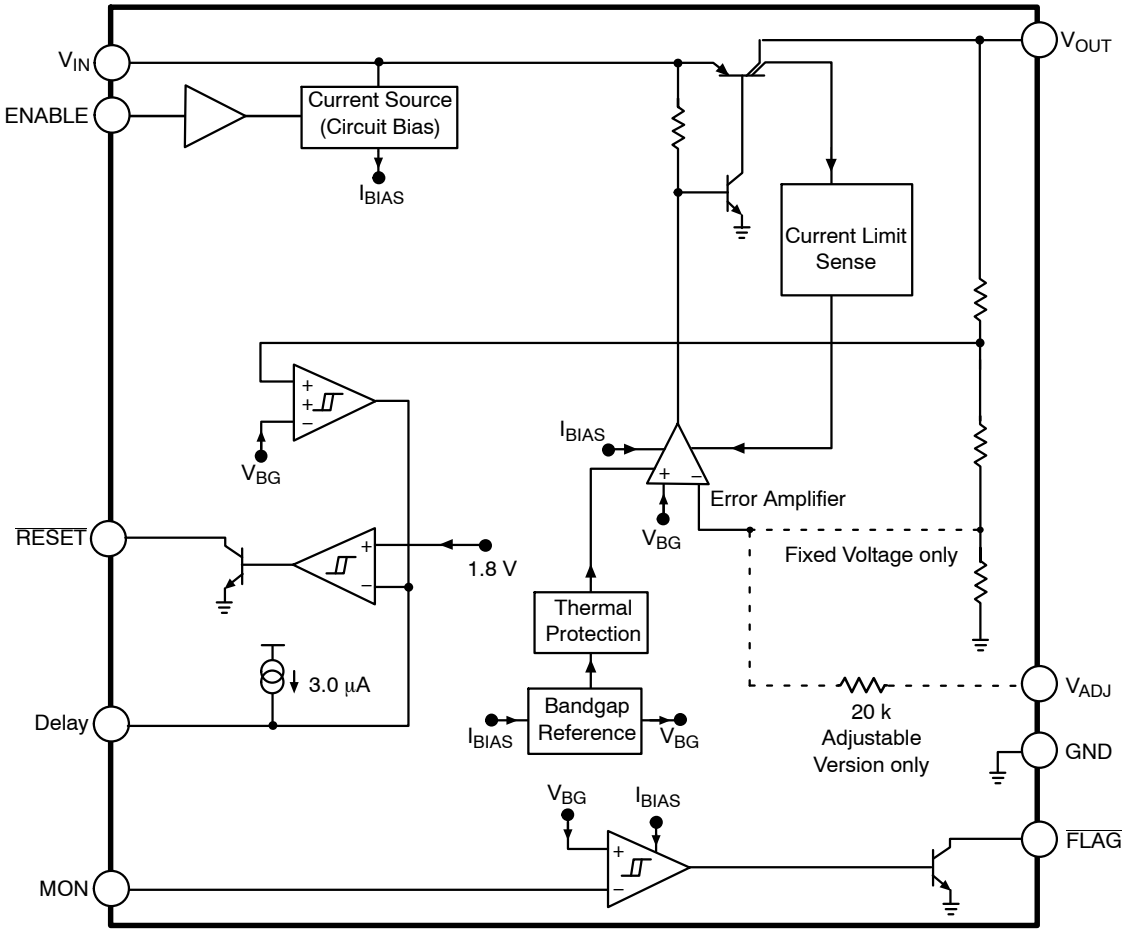


Figure 13. Block Diagram

CIRCUIT DESCRIPTION

REGULATOR CONTROL FUNCTIONS

The NCV8501 contains the microprocessor compatible control function $\overline{\text{RESET}}$ (Figure 14).

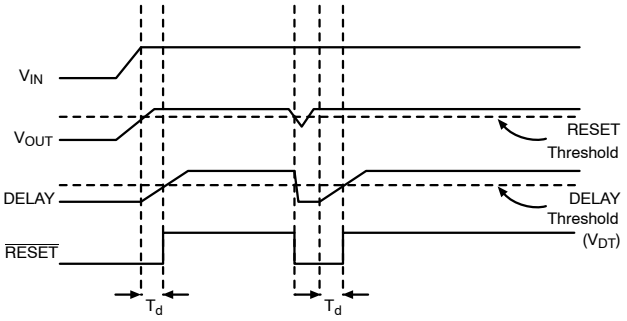


Figure 14. Reset and Delay Circuit Wave Forms

$\overline{\text{RESET}}$ Function

A $\overline{\text{RESET}}$ signal (low voltage) is generated as the IC powers up until V_{OUT} is within 6.0% of the regulated output voltage, or when V_{OUT} drops out of regulation,and is lower than 8.0% below the regulated output voltage. Hysteresis is included in the function to minimize oscillations.

The $\overline{\text{RESET}}$ output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC thereby guaranteeing that the $\overline{\text{RESET}}$ signal is valid for V_{OUT} as low as 1.0 V.

ENABLE Function

The part stays in a low I_Q sleep mode when the ENABLE pin is held low. The part has an internal pull down if the pin is left floating. This is intended for failure modes only. An external connection (active pulldown, resistor, or switch) for normal operation is recommended.

The integrity of the ENABLE pin allows it to be tied directly to the battery line through an external resistor. It will withstand load dump potentials in this configuration.

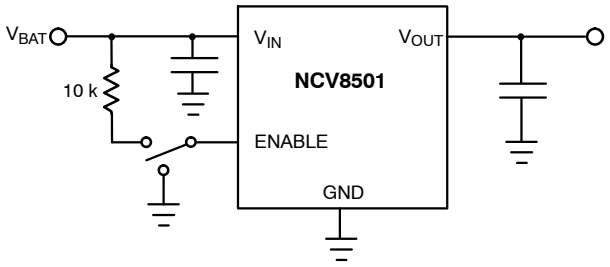


Figure 15. ENABLE Function

DELAY Function

The reset delay circuit provides a programmable (by external capacitor) delay on the $\overline{\text{RESET}}$ output lead.

The DELAY lead provides source current (typically 2.5 μA) to the external DELAY capacitor during the following proceedings:

1. During Power Up (once the regulation threshold has been verified).
2. After a reset event has occurred and the device is back in regulation. The DELAY capacitor is discharged when the regulation ($\overline{\text{RESET}}$ threshold) has been violated. This is a latched incident. The capacitor will fully discharge and wait for the device to regulate before going through the delay time event again.

$\overline{\text{FLAG}}$/Monitor Function

An on−chip comparator is provided to perform an early warning to the microprocessor of a possible reset signal. The reset signal typically turns the microprocessor off instantaneously. This can cause unpredictable results with the microprocessor. The signal received from the $\overline{\text{FLAG}}$ pin will allow the microprocessor time to complete its present task before shutting down. This function is performed by a comparator referenced to the bandgap reference. The actual trip point can be programmed externally using a resistor divider to the input monitor (MON) (Figure 16). The typical threshold is 1.20 V on the MON pin.

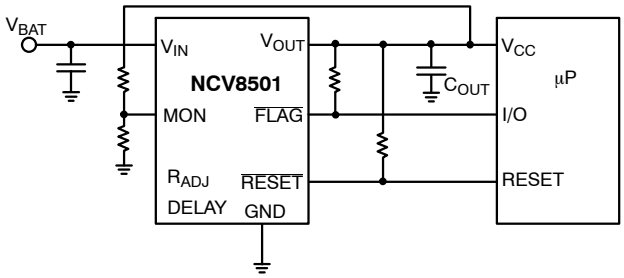


Figure 16. $\overline{\text{FLAG}}$/Monitor Function

Voltage Adjust

Figure 17 shows the device setup for a user configurable output voltage. The feedback to the V_{ADJ} pin is taken from a voltage divider referenced to the output voltage. The loop is balanced around the Unity Gain threshold (1.28 V typical).

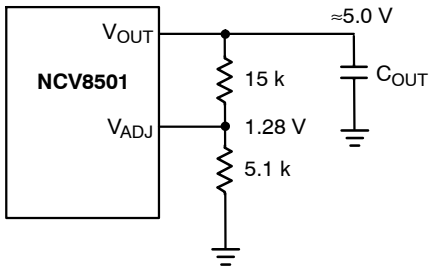


Figure 17. Adjustable Output Voltage

APPLICATION NOTES

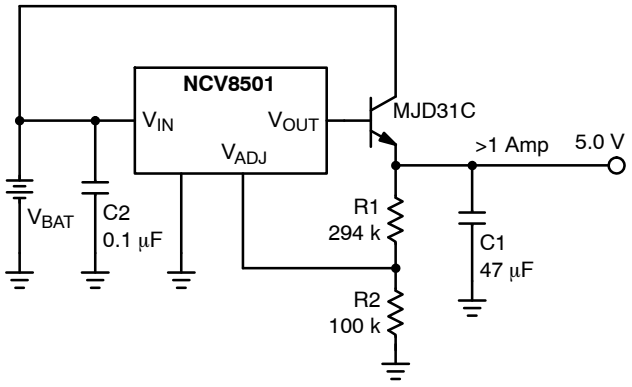


Figure 18. Additional Output Current

Adding Capability

Figure 18 shows how the adjustable version of parts can be used with an external pass transistor for additional current capability. The setup as shown will provide greater than 1 Amp of output current.

FLAG MONITOR

Figure 19 shows the FLAG Monitor waveforms as a result of the circuit depicted in Figure 16. As the output voltage falls (V_{OUT}), the Monitor threshold is crossed. This causes the voltage on the $\overline{\text{FLAG}}$ output to go low sending a warning signal to the microprocessor that a $\overline{\text{RESET}}$ signal may occur in a short period of time. $T_{WARNING}$ is the time the microprocessor has to complete the function it is currently working on and get ready for the $\overline{\text{RESET}}$ shutdown signal.

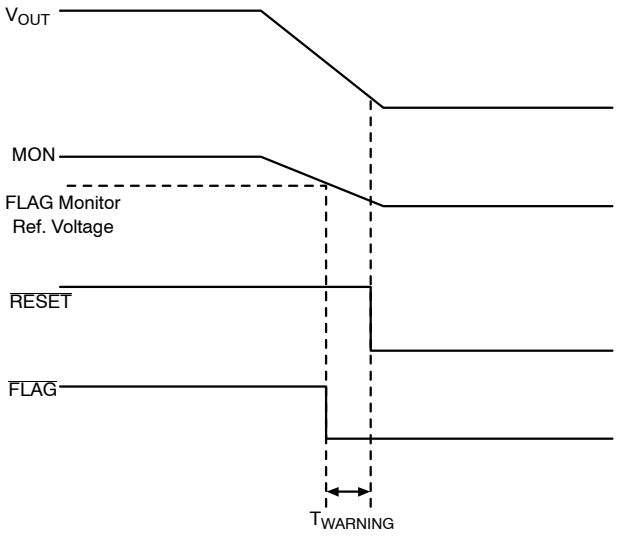
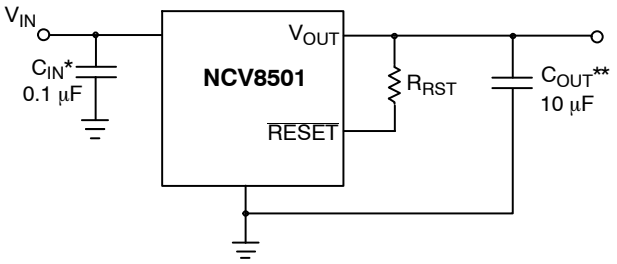


Figure 19. FLAG Monitor Circuit Waveform



*C_{IN} required if regulator is located far from the power supply filter
**C_{OUT} required for stability. Capacitor must operate at minimum temperature expected

Figure 20. Test and Application Circuit Showing Output Compensation

SETTING THE DELAY TIME

The delay time is controlled by the Reset Delay Low Voltage, Delay Switching Threshold, and the Delay Charge Current. The delay follows the equation:

$$t_{DELAY} = \frac{\left[C_{DELAY}(V_{dt} - \text{Reset Delay Low Voltage})\right]}{\text{Delay Charge Current}}$$

Example:

Using C_{DELAY} = 33 nF.

Assume reset Delay Low Voltage = 0.

Use the typical value for V_{dt} = 1.8 V.

Use the typical value for Delay Charge Current = 2.5 μA.

$$t_{DELAY} = \frac{\left[33\ \text{nF}(1.8 - 0)\right]}{2.5\ \mu\text{A}} = 23.8\ \text{ms}$$

STABILITY CONSIDERATIONS

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start−up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints.

The value for the output capacitor C_{OUT} shown in Figure 20 should work for most applications, however it is not necessarily the optimized solution.

UNDERSTANDING THE NCV8501 ENABLE PIN INPUT CURRENT

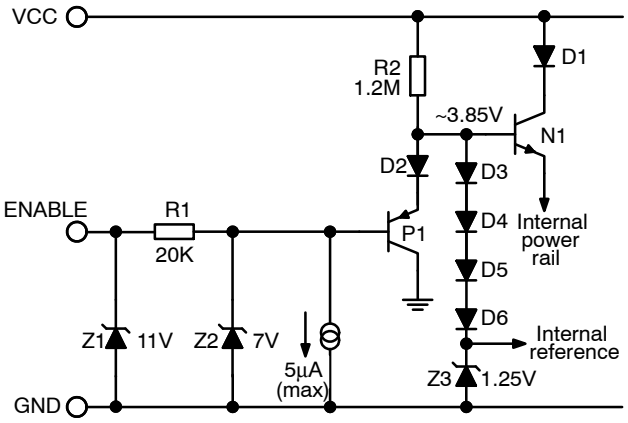


Figure 21. NCV8501 Enable Function Equivalent Circuit

Z1, R1, and Z2 provide ESD and overvoltage protection. Note that, for ENABLE pin voltages in excess of 10 V, an external series resistor is required to limit the current into Z1.

For ENABLE pin voltages less than +7 V, the 5 μA (maximum value) current source dominates the input current, as the opposing P1 base current is negligible by comparison.

For ENABLE pin voltages between +7 V and +11 V, the input current is given by:

$$5\ \mu A + ((V_{ENABLE} - 7) / 20\ k\Omega)$$

For ENABLE pin voltages in excess of 10 V (Z1 breakover voltage can be as low as 10 V), the input current is dominated by the external series resistor. For the case where V_{ENABLE} = 12 V; R_{EXT} = 10 kΩ, the input current can be up to (2 V/10 kΩ), = 200 μA.

The ENABLE threshold is that voltage required to achieve ~3.85 V at the base of N1, or approximately (3.85 V − 2 Vbe). At +20°C, this threshold is ~2.55 V. At −40°C, it can be as high as 3 V.

If the value of R_{EXT} is increased to ~200 kΩ, to reduce ENABLE input current, then the worst−case drop across R_{EXT} must be added to 3 V to determine the effective maximum ENABLE threshold. At V_{ENABLE} < 7 V, we only need to consider the 5 μA current sink.

Max effective threshold = 3 V + (5 μA * 220 kΩ)
= 3 V + 1.1 V
= 4.1 V

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 22) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}]I_{OUT(max)} + V_{IN(max)}I_Q \quad \text{(eq. 1)}$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150^\circ C - T_A}{P_D} \quad \text{(eq. 2)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

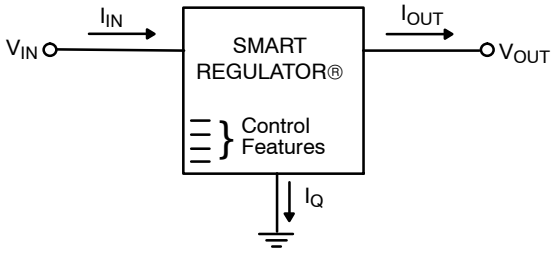


Figure 22. Single Output Regulator with Key Performance Parameters Labeled

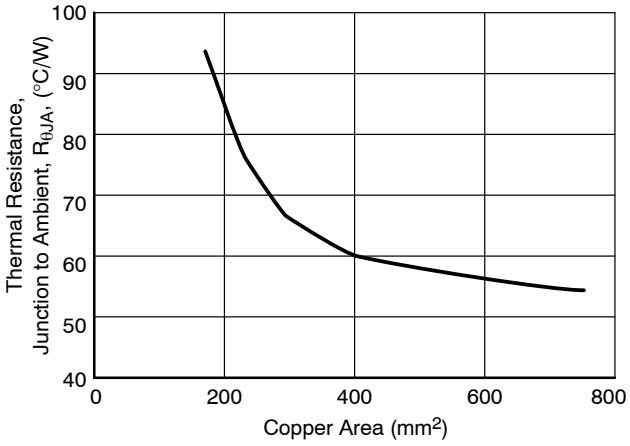


Figure 23. 16 Lead SOW (Exposed Pad), θJA as a Function of the Pad Copper Area (2 oz. Cu Thickness), Board Material = 0.0625″ G−10/R−4

HEATSINKS

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 3)}$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and

$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers.

ORDERING INFORMATION

Device	Output Voltage	Package	Shipping†
NCV8501DADJG	Adjustable	SO−8 (Pb−Free)	98 Units/Rail
NCV8501DADJR2G	Adjustable	SO−8 (Pb−Free)	2500 Tape & Reel
NCV8501PDWADJG	Adjustable	SOW−16 Exposed Pad (Pb−Free)	47 Units/Rail
NCV8501PDWADJR2G	Adjustable	SOW−16 Exposed Pad (Pb−Free)	1000 Tape & Reel
NCV8501D25G	2.5 V	SO−8 (Pb−Free)	98 Units/Rail
NCV8501D25R2G	2.5 V	SO−8 (Pb−Free)	2500 Tape & Reel
NCV8501PDW25G	2.5 V	SOW−16 Exposed Pad (Pb−Free)	47 Units/Rail
NCV8501PDW25R2G	2.5 V	SOW−16 Exposed Pad (Pb−Free)	1000 Tape & Reel
NCV8501D33G	3.3 V	SO−8 (Pb−Free)	98 Units/Rail
NCV8501D33R2G	3.3 V	SO−8 (Pb−Free)	2500 Tape & Reel
NCV8501PDW33G	3.3 V	SOW−16 Exposed Pad (Pb−Free)	47 Units/Rail
NCV8501PDW33R2G	3.3 V	SOW−16 Exposed Pad (Pb−Free)	1000 Tape & Reel
NCV8501D50G	5.0 V	SO−8 (Pb−Free)	98 Units/Rail
NCV8501D50R2G	5.0 V	SO−8 (Pb−Free)	2500 Tape & Reel
NCV8501PDW50G	5.0 V	SOW−16 Exposed Pad (Pb−Free)	47 Units/Rail
NCV8501PDW50R2G	5.0 V	SOW−16 Exposed Pad (Pb−Free)	1000 Tape & Reel
NCV8501D80G	8.0 V	SO−8 (Pb−Free)	98 Units/Rail
NCV8501D80R2G	8.0 V	SO−8 (Pb−Free)	2500 Tape & Reel
NCV8501PDW80G	8.0 V	SOW−16 Exposed Pad (Pb−Free)	47 Units/Rail
NCV8501PDW80R2G	8.0 V	SOW−16 Exposed Pad (Pb−Free)	1000 Tape & Reel
NCV8501D100G	10 V	SO−8 (Pb−free)	98 Units/Rail
NCV8501D100R2G	10 V	SO−8 (Pb−Free)	2500 Tape & Reel
NCV8501PDW100G	10 V	SOW−16 Exposed Pad (Pb−Free)	47 Units/Rail
NCV8501PDW100R2G	10 V	SOW−16 Exposed Pad (Pb−Free)	1000 Tape & Reel

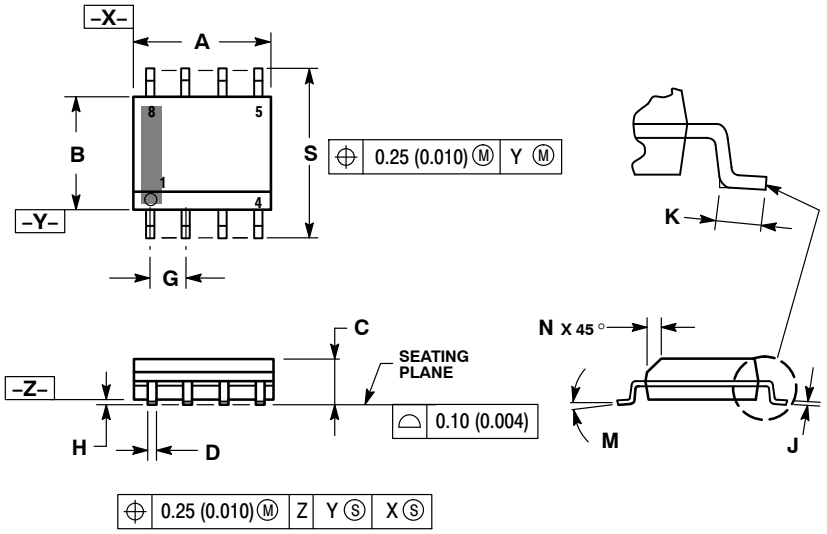
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

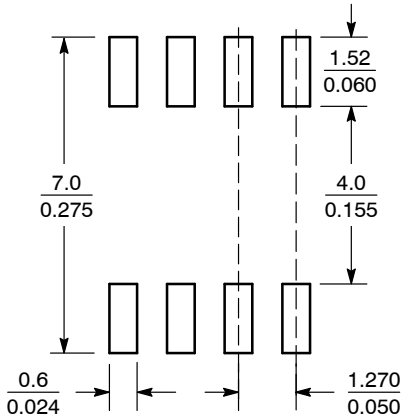
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

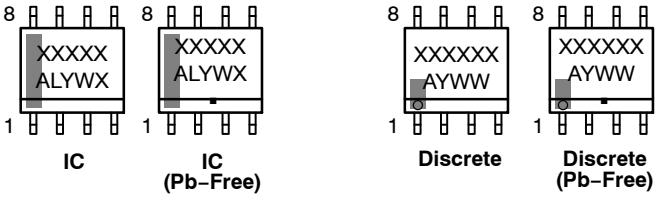
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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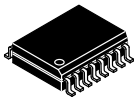
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

SOIC 16 LEAD WIDE BODY, EXPOSED PAD

CASE 751AG
ISSUE B

DATE 31 MAY 2016



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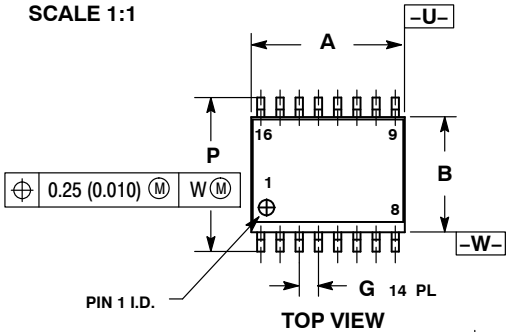
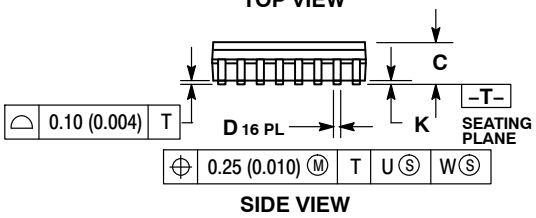
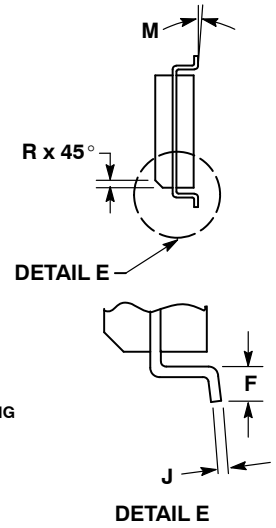


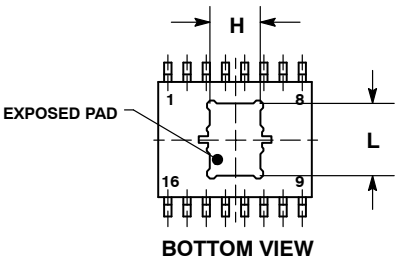
TOP VIEW



SIDE VIEW

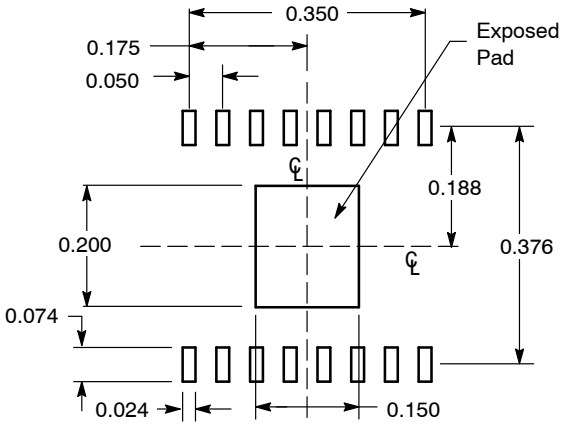


DETAIL E



BOTTOM VIEW

SOLDERING FOOTPRINT*



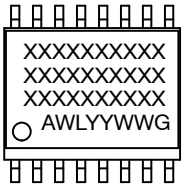
DIMENSIONS: INCHES

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751R–01 OBSOLETE, NEW STANDARD 751R–02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
H	3.45	3.66	0.136	0.144
J	0.25	0.32	0.010	0.012
K	0.00	0.10	0.000	0.004
L	4.72	4.93	0.186	0.194
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	**98AON21237D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOIC–16, WB EXPOSED PAD**	**PAGE 1 OF 1**

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Europe, Middle East and Africa Technical Support:
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