

Buck-Boost Regulator

DESCRIPTION

The SiP1759 is a buck-boost regulating charge pump. It is designed to provide a regulated output from 1 cell Li Ion or 2/3 cell NiMH voltages found in handheld portable equipment, 1.6 V to 5.5 V. SiP1759 allows the option of a fixed 3.3 V output voltage, or an adjustable output which can be set from 2.5 V to 5.5 V. The output current is up to 100 mA.

For flexibility in application, SiP1759 has a shutdown pin (SD) and an ERROR output to indicate when the output voltage is in regulation.

SiP1759 is available in a 10 pin MSOP package and is rated over the industrial temperature range of - 40 °C to 85 °C.

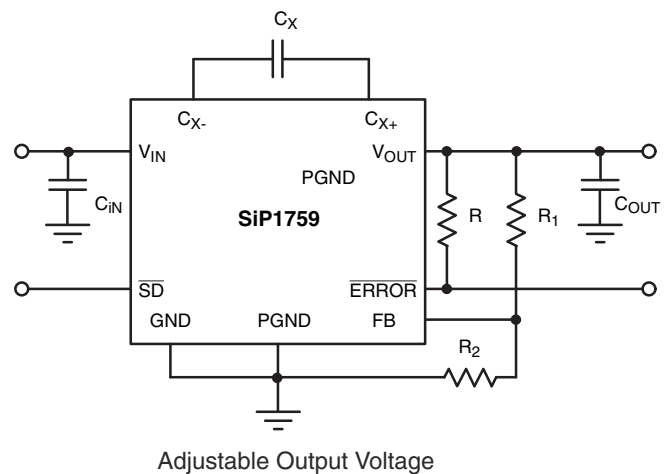
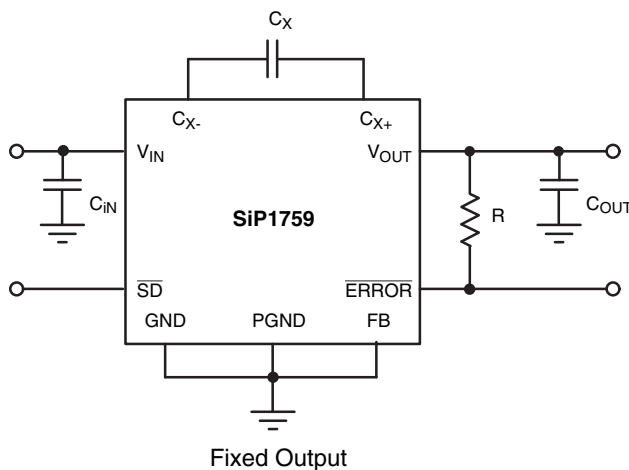
FEATURES

- Output voltage - fixed 3.3 V or adjustable from 2.5 V to 5.5 V
- 1.6 V to 5.5 V input voltage range
- 100 mA output current
- 60 μ A quiescent current
- Shutdown current < 1 μ A
- Short circuit protection
- Thermal shutdown
- MSOP-10 package

APPLICATIONS

- 1 cell Li ion battery powered equipment
- 2 to 3 cell NiMH battery powered equipment
- 2 to 3 cell alkaline battery powered equipment
- Backup battery boost converters

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS (all voltages referenced to GND = 0 V)

| Parameter | Limit | Unit |
|--|---|------|
| Input Voltage (V_{IN}) | - 0.3 to 6 | V |
| OUT \overline{SD} , FB, ERROR to GND | - 0.3 to 6 | |
| C_X to GND | - 0.3 to ($V_{IN} + 0.3$) | |
| C_{X+} to GND | - 0.3 to (the greater of V_{IN} or V_{OUT}) + 1) | |
| Storage Temperature | - 55 to 150 | °C |
| Maximum Junction Temperature | 150 | |
| Power Dissipation ^{a,b} | MSOP-10 ($T_A = 70$ °C) | mW |

Notes:

- a. Device Mounted with all leads soldered or welded to PC board.
 b. Derate 5.6 mW/°C above 25 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE (all voltages referenced to GND = 0 V)

| Parameter | Limit | Unit |
|---------------------------------|------------|------|
| Input Voltage Range | 1.6 to 5.5 | V |
| Output Voltage Adjustment Range | 2.5 to 5.5 | |
| C_{IN} | 10 | μF |
| C_X | 0.33 | |
| C_{OUT} | 10 | |
| Operating Temperature Range | - 40 to 85 | °C |

SPECIFICATIONS

| Parameter | Symbol | Test Condition Unless Specified $V_{IN} = V_{SD} = 2$ V, FB = PGND = GND $C_{IN} = 10$ μF, $C_X = 0.33$ μF, $C_{OUT} = 10$ μF | Temp. ^a | Limits - 40 °C to 85 °C | | | Unit |
|---------------------------------------|-----------------|---|--------------------|----------------------------|-------------------|-----------------|------|
| | | | | Min. | Typ. ^b | Max. | |
| Input Voltage Range | V_{IN} | | Full | 1.6 | | 5.5 | V |
| Input Undervoltage Lockout | V_{UVLO} | | Full | 0.7 | 1.0 | 1.5 | |
| Output Voltage Adjustment Range | | 1.6 V $\leq V_{IN} \leq 5.5$ V | Full | 2.5 | | 5.5 | |
| Output Voltage | V_{OUT} | 2 V $\leq V_{IN} \leq 5.5$ V, 1 mA $\leq I_{OUT} \leq 50$ mA | 0 °C to 85 °C | 3.17 | 3.3 | 3.43 | |
| | | 2.5 V $\leq V_{IN} \leq 5.5$ V, 1 mA $\leq I_{OUT} \leq 100$ mA | | 3.17 | 3.3 | 3.43 | |
| | | 2 V $\leq V_{IN} \leq 5.5$ V, 1 mA $\leq I_{OUT} \leq 50$ mA | Full | 3.15 | | 3.45 | |
| | | 2.5 V $\leq V_{IN} \leq 5.5$ V, 1 mA $\leq I_{OUT} \leq 100$ mA | | 3.15 | | 3.45 | |
| Maximum Output Current | $I_{OUT(max)}$ | 2.5 V $\leq V_{IN} \leq 5.5$ V | Full | 100 | | | mA |
| Transient Load Current | | $I_{OUT} \leq 100$ mA (RMS) | 0 °C to 85 °C | | 200 | | |
| Quiescent Supply Current | I_Q | $V_{IN} = V_{SD} = 4$ V, $V_{FB} = 0$ V, Stepping Down | Full | | 60 | 100 | μA |
| | | $V_{IN} = V_{SD} = 2$ V, $V_{FB} = 0$ V, Stepping Up | | | 60 | 100 | |
| Shutdown Supply Current | I_{QSD} | 1.6 V $\leq V_{IN} \leq 5.5$ V, $V_{SD} = 0$ V | Full | | 1 | 5 | |
| Output Leakage Current in Shutdown | \overline{SD} | $V_{IN} = 2$ V, $V_{OUT} = 3.3$ V, $V_{SD} = 0$ V | Full | | 1 | 5 | |
| \overline{SD} Logic Input Voltage | V_{IL} | 1.6 V $\leq V_{IN} \leq 5.5$ V | Full | | | $0.25 * V_{IN}$ | V |
| | V_{IH} | | Full | $0.7 * V_{IN}$ | | | |
| \overline{SD} Input Leakage Current | | $V_{SD} = 5.5$ V | Full | - 1 | | 1 | μA |
| FB Regulation Voltage | V_{FB} | $V_{IN} = 1.65$ V, $V_{OUT} = 3.3$ V | Full | 1.205 | 1.235 | 1.265 | V |
| FB Input Current | I_{IFB} | $V_{FB} = 1.27$ V | Full | | 25 | 200 | nA |

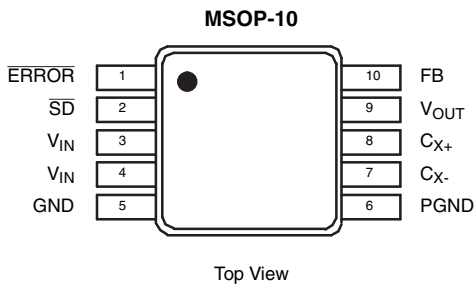
| SPECIFICATIONS | | | | | | | |
|------------------------------|-----------|---|--------------------|----------------------------|-------------------|------|---------------|
| Parameter | Symbol | Test Condition Unless Specified $V_{IN} = V_{SD} = 2\text{ V}$, $FB = PGND = GND$ $C_{IN} = 10\ \mu\text{F}$, $C_x = 0.33\ \mu\text{F}$, $C_{OUT} = 10\ \mu\text{F}$ | Temp. ^a | Limits - 40 °C to 85 °C | | | Unit |
| | | | | Min. | Typ. ^b | Max. | |
| FB Dual Mode Threshold | | Internal feedback | Full | | 100 | 50 | mV |
| | | External feedback | Full | 200 | 100 | | |
| ERROR Trip Voltage | | Falling edge at FB | Full | 1.0 | 1.1 | 1.2 | V |
| ERROR Output Low Voltage | V_{OL} | $I_{OL} = 0.5\ \text{mA}$, $V_{IN} = 2\ \text{V}$ | Full | | 5 | 100 | mV |
| ERROR Leakage Current | | $V_{ERROR} = 5.5\ \text{V}$, $V_{FB} = 1.27\ \text{V}$ | Full | | 0.01 | 0.2 | μA |
| Switching Frequency | f_{OSC} | $1.6\ \text{V} \leq V_{IN} \leq 5.5\ \text{V}$, $V_{FB} = 1\ \text{V}$ | Full | 1.2 | 1.5 | 1.8 | MHz |
| Output Short-Circuit Current | | $V_{OUT} = 0\ \text{V}$, $2.5\ \text{V} \leq V_{IN} \leq 5.5\ \text{V}$ foldback current limit | Full | | 110 | | mA |
| Thermal Shutdown Temperature | | Temperature rising | Full | | 160 | | °C |
| Thermal Shutdown Hysteresis | | | Full | | 20 | | |
| Efficiency | | $V_{IN} = 3.6\ \text{V}$, $I_{OUT} = 10\ \text{mA}$ | Full | | 90 | | % |

Notes:

a. Full = as determined by the operating suffix.

b. Typical values are for Design Aid only, not guaranteed nor subject to production testing.

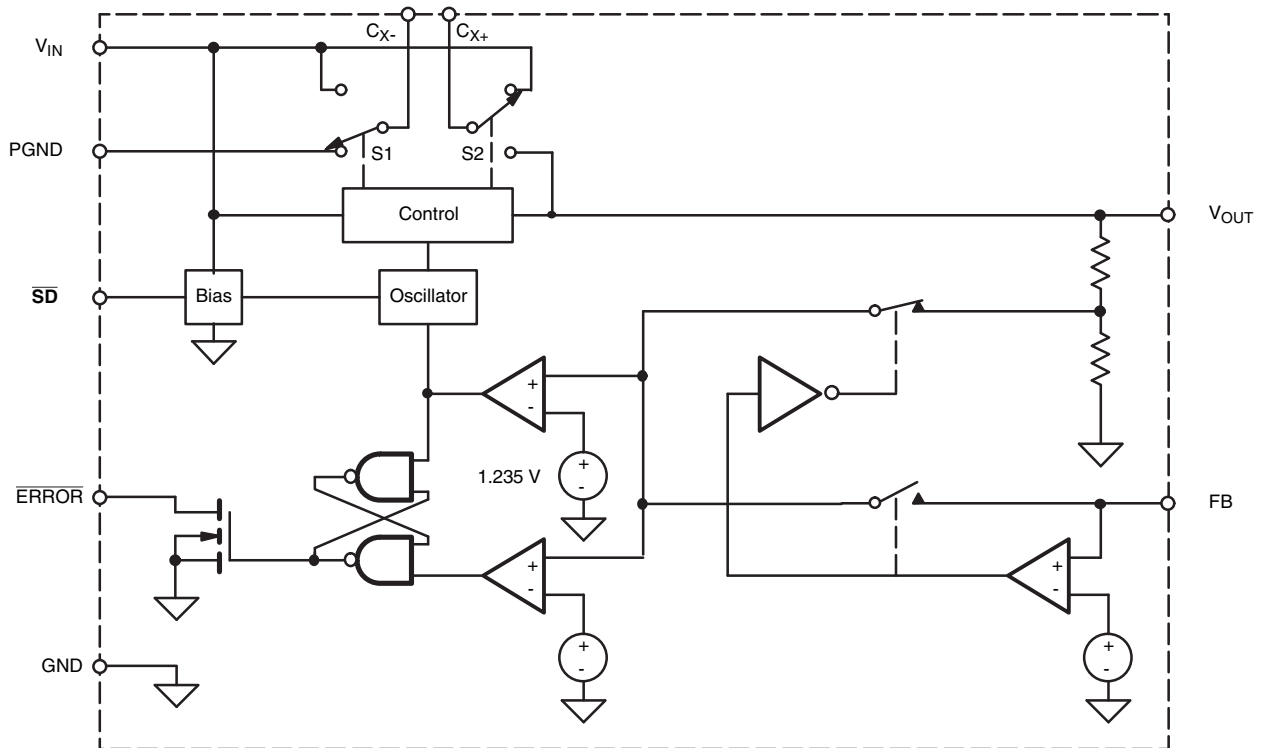
PIN CONFIGURATION AND TRUTH TABLE



| ORDERING INFORMATION | | |
|----------------------|-------------------|---------------|
| Part Number | Temperature Range | Marking |
| SiP1759DH-T1 | - 40 °C to 85 °C | 1759 |
| Eval Kit | Temperature Range | Board |
| SiP1759DB | - 40 °C to 85 °C | Surface Mount |

| PIN DESCRIPTION | | |
|-----------------|-----------------|---|
| Pin Number | Name | Function |
| 1 | ERROR | Open drain error flag - a low output indicates that the output voltage is out of range |
| 2 | \overline{SD} | Shutdown input |
| 3, 4 | V_{IN} | Input voltage |
| 5 | GND | Ground |
| 6 | PGND | Power ground |
| 7 | C_{X-} | Negative terminal of the charge pump capacitor |
| 8 | C_{X+} | Positive terminal of the charge pump capacitor |
| 9 | V_{OUT} | Regulated output voltage |
| 10 | FB | Feedback input - connected to GND for fixed 3.3 V output. Connected to a resistive divider for an adjustable output |

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

The SiP1759 is a buck-boost regulating charge pump. This allows for the V_{IN} to be a higher or lower voltage than the regulated output. This is done with a charge pump that when V_{IN} is lower than V_{OUT} is a regulated voltage doubler. When V_{IN} is higher than V_{OUT} the charge pump is a step down gated switch.

In boost mode, the IC controls the transfer capacitor through C_{X+} and C_{X-} pins, switching the charge to the output keeping it regulated. In this mode the charge pump only switches to maintain regulation, the output ripple does not increase with light loads. In buck mode, the C_{X-} pin is internally connected to PGND and the C_{X+} is switched internally between V_{IN} and V_{OUT} . Unless V_{IN} is significantly larger than V_{OUT} ($V_{IN} \geq V_{OUT} + 1\text{ V}$), in heavy load the IS will slip from buck mode to boost mode as necessary to charge the transfer capacitor.

Shutdown Mode

The IC is designed to conserve power by decreasing current consumption during normal operation as well as shutdown mode. Pulling the \overline{SD} pin logic low, the output is disconnected from the input and is in high impedance; the internal circuitry of the oscillator, control logic, and the charge-pump switches are turned off, decreasing the current consumption to less than $1\ \mu\text{A}$.

Undervoltage Lockout

When V_{IN} falls below 1 V the undervoltage lockout disables the SiP1759.

Power OK Output

POK is an open-drain output that goes low when the regulator feedback voltage falls below 1.1 V. A $10\ \text{k}\Omega$ to $1\ \text{M}\Omega$ pull-up resistor from POK to OUT should be used to provide a logic output and keep current consumption to a minimum. Connect POK to GND or leave floating if not used. The POK output is high impedance when the IC is in shutdown mode.

Fixed Output

The SiP1759 can be configured as a fixed 3.3 V output regulator or as an adjustable output from 2.5 V to 5.5 V. In the fixed 3.3 V output mode the feedback voltage is generated from the internal resistor-divider network. The FB pin must be tied to GND.

Soft-Start and Short Circuit Protection

The IC features a soft-start mechanism that limits the inrush current during start-up and if the output is short circuited the SiP1759 limits the output current to 110 mA.

Thermal Shutdown

The SiP 1759 is designed with a thermal shutdown circuit that will shut down the IC when the die temperature exceeds $160\ ^\circ\text{C}$. The thermal shutdown has $20\ ^\circ\text{C}$ of hysteresis, insuring when the die cools down the IC will turn on again.

DESIGNS CONSIDERATIONS

Setting the Adjustable Output Voltage

The SiP1759 regulated output can be adjusted from 2.5 V to 5.5 V via resistor divider network from V_{OUT} to GND (see Typical Application Circuits). R1 and R2 should be kept in the 50 k Ω to 100 k Ω range for low power consumption, while maintaining adequate noise immunity. The value R1 is calculated using the following formula:

$$R1 = R2 \{ (V_{OUT}/V_{FB}) - 1 \}$$

V_{FB} is nominally 1.235 V.

Capacitor Selection

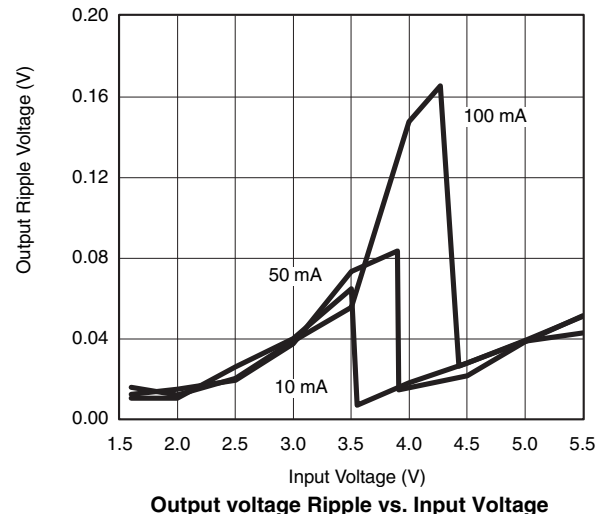
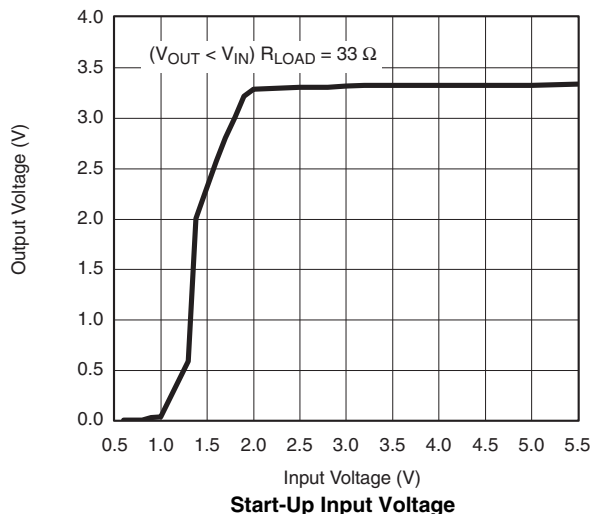
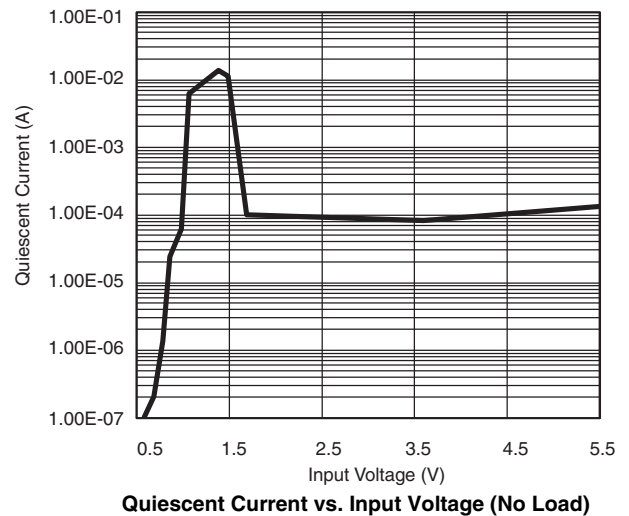
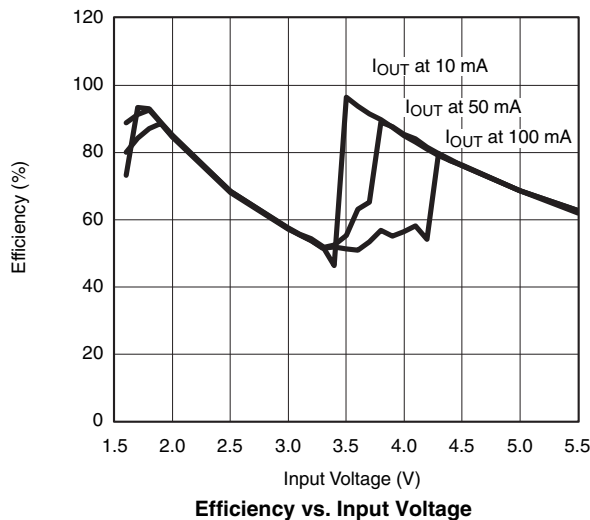
Capacitor selection for C_{IN} , C_{OUT} and C_X will have an impact in the voltage output ripple, output current and overall physical size of the circuit.

Ceramic capacitors are recommended for their low ESR (≤ 20 m Ω) which will help keep the output voltage ripple at a minimum. The initial values for the C_{IN} and C_{OUT} capacitors should be 10 μ F, the C_X capacitor should be 0.33 μ F.

Output Voltage Ripple

The SiP1759 automatically decides whether to be in step up mode or step down mode depending on the V_{IN} , V_{OUT} and current load conditions, therefore the voltage output ripple will vary. In step-up mode the voltage output ripple is higher than step-down mode. But unless V_{IN} is significant larger than V_{OUT} ($V_{IN} \geq V_{OUT} + 1$ V), in heavy load the IC will slip from buck mode to boost mode as necessary to charge the transfer capacitor and the ripple will increase. Reducing the C_X capacitor value will cause an increase in the switching frequency and a reduction of the output ripple.

TYPICAL CHARACTERISTICS



TYPICAL WAVEFORMS

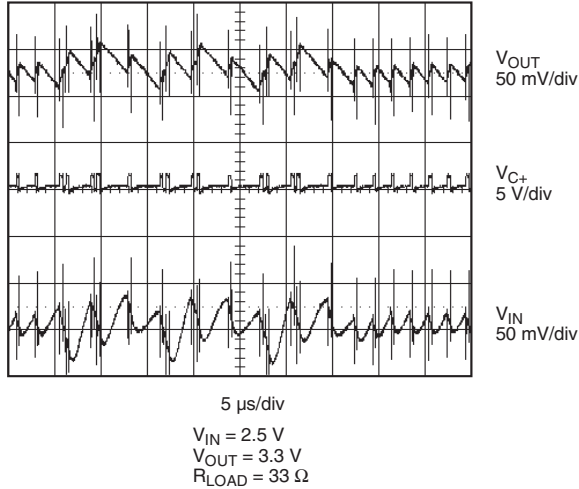


Figure 1. Typical Switching Waveform ($V_{OUT} > V_{IN}$)

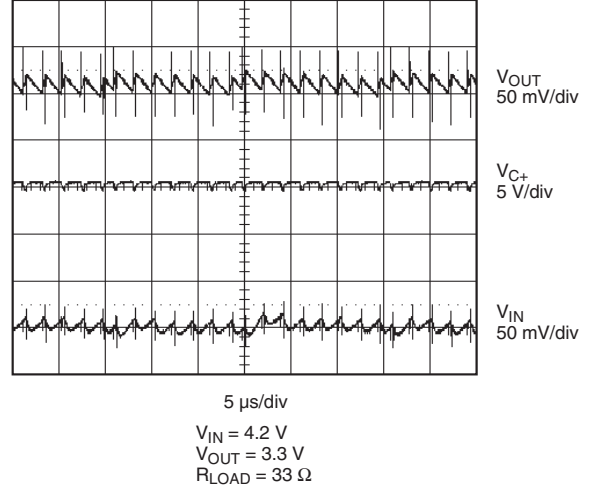


Figure 2. Typical Switching Waveforms ($V_{OUT} > V_{IN}$)

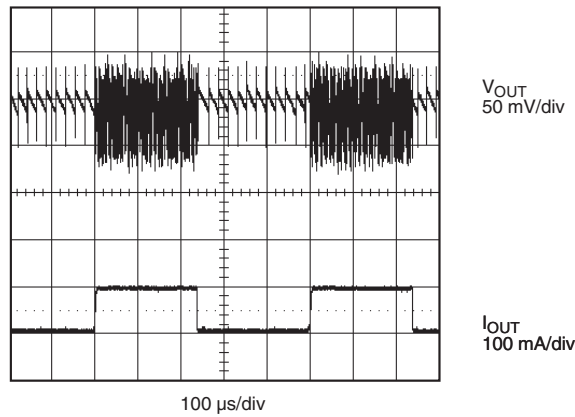


Figure 3. Load Transient Response ($V_{OUT} > V_{IN}$)

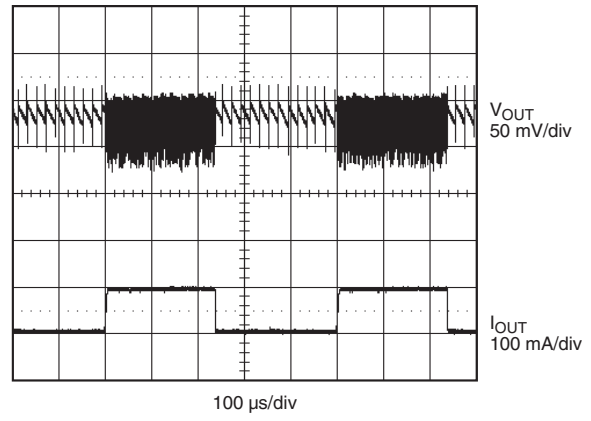


Figure 4. Load Transient Response ($V_{OUT} < V_{IN}$)

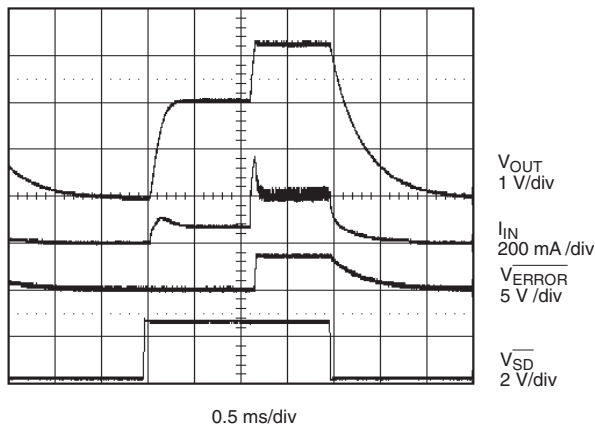


Figure 5. Turn On/Off Response ($V_{IN} = 2.5\text{ V}$)

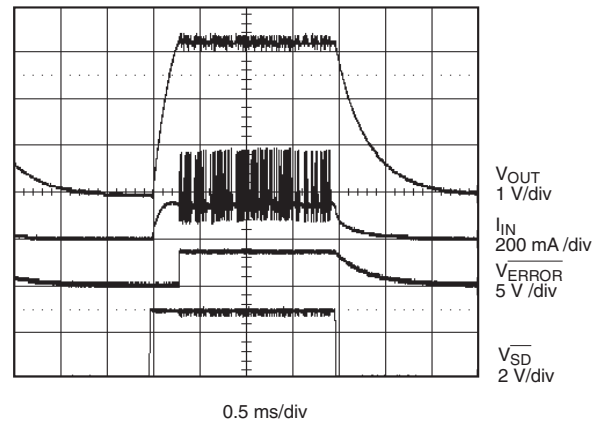
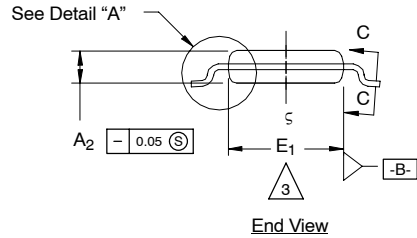
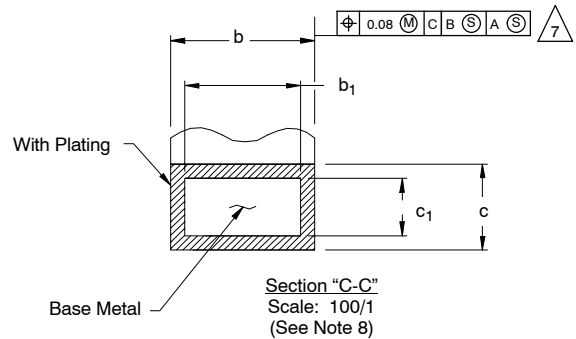
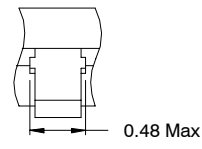
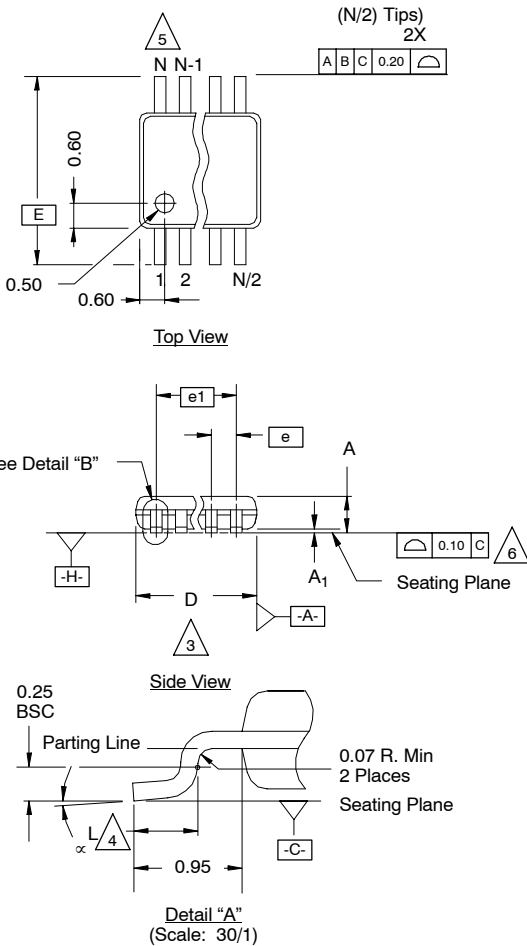


Figure 6. Turn On/Off Response ($V_{IN} = 4.2\text{ V}$)

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MSOP: 10-LEADS (POWER IC ONLY)
JEDEC Part Number: MO-187, (Variation AA and BA)



NOTES:

- Die thickness allowable is 0.203 ± 0.0127 .
- Dimensioning and tolerances per ANSI.Y14.5M-1994.
- Dimensions "D" and "E₁" do not include mold flash or protrusions, and are measured at Datum plane [-H-], mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimension is the length of terminal for soldering to a substrate.
- Terminal positions are shown for reference only.
- Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
- The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
- Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
- Controlling dimension: millimeters.
- This part is compliant with JEDEC registration MO-187, variation AA and BA.
- Datums [-A-] and [-B-] to be determined Datum plane [-H-].
- Exposed pad area in bottom side is the same as teh leadframe pad size.

N = 10L

| Dim | MILLIMETERS | | | Note |
|---|-------------|------|------|------|
| | Min | Nom | Max | |
| A | - | - | 1.10 | |
| A ₁ | 0.05 | 0.10 | 0.15 | |
| A ₂ | 0.75 | 0.85 | 0.95 | |
| b | 0.17 | - | 0.27 | 8 |
| b ₁ | 0.17 | 0.20 | 0.23 | 8 |
| c | 0.13 | - | 0.23 | |
| c ₁ | 0.13 | 0.15 | 0.18 | |
| D | 3.00 BSC | | | 3 |
| E | 4.90 BSC | | | |
| E ₁ | 2.90 | 3.00 | 3.10 | 3 |
| e | 0.50 BSC | | | |
| e ₁ | 2.00 BSC | | | |
| L | 0.40 | 0.55 | 0.70 | 4 |
| N | 10 | | | 5 |
| α | 0° | 4° | 6° | |
| ECN: S-40082—Rev. A, 02-Feb-04 DWG: 5922 | | | | |



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