

# MJD122, NJVMJD122 (NPN), MJD127, NJVMJD127 (PNP)

## Complementary Darlington Power Transistor

### DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

#### Features

- Lead Formed for Surface Mount Applications in Plastic Sleeves
- Surface Mount Replacements for 2N6040–2N6045 Series, TIP120–TIP122 Series, and TIP125–TIP127 Series
- Monolithic Construction With Built-in Base–Emitter Shunt Resistors
- High DC Current Gain:  $h_{FE} = 2500$  (Typ) @  $I_C = 4.0$  Adc
- Epoxy Meets UL 94 V–0 @ 0.125 in
- ESD Ratings:
  - ♦ Human Body Model,  $3B > 8000$  V
  - ♦ Machine Model,  $C > 400$  V
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant



ON Semiconductor®

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**SILICON  
POWER TRANSISTOR  
8 AMPERES  
100 VOLTS, 20 WATTS**



**DPAK  
CASE 369C  
STYLE 1**



#### MARKING DIAGRAM



A = Assembly Location  
Y = Year  
WW = Work Week  
x = 2 or 7  
G = Pb–Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	100	Vdc
Collector–Base Voltage	$V_{CB}$	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5	Vdc
Collector Current Continuous Peak	$I_C$	8 16	Adc
Base Current	$I_B$	120	mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16	W W/ $^\circ\text{C}$
Total Power Dissipation (Note 1) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.75 0.014	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	6.25	$^\circ\text{C/W}$
Thermal Resistance, Junction–to–Ambient (Note1)	$R_{\theta JA}$	71.4	$^\circ\text{C/W}$

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

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## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	$V_{CE(sus)}$	100	–	Vdc
Collector Cutoff Current ( $V_{CE} = 50\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	–	10	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	–	10	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	2	mAdc

### ON CHARACTERISTICS

DC Current Gain ( $I_C = 4\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ ) ( $I_C = 8\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )	$h_{FE}$	1000 100	12,000 –	–
Collector–Emitter Saturation Voltage ( $I_C = 4\text{ Adc}$ , $I_B = 16\text{ mAdc}$ ) ( $I_C = 8\text{ Adc}$ , $I_B = 80\text{ mAdc}$ )	$V_{CE(sat)}$	– –	2 4	Vdc
Base–Emitter Saturation Voltage (Note 2) ( $I_C = 8\text{ Adc}$ , $I_B = 80\text{ mAdc}$ )	$V_{BE(sat)}$	–	4.5	Vdc
Base–Emitter On Voltage ( $I_C = 4\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )	$V_{BE(on)}$	–	2.8	Vdc

### DYNAMIC CHARACTERISTICS

Current–Gain–Bandwidth Product ( $I_C = 3\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$ h_{fe} $	4	–	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ ) MJD127, NJVMJD127 MJD122, NJVMJD122	$C_{ob}$	– –	300 200	pF
Small–Signal Current Gain ( $I_C = 3\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ , $f = 1\text{ kHz}$ )	$h_{fe}$	300	–	–

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

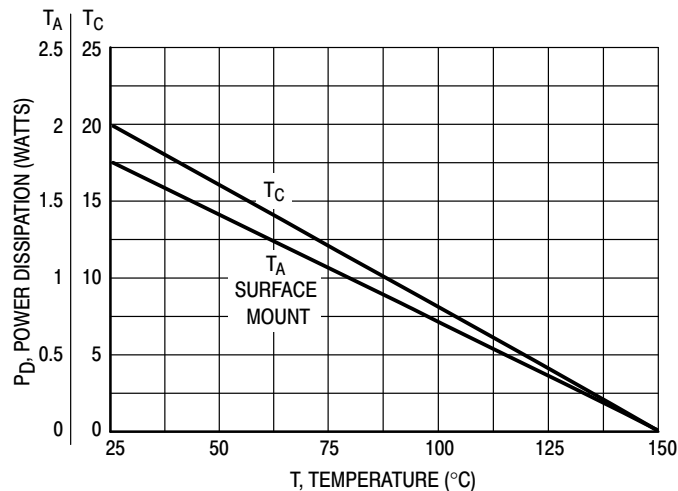


Figure 1. Power Derating

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## TYPICAL ELECTRICAL CHARACTERISTICS



Figure 2. DC Current Gain



Figure 3. Collector Saturation Region



Figure 4. "On" Voltages

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## TYPICAL ELECTRICAL CHARACTERISTICS



Figure 5. Temperature Coefficients

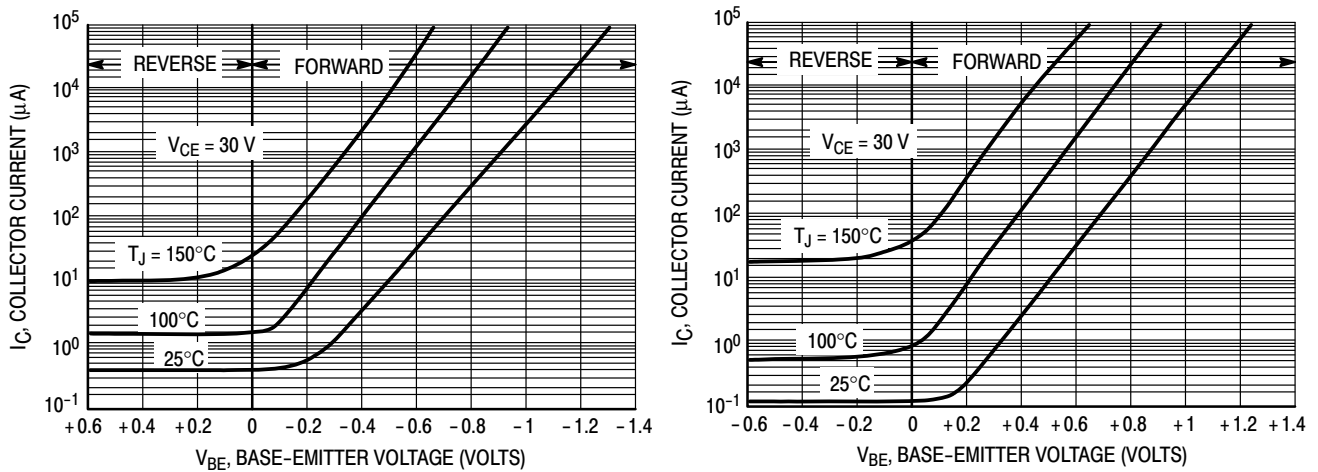


Figure 6. Collector Cut-Off Region



Figure 7. Small-Signal Current Gain



Figure 8. Capacitance

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Figure 9. Switching Times Test Circuit



Figure 10. Switching Times



Figure 11. Thermal Response



Figure 12. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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Figure 13. Darlington Schematic

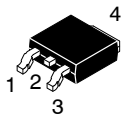
### ORDERING INFORMATION

Device	Package Type	Shipping†
MJD122G	DPAK (Pb-Free)	75 Units / Rail
MJD122T4G	DPAK (Pb-Free)	2,500 / Tape & Reel
NJVMJD122T4G*	DPAK (Pb-Free)	2,500 / Tape & Reel
MJD127G	DPAK (Pb-Free)	75 Units / Rail
MJD127T4G	DPAK (Pb-Free)	2,500 / Tape & Reel
NJVMJD127T4G*	DPAK (Pb-Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



## DPAK (SINGLE GAUGE) CASE 369C ISSUE F

DATE 21 JUL 2015

SCALE 1:1



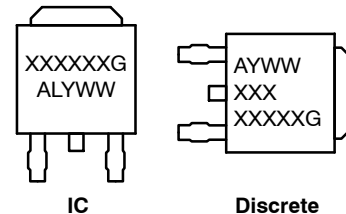
**NOTES:**

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
- OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### GENERIC MARKING DIAGRAM\*

- |   |   |  |  |   |
|---|---|--|--|---|
| <p><b>STYLE 1:</b><br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p><b>STYLE 2:</b><br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p>          | <p><b>STYLE 3:</b><br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p> | <p><b>STYLE 4:</b><br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p>              | <p><b>STYLE 5:</b><br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>     |
| <p><b>STYLE 6:</b><br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>                 | <p><b>STYLE 7:</b><br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p><b>STYLE 8:</b><br/>PIN 1. N/C<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>   | <p><b>STYLE 9:</b><br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. RESISTOR ADJUST<br/>4. CATHODE</p> | <p><b>STYLE 10:</b><br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p> |



- XXXXXX = Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 WW = Work Week  
 G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

### SOLDERING FOOTPRINT\*



SCALE 3:1  $\left( \frac{\text{mm}}{\text{inches}} \right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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