

Evaluating the ADL8142 GaAs, pHEMT, MMIC, Low Noise Amplifier, 23 GHz to 31 GHz

FEATURES

- ▶ 4-layer, Rogers 4003C and Isola Group 370HR evaluation board
- ▶ End launch, 2.92 mm RF connectors
- ▶ Through calibration path (depopulated)

EVALUATION KIT CONTENTS

- ▶ ADL8142-EVALZ evaluation board

EQUIPMENT NEEDED

- ▶ RF signal generator
- ▶ RF spectrum analyzer
- ▶ RF network analyzer
- ▶ 4 V, 100 mA power supply

GENERAL DESCRIPTION

The ADL8142-EVALZ consists of a 4-layer printed circuit board (PCB) fabricated from 8 mil thick, Rogers 4003C and Isola 370HR, copper clad, forming a nominal thickness of 62 mils. The RFIN and RFOUT ports on the ADL8142-EVALZ are populated with 2.92 mm, female coaxial connectors, and the corresponding RF traces have a 50 Ω characteristic impedance. The ADL8142-EVALZ is populated with components suitable for use over the entire -40°C to $+85^{\circ}\text{C}$ operating temperature range of the [ADL8142](#). To calibrate board trace losses, a through calibration path is provided between the J1 and J2 connectors. J1 and J2 must be populated with RF connectors to use the through calibration path. Refer to [Table 1](#) and [Figure 3](#) for the through calibration path performance.

Access the ADL8142-EVALZ ground path and VDD pin through the surface-mount technology (SMT) test point connectors, GND and VDD. A supplementary test point for VBIAS is included for simple access on the RBIAS pin (see [Figure 5](#) for the test point assembly).

The RF traces on the ADL8142-EVALZ are 50 Ω , grounded, coplanar waveguide. The package ground leads and the exposed pad connect directly to the ground plane. Multiple vias connect the top and bottom ground planes with particular focus on the area directly beneath the ground paddle to provide adequate electrical conduction and thermal conduction to the heat sink.

The power supply decoupling capacitors on the ADL8142-EVALZ represent the configuration used to characterize and qualify the device.

For full details on the ADL8142, see the ADL8142 data sheet, which must be consulted in conjunction with this user guide when using the ADL8142-EVALZ.

EVALUATION BOARD PHOTOGRAPHS

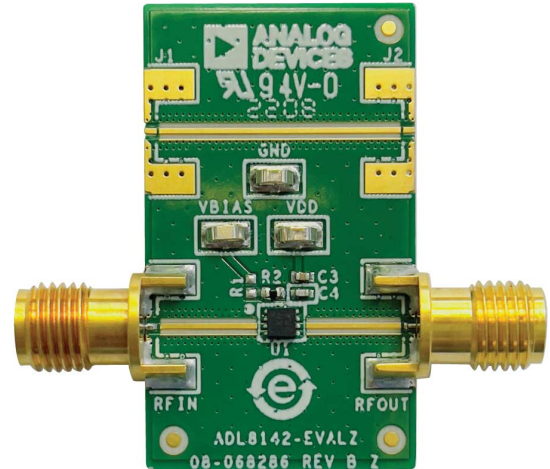


Figure 1. ADL8142-EVALZ Primary Side

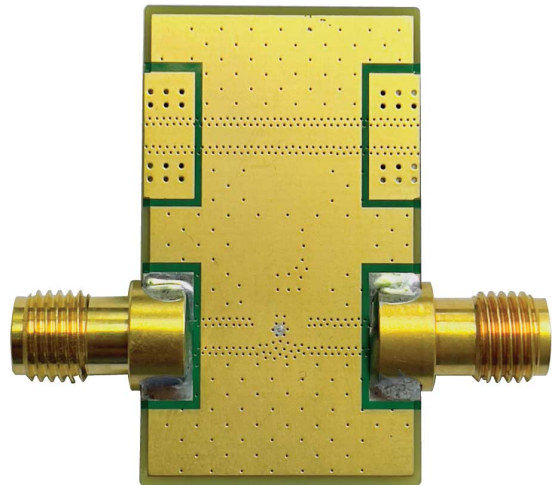


Figure 2. ADL8142-EVALZ Secondary Side

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REVISION HISTORY**4/2022—Revision 0: Initial Version**

OPERATING THE ADL8142-EVALZ

A 2 V, 100 mA power supply is required to provide the bias to the ADL8142 when using the ADL8142-EVALZ. Connect the 2 V power supply to the SMT test point, VDD. Connect the ground reference to the GND test point. Apply the RF power after V_{DD} has been turned on and remove the RF power before V_{DD} is turned off.

Refer to the ADL8142 data sheet for the recommended resistor values to achieve different supply currents. The following bias conditions are recommended to achieve optimal performance: V_{DD} = 2 V and quiescent current (I_{DQ}) = 25 mA. I_{DQ} is typically achieved using a 634 Ω value for the bias resistance (R_{BIAS}).

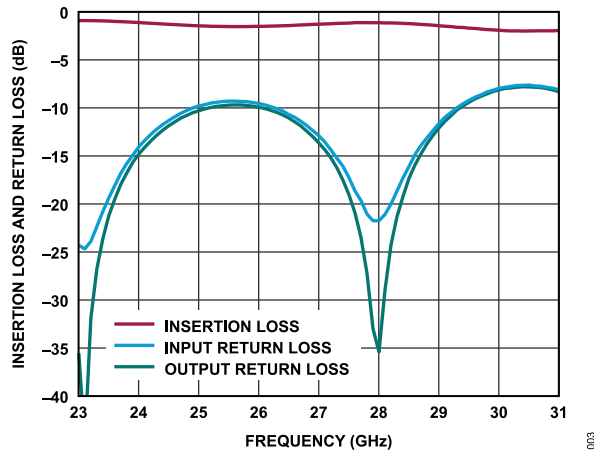


Figure 3. Insertion Loss and Return Loss of the Through Calibration Path, 23 GHz to 31 GHz

Table 1. Insertion Loss and Return Loss of the Through Calibration Path

| Frequency (GHz) | Insertion Loss (dB) | Input Return Loss (dB) | Output Return Loss (dB) |
|-----------------|---------------------|------------------------|-------------------------|
| 23 | -0.908 | -24.304 | -35.554 |
| 23.5 | -0.959 | -19.365 | -21.21 |
| 24 | -1.111 | -14.038 | -14.799 |
| 24.5 | -1.299 | -11.303 | -11.85 |
| 25 | -1.461 | -9.793 | -10.294 |
| 25.5 | -1.537 | -9.301 | -9.71 |
| 26 | -1.519 | -9.532 | -9.931 |
| 26.5 | -1.438 | -10.699 | -11.062 |
| 27 | -1.293 | -12.907 | -13.664 |
| 27.5 | -1.177 | -17.255 | -19.039 |
| 28 | -1.137 | -21.744 | -35.417 |
| 28.5 | -1.235 | -16.089 | -17.334 |
| 29 | -1.453 | -11.593 | -12.081 |
| 29.5 | -1.705 | -9.217 | -9.417 |
| 30 | -1.92 | -7.958 | -8.139 |
| 30.5 | -1.993 | -7.623 | -7.823 |
| 31 | -1.941 | -8.134 | -8.333 |

RECOMMENDED BIAS SEQUENCING

During Power-Up

To power up the ADL8142-EVALZ, take the following bias sequencing steps:

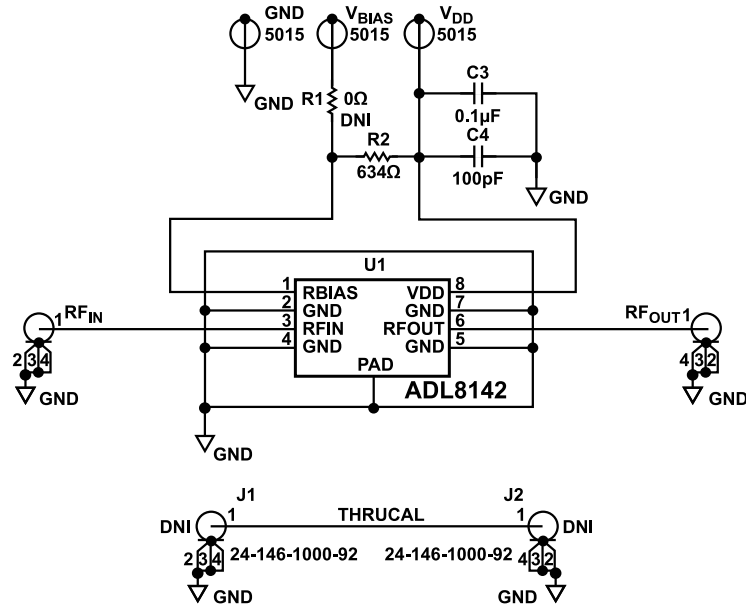
1. Connect the VDD power supply.
2. Set the VDD supply to 2 V.
3. Apply the RF input signal.

During Power-Down

To power down the ADL8142-EVALZ, take the following bias sequencing steps:

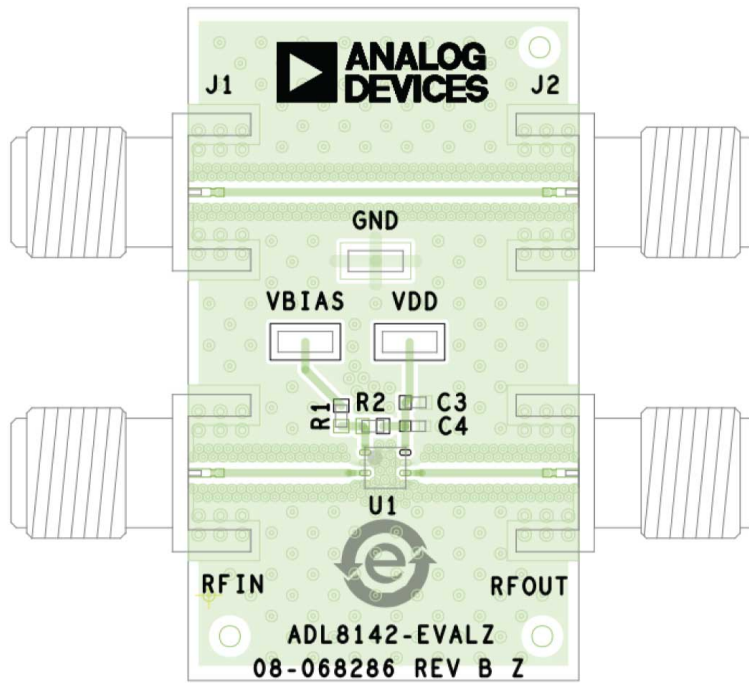
1. Turn off the RF input signal.
2. Set the VDD supply to 0 V.

EVALUATION BOARD SCHEMATIC AND ARTWORK



004

Figure 4. ADL8142-EVALZ Schematic



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Figure 5. ADL8142-EVALZ Assembly Drawing (J1 and J2 Not Installed)

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

| Reference Designator | Description | Manufacturer | Part Number |
|----------------------|-------------------------------------------------------------------------------------------------|------------------------|------------------|
| C3 | Capacitor, ceramic, 0.1 μ F, 16 V, 10%, X7R, 0402 | Samsung | CL05B104K05NNNC |
| C4 | Capacitor, ceramic, 100 pF, 50 V, 5%, COG, 0402, extreme low, effective series resistance (ESR) | KEMET | C0402C101J5GACTU |
| GND, VBIAS, VDD | Connectors, SMT test points | Keystone Electronics | 5015 |
| J1, J2 | Connectors, 2.92 mm, jack edge, do not install (DNI) | SRI Connector Gage Co. | 25-146-1000-92 |
| R1 | Resistor, 0402, SMD chip, precision, 0 Ω , DNI | Panasonic | ERJ-2GE0R00X |
| R2 | Resistor, 0402, SMD chip, precision, 634 Ω | Panasonic | ERJ-2RKF6340X |
| RFIN, RFOUT | Connectors, 2.92 mm, jack edge | SRI Connector Gage Co. | 25-146-1000-92 |
| U1 | GaAs, pHEMT, MMIC, low noise amplifier, 23 GHz to 31 GHz | Analog Devices, Inc. | ADL8142 |

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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