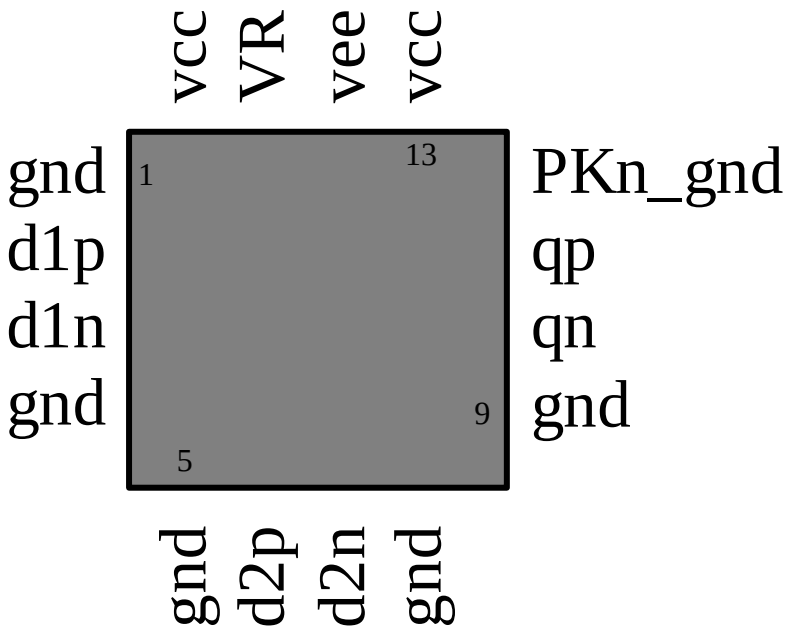
ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Dr., Ste #112, Torrance, CA 90505

Office: (310) 530-9400 Fax: (310) 530-9402
www.adsantec.com

IFC211 / ASNT5143-ALD
DC-32*GHz* XOR Logic Gate

- High speed broadband Exclusive-OR (XOR) Boolean logic gate
- Fully differential CML input interfaces
- Fully differential CML output interface with externally adjustable voltage swing
- Optional external adjustment of peaking/bandwidth
- Single +3.1*V* or -3.1*V* power supply
- Ground-independent floating supplies to allow for the output common mode voltage adjustment
- Power consumption: 250*mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom 16-pin QFN package with exposed die substrate at the top



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DESCRIPTION

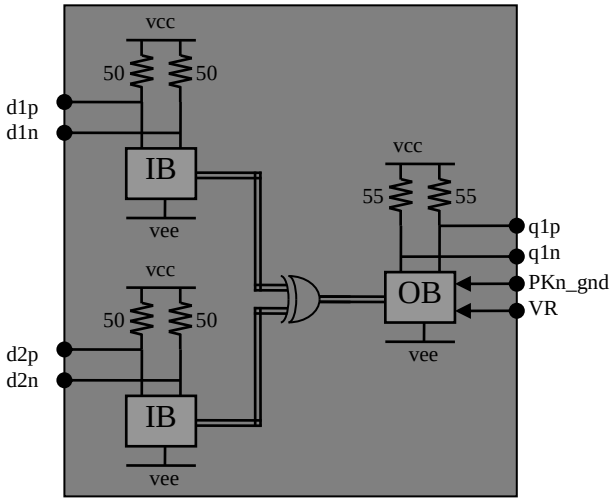

Fig. 1. Functional Block Diagram.

This SiGe IC provides broadband Exclusive-OR (XOR) Boolean logic functionality, and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can perform XOR operation with a high-speed data or clock input signal d1p/d1n and another high-speed data or clock input signal d2p/d2n. The resulting high-speed double-rate or double-frequency output signal is delivered to the output port q1p/q1n.

The part's inputs and outputs support the CML logic interface with on chip 50*Ohm* or 55*Ohm* termination to vcc respectively, and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS.

In the input AC-coupling mode, the input termination provides the required common mode voltage automatically. In this case, the output can be used in DC-coupling mode and its common mode voltage can be adjusted using floating power supplies as described in the POWER SUPPLY CONFIGURATION section below.

The output signal amplitude can be controlled by applying external voltage to the port VR.

The part's bandwidth (or AC-characteristic peaking) can be controlled by applying external voltage to the port PKn. The pin can be left not connected to provide the minimum peaking and bandwidth, or connected to vee to provide the maximum peaking and bandwidth.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground), or positive supply (vee = 0.0*V* = ground), or floating supply as described below. In case of the positive or floating supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

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Two floating supply configurations are shown in Fig. 2. In this case, the part's output common mode voltage can be adjusted by modifying the voltage of PSU1. The negative supply configuration provides common mode voltages below ground while the positive supply configuration delivers common mode voltages above ground.

Fig. 2. Negative (a) and Positive (b) Floating Supply Configurations

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
d1p	2	CML input	Differential data/clock inputs with internal SE 50*Ohm* termination to vcc
d1n	3		
d2p	6	CML input	Differential data/clock inputs with internal SE 50*Ohm* termination to vcc
d2n	7		
q1p	11	CML output	Differential data outputs with internal SE 55*Ohm* termination to vcc. Require either external SE 55*Ohm* terminations to vcc, or differential 110*Ohm* termination.
q1n	10		
Low-Speed Control Ports			
Pkn-gnd	12	Analog	DC control input with internal 32*KOhm* termination to vcc
VR	15	Analog	DC control input with internal 6.4*KOhm* termination to vcc

Supply and Termination Voltages		
Name	Description	Pin Number
vcc	Positive power supply. (+2.8*V* or 0)	13, 16
vee	Negative power supply. (0*V* or -2.8*V*)	14
gnd	Floating ground (AC-decoupled to vee on chip)	1, 4, 5, 8, 9

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied.

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Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Positive supply voltage (vcc)	0	3.6	*V*
Negative supply voltage (vee)	vcc-3.6	0	*V*
RF Input voltage swing (SE)		0.8	*V*
Case temperature		+100	*ºC*
Storage temperature	-40	+100	*ºC*
Operational/storage humidity	10	98	*%*

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Notes
General Parameters						
Positive supply voltage	vcc	1.2		1.6	*V*	*Recommended range*
Negative supply voltage	vee	vcc-3.1		vcc-2.8	*V*	
Power consumption			225		*mW*	*at 2.8V supply*
			250		*mW*	*at 3.1V supply*
Junction temperature		-40		125	*ºC*	
High-Speed Inputs						
Number of ports			2			*Differential*
On-chip termination	Rin		50		*Ohm*	*Each input pin to vcc*
Input resistance			100		*Ohm*	*Differential*
Data rate		DC		28	*Gbps*	*for PRBS-type input signal*
Clock Speed		DC		28	*GHz*	
Voltage swing	ΔV_{in}	50		400	*mV*	*pk-pk, each SE input pin*
Common mode level		vcc-0.4		vcc-$\Delta V_{in}/2$	*V*	
Input return loss	S11		TBD		*dB*	*in BW*
High-Speed Outputs						
On-chip termination	Rout		55		*Ohm*	*Each output pin to vcc*
Data rate		DC		32	*Gbps*	*PRBS eye opening >600mV*
		DC		36	*Gbps*	*PRBS eye opening >530mV*
Clock Speed		DC		32	*GHz*	
Latency	t_L		TBD		*ps*	*Packaged die*
Rise/Fall time	t_R/t_F	8.5		14	*ps*	
Jitter				2	*ps*	*Peak-to-peak, PRBS7 input*
Logic “1” voltage level	V^1		vcc		*V*	
Logic “0” voltage level	V^0	vcc-0.8		vcc-0.1		*For VR from Max to Min*
Voltage swing	ΔV_{out}	1600		200	*mV*	*Differential, pk-pk*
Output return loss	S22		TBD		*dB*	*in BW*
Manual Amplitude Control Port (VR)						
Input voltage range		vcc-0.6		vcc-0.3	*V*	*Max output swing at vcc-0.3*
Manual Peaking Control Port (PKn_gnd)						
Input voltage range		vee		vcc	*V*	*Faster slope at lower voltage*

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PACKAGE INFORMATION

The flip-chip die is housed in a custom 16-pin QFN package shown in Fig. 3. The back side of the die is exposed at the top of the package to provide the heat dissipation path. An external heat sink can be attached to the exposed top.

The InfoCube part's identification label is IFC211. The Adsnatec part's identification label is ASNT5143-ALD. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

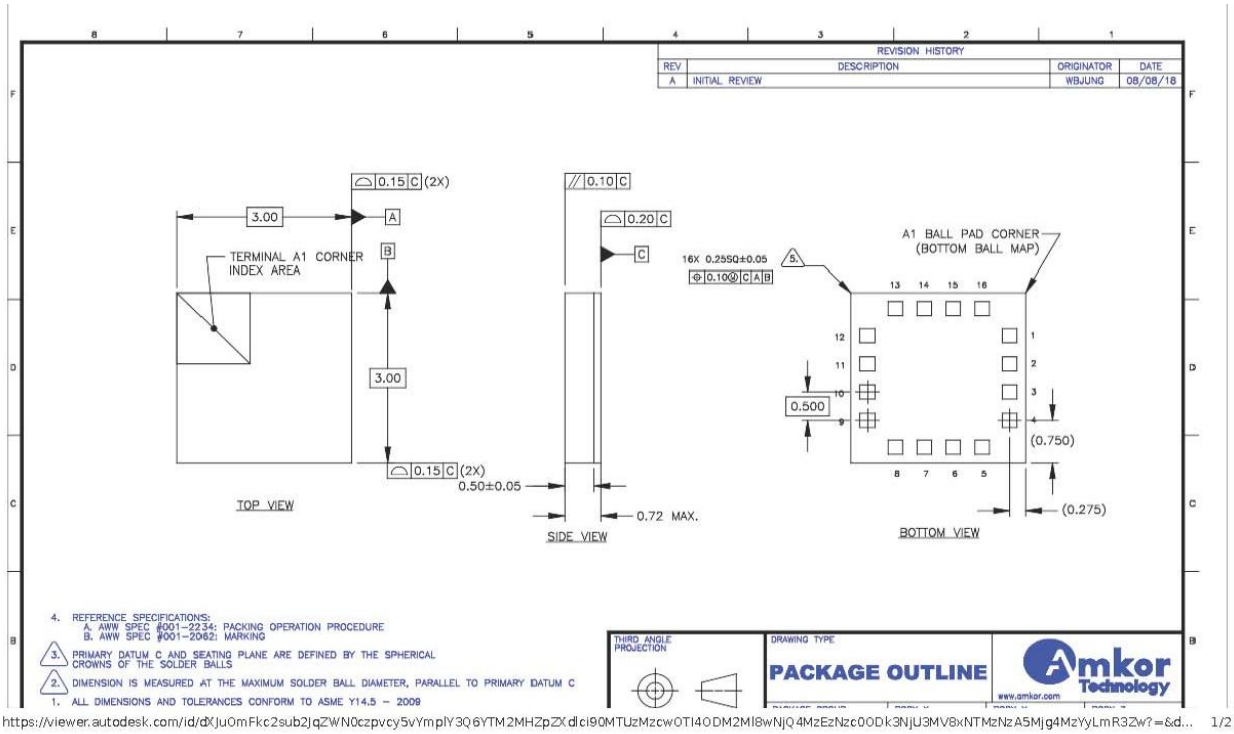

Fig. 3. LGA 16-Pin Package Drawing (All Dimensions in mm)

REVISION HISTORY

Revision	Date	Changes
1.3.2	01-2020	Corrected clock speed
1.2.2	11-2019	Corrected title Corrected maximum speed Corrected header
1.1.1	01-2019	Corrected ADSANTEC chip name Corrected electrical Specifications Added package drawing
1.0.1	04-2018	Preliminary release.