# C57401  C57401A  C57402  C57402A
# 57401    57401A   57402   57402A

## Military Standard FIFOs 64x4 64x5
## Cascadable & Standalone Memory

Advanced
Micro
Devices

## DISTINCTIVE CHARACTERISTICS

- Choice of 7 or 10 MHz shift-out/shift-in rates
- Choice of standalone or cascadable devices
- Choice of 4-bit or 5-bit data width
- TTL Inputs and outputs
- Cascadable devices readily expandable in the word and bit dimension
- Standalone devices expandable in the word dimension only

- Structured pinouts. Output pins directly opposite corresponding inputs pins
- Asynchronous operation
- Dose rate (transient upset) junction-isolated bipolar process $2\times10^{10}$ RADs (SI)/s recovery time of 50 to 70 $\mu$s from a 1$\mu$s pulse
- Neutron fluence (permanent damage): $1\times10^{13}$ N/cm$^2$

## GENERAL DESCRIPTION

The C/57401/1A and C57402/2A are "fall through" high-speed First-In First-Out (FIFO) memories organized 64 words by 4 bits and 64 words by 5 bits respectively. FIFO word width and depth are expandable on cascadable devices. Standalone devices are expandable in word width only.
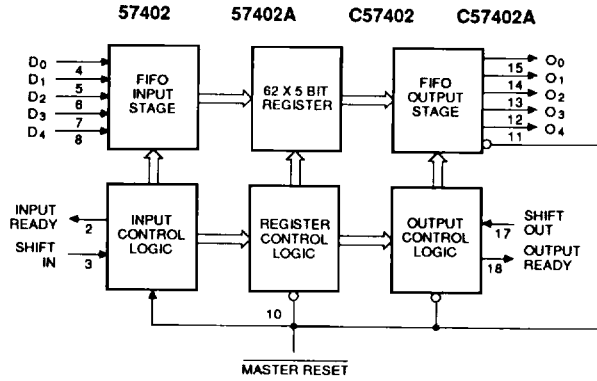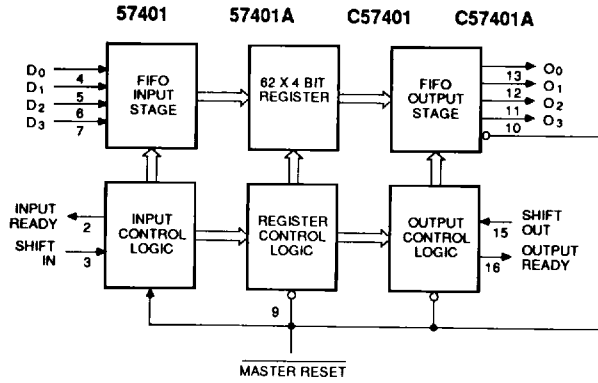
## Ordering Information

| PART NUMBER | PINS | PACKAGE | PACKAGE TYPE | MIL-M-38510 CASE OUTLINE | CASCADABLE/ STANDALONE | DESCRIPTION |
|---|---|---|---|---|---|---|
| 57401* | 16 | CD 016 | Ceramic Dip | D-2 | Standalone | 7 MHz 64X4 FIFO |
|  |  | CL 020 | Leadless Chip Carrier | C-2 | Standalone |  |
| 57401A* | 16 | CD 016 | Ceramic Dip | D-2 | Standalone | 10 MHz 64X4 FIFO |
|  |  | CL 020 | Leadless Chip Carrier | C-2 | Standalone |  |
| 57402 | 18 | CD 018 | Ceramic Dip | D-6 | Standalone | 7 MHz 64X5 FIFO |
|  |  | CL 020 | Leadless Chip Carrier | C-2 | Standalone |  |
| 57402A | 18 | CD 018 | Ceramic Dip | D-6 | Standalone | 10 MHz 64X5 FIFO |
|  |  | CL 020 | Leadless Chip Carrier | C-2 | Standalone |  |
| C57401* | 16 | CD 016 | Ceramic Dip | D-2 | Cascadable | 7 MHz 64X4 FIFO |
|  |  | CL 020 | Leadless Chip Carrier | C-2 | Cascadable |  |
| C57401A* | 16 | CD 016 | Ceramic Dip | D-6 | Cascadable | 10 MHz 64X4 FIFO |
|  |  | CL 020 | Leadless Chip Carrier | C-2 | Cascadable |  |
| C57402 | 18 | CD 018 | Ceramic Dip | D-6 | Cascadable | 7 MHz 64X5 FIFO |
|  |  | CL 020 | Leadless Chip Carrier | C-2 | Cascadable |  |
| C57402A | 18 | CD 018 | Ceramic Dip | D-6 | Cascadable | 10 MHz 64X5 FIFO |
|  |  | CL 020 | Leadless Chip Carrier | C-2 | Cascadable |  |

* Also available in Ceramic Flatpackage. Contact factory for detail.
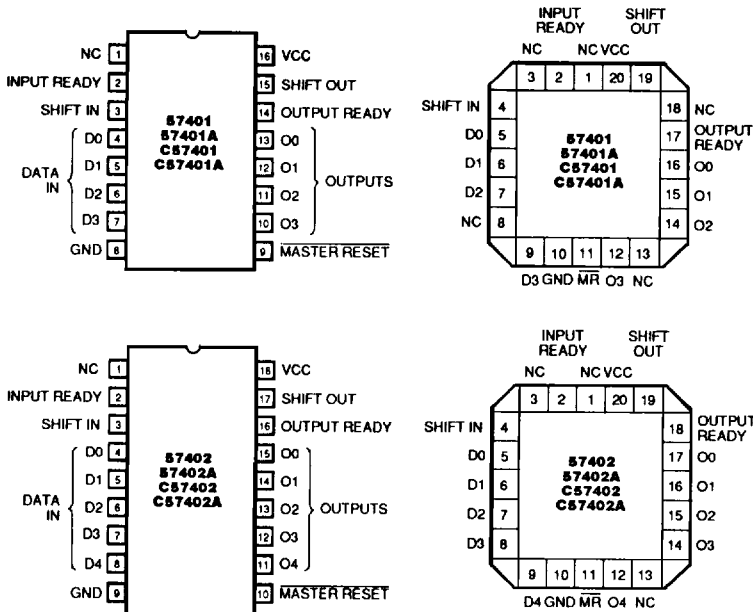
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## BLOCK DIAGRAMS
### DIP Pinout

**57401    57401A    C57401    C57401A**



**57402    57402A    C57402    C57402A**



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## CONNECTION DIAGRAMS



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## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ ............................................ –0.5 V to 7 V

Input voltage ......................................................... –1.5 V to 7 V

Off-state output voltage .................................... –0.5 V to 5.5 V

Storage Temperature ................................... –65°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and a functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability. Absolute maximum ratings are for system design reference; parameters given are not tested.*

## OPERATING CONDITIONS 57401/2

| Symbol | Parameter | Figure | Military | | | Unit |
| | | | Min | Typ | Max | |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $T_A^*$ | Operating temperature | | –55 | | 125 | °C |
| $t_{SIH}^\dagger$ | Shift in HIGH time | 1 | 45 | | | ns |
| $t_{SIL}$ | Shift in LOW time | 1 | 45 | | | ns |
| $t_{IDS}$ | Input data setup | 1 | 10 | | | ns |
| $t_{IDH}$ | Input data hold time | 1 | 55 | | | ns |
| $f_{IN}$ | Shift in rate | 1 | 7 | | | MHz |
| $f_{OUT}$ | Shift Out rate | 4 | 7 | | | MHz |
| $t_{SOH}^\dagger$ | Shift Out HIGH time | 4 | 45 | | | ns |
| $t_{SOL}$ | Shift Out LOW time | 4 | 45 | | | ns |
| $t_{MRW}$ | Master Reset pulse$^\dagger$ | 8 | 30 | | | ns |
| $t_{MRS}^{**}$ | Master Reset to SI | 8 | 45 | | | ns |

\* Instant-On Case Temperature

\*\* $t_{MRS}$ is measured on initial characterization lots only and is not directly tested in production.

## SWITCHING CHARACTERISITCS 57401/2 Over Operating Conditions

| Symbol | Parameter | Figure | Military | | Unit |
| | | | Min | Max | |
|---|---|---|---|---|---|
| $t_{IRL}^\dagger$ | Shift In to Input Ready LOW | 1 | | 60 | ns |
| $t_{IRH}^\dagger$ | Shift In to Input Ready HIGH | 1 | | 60 | ns |
| $t_{ORL}^\dagger$ | Shift Out to Output Ready LOW | 4 | | 65 | ns |
| $t_{ORH}^\dagger$ | Shift Out to Output Ready HIGH | 4 | | 70 | ns |
| $t_{ODH}$ | Output Data Hold (previous word) | 4 | 10 | | ns |
| $t_{ODS}$ | Output Data Shift (next word) | 4 | | 65 | ns |
| $t_{PT}$ | Data throughput or "fall through" | 3, 6 | | 4 | µs |
| $t_{MRORL}$ | Master Reset to OR LOW | 8 | | 65 | ns |
| $t_{MRIRH}$ | Master Reset to IR HIGH | 8 | | 65 | ns |
| $t_{IPH}^*$ | Input Ready pulse HIGH | 3 | 20 | | ns |
| $t_{OPH}^*$ | Output Ready pulse HIGH | 6 | 20 | | ns |

† See AC test and high speed application note.

\* $t_{IPH}$ and $t_{OPH}$ are measured on initial characterization lots only and are not directly tested in production.

C57401/A     C57402/A     57401/A     57402/A

## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{cc}$ ............................................. −0.5 V to 7 V
Input voltage ............................................................. −1.5 V to 7 V
Off state output voltage .................................... −0.5 V to 5.5 V
Storage temperature ..................................... −65°C to +150°C

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## OPERATING CONDITIONS 57401A/2A

| Symbol | Parameter | Figure | Military | | | Unit |
| | | | Min | Typ | Max | |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $T_A$* | Operating temperature | | −55 | | 125 | °C |
| $t_{SIH}$† | Shift in HIGH time | 1 | 35 | | | ns |
| $t_{SIL}$ | Shift in LOW time | 1 | 35 | | | ns |
| $t_{IDS}$ | Input data setup | 1 | 5 | | | ns |
| $t_{IDH}$ | Input data hold time | 1 | 45 | | | ns |
| $f_{IN}$ | Shift in rate | 1 | 10 | | | MHz |
| $f_{OUT}$ | Shift Out rate | 4 | 10 | | | MHz |
| $t_{SOH}$† | Shift Out HIGH time | 4 | 35 | | | ns |
| $t_{SOL}$ | Shift Out LOW time | 4 | 35 | | | ns |
| $t_{MRW}$ | Master Reset pulse | 8 | 40 | | | ns |
| $t_{MRS}$** | Master Reset to SI | 8 | 45 | | | ns |

\* Instant-On Case Temperature
\*\* $t_{MRS}$ is measured on initial characterization lots only and is not directly tested in production.

## SWITCHING CHARACTERISTICS 57401A/2A Over Operating Conditions

| Symbol | Parameter | Figure | Military | | Unit |
| | | | Min | Max | |
|---|---|---|---|---|---|
| $t_{IRL}$† | Shift In to Input Ready LOW | 1 | | 50 | ns |
| $t_{IRH}$† | Shift In to Input Ready HIGH | 1 | | 50 | ns |
| $t_{ORL}$† | Shift Out to Output Ready LOW | 4 | | 65 | ns |
| $t_{ORH}$† | Shift Out to Output Ready HIGH | 4 | | 65 | ns |
| $t_{ODH}$ | Output Data Hold (previous word) | 4 | 10 | | ns |
| $t_{ODS}$ | Output Data Shift (next word) | 4 | | 60 | ns |
| $t_{PT}$ | Data throughput or "fall through" | 3, 6 | | 2.2 | μs |
| $t_{MRORL}$ | Master Reset to OR LOW | 8 | | 65 | ns |
| $t_{MRIRH}$ | Master Reset to IR HIGH | 8 | | 65 | ns |
| $t_{IPH}$ * | Input Ready pulse HIGH | 3 | 20 | | ns |
| $t_{OPH}$ * | Output Ready pulse HIGH | 6 | 20 | | ns |

† See AC test and high speed application note.
\* $t_{IPH}$ and $t_{OPH}$ are measured on initial characterization lots only and are not directly tested in production.

## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{cc}$ ............................................ −0.5 V to 7 V

Input voltage ........................................................ −1.5 V to 7 V

Off state output voltage .................................... −0.5 V to 5.5 V

Storage temperature ..................................... −65°C to +150°C

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## OPERATING CONDITIONS C57401/2

| Symbol | Parameter | Figure | Military | | | Unit |
| | | | Min | Typ | Max | |
|---|---|---|---|---|---|---|
| $V_{cc}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $T_A$* | Operating temperature | | −55 | | 125 | °C |
| $t_{SIH}$† | Shift in HIGH time | 1 | 45 | | | ns |
| $t_{SIL}$ | Shift in LOW time | 1 | 45 | | | ns |
| $t_{IDS}$ | Input data setup | 1 | 0 | | | ns |
| $t_{IDH}$ | Input data hold time | 1 | 55 | | | ns |
| $f_{IN}$ | Shift in rate | 1 | 7 | | | MHz |
| $f_{OUT}$ | Shift Out rate | 4 | 7 | | | MHz |
| $t_{SOH}$† | Shift Out HIGH time | 4 | 45 | | | ns |
| $t_{SOL}$ | Shift Out LOW time | 4 | 45 | | | ns |
| $t_{MRW}$ | Master Reset pulse† | 8 | 30 | | | ns |
| $t_{MRS}$** | Master Reset to SI | 8 | 45 | | | ns |

* Instant-On Case Temperature

** $t_{MRS}$ is measured on initial characterization lots only and is not directly tested in production.

## SWITCHING CHARACTERISTICS C57401/2 Over Operating Conditions

| Symbol | Parameter | Figure | Military | | Unit |
| | | | Min | Max | |
|---|---|---|---|---|---|
| $t_{IRL}$† | Shift In to Input Ready LOW | 1 | | 60 | ns |
| $t_{IRH}$† | Shift In to Input Ready HIGH | 1 | | 60 | ns |
| $t_{ORL}$† | Shift Out to Output Ready LOW | 4 | | 65 | ns |
| $t_{ORH}$† | Shift Out to Output Ready HIGH | 4 | | 70 | ns |
| $t_{ODH}$ | Output Data Hold (previous word) | 4 | 10 | | ns |
| $t_{ODS}$ | Output Data Shift (next word) | 4 | | 65 | ns |
| $t_{PT}$ | Data throughput or "fall through" | 3, 6 | | 4 | μs |
| $t_{MRORL}$ | Master Reset to OR LOW | 8 | | 65 | ns |
| $t_{MRIRH}$ | Master Reset to IR HIGH | 8 | | 65 | ns |
| $t_{IPH}$* | Input Ready pulse HIGH | 3 | 30 | | ns |
| $t_{OPH}$* | Output Ready pulse HIGH | 6 | 30 | | ns |

† See AC test and high speed application note.

* This parameter applies to FIFOs communicating with each other in a cascaded mode. $t_{IPH}$ and $t_{OPH}$ are measured on initial characterization lots only and are not directly tested in production.

## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ ............................................. −0.5 V to 7 V

Input voltage ........................................................ −1.5 V to 7 V

Off-state output voltage ..................................... −0.5 V to 5.5 V

Storage temperature ...................................... −65°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and a functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability. Absolute maximum ratings are for system design reference; parameters given are not tested.*

## OPERATING CONDITIONS C57401A/2A

| Symbol | Parameter | Figure | Military | | | Unit |
| | | | Min | Typ | Max | |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $T_A$* | Operating temperature | | −55 | | 125 | °C |
| $t_{SIH}$† | Shift in HIGH time | 1 | 35 | | | ns |
| $t_{SIL}$ | Shift in LOW time | 1 | 35 | | | ns |
| $t_{IDS}$ | Input data setup | 1 | 0 | | | ns |
| $t_{IDH}$ | Input data hold time | 1 | 45 | | | ns |
| $f_{IN}$ | Shift in rate | 1 | 10 | | | MHz |
| $f_{OUT}$ | Shift Out rate | 4 | 10 | | | MHz |
| $t_{SOH}$† | Shift Out HIGH time | 4 | 35 | | | ns |
| $t_{SOL}$ | Shift Out LOW time | 4 | 35 | | | ns |
| $t_{MRW}$ | Master Reset pulse | 8 | 40 | | | ns |
| $t_{MRS}$** | Master Reset to SI | 8 | 45 | | | ns |

\* Instant-On Case Temperature

\*\* $t_{MRS}$ is measured on initial characterization lots only and is not directly tested in production.

## SWITCHING CHARACTERISTICS C57401A/2A Over Operating Conditions

| Symbol | Parameter | Figure | Military | | Unit |
| | | | Min | Max | |
|---|---|---|---|---|---|
| $t_{IRL}$† | Shift In to Input Ready LOW | 1 | | 50 | ns |
| $t_{IRH}$† | Shift In to Input Ready HIGH | 1 | | 50 | ns |
| $t_{ORL}$† | Shift Out to Output Ready LOW | 4 | | 65 | ns |
| $t_{ORH}$† | Shift Out to Output Ready HIGH | 4 | | 65 | ns |
| $t_{ODH}$ | Output Data Hold (previous word) | 4 | 10 | | ns |
| $t_{ODS}$ | Output Data Shift (next word) | 4 | | 60 | ns |
| $t_{PT}$ | Data throughput or "fall through" | 3, 6 | | 2.2 | µs |
| $t_{MRORL}$ | Master Reset to OR LOW | 8 | | 65 | ns |
| $t_{MRIRH}$ | Master Reset to IR HIGH | 8 | | 65 | ns |
| $t_{IPH}$* | Input Ready pulse HIGH | 3 | 30 | | ns |
| $t_{OPH}$* | Output Ready pulse HIGH | 6 | 30 | | ns |

† See AC test and high speed application note.

\* This parameter applies to FIFOs communicating with each other in a cascaded mode. $t_{IPH}$ and $t_{OPH}$ are measured on initial characterization lots only and are not directly tested in production.

## TEST LOAD FOR ALL DEVICES

Input pulse 0 to 3 V.
Input Rise and Fall Time (10%–90%).
5 ns minimum.
Measurements made at 1.5 V.

5 V

560 Ω

⊙ TEST POINT *

1.1 KΩ    30 pF
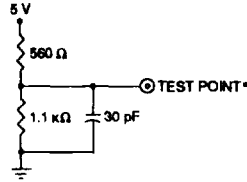
505 133

\* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

## DC CHARACTERISTICS Over Operating Conditions For all Devices

| Symbol | Parameter | | Test Conditions | | Min | Typ | Max | Unit |
|--------|-----------|--|-----------------|--|-----|-----|-----|------|
| $V_{IL}$ | Low-level input voltage | | | | | | $0.8^\dagger$ | V |
| $V_{IH}$ | High-level input voltage | | | | $2^\dagger$ | | | V |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$ – MIN | $I_I = -18$ mA | | | –1.5 | V |
| $I_{IL1}$ | Low-level input current | $D_0$–$D_n$, $\overline{MR}$ | $V_{CC}$ – MAX | $V_I = 0.45$ V | | | –0.8 | mA |
| $I_{IL2}$ | | SI, SO | | | | | –1.6 | mA |
| $I_{IH}$ | High-level input current | | $V_{CC}$ – MAX | $V_I = 2.4$ V | | | 50 | μA |
| $I_I$ | Maximum input current | | $V_{CC}$ – MAX | $V_I = 5.5$ V | | | 1 | mA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ – MIN | $I_{OL} = 8$ mA | | | 0.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ – MIN | $I_{OH} = -0.9$ mA | 2.4 | | | V |
| $I_{OS}$ | Output short-circuit current* | | $V_{CC}$ – MAX | $V_O = 0$ V | –20 | | –90 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ – MAX     Inputs low, outputs open. | 57401 | | | 160 | mA |
| | | | | 57401A | | | 180 | |
| | | | | 57402 | | | 180 | |
| | | | | 57402A | | | 200 | |
| | | | | C57401 | | | 160 | |
| | | | | C57401A | | | 180 | |
| | | | | C57402 | | | 180 | |
| | | | | C57402A | | | 200 | |

\* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† $V_{IL}$ and $V_{IH}$ are input conditions of output tests and are not themselves directly tested. $V_{IL}$ and $V_{IH}$ are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

## FUNCTIONAL DESCRIPTION

### Data Input

After power up the Master Reset is pulsed low (Fig 8) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the $D_x$ inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought low. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a Shift-Out is applied. If the memory is full, IR will remain LOW.

### Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. $t_{PT}$ defines the time required for the first data to travel from input to the output of a previously empty device.

### Data Output

Data is read from the $O_x$ outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage.

When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and $O_x$ remains as before (i.e. data does not change if FIFO is empty). Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least $t_{PT}$) or completely empty (Output Ready stays LOW for at least $t_{PT}$).

### AC Test and High Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between $V_{CC}$ and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e. rising edge of the Shift-In pulse is not recognized until Input-Ready is HIGH. If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time ($t_{IDH}$) and the next activity of the Input Ready ($t_{IRL}$) to be extended relative to Shift In going High. This same type of problem is also related to $t_{IRH}$, $t_{ORL}$ and $t_{ORH}$ as related to Shift-Out.
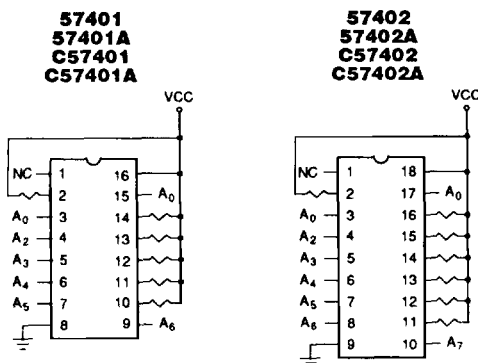
## LIFE TEST/ BURN-IN CIRCUITS

### Military Burn-In

### Dynamic Burn-In Circuitry



57401
57401A
C57401
C57401A

57402
57402A
C57402
C57402A

$T_{ambient}$ = 125°C
$V_{CC}$ = 5.25 ± 0.25 V
Square wave pulses on $A_0$ to $A_8$ are:
1. 50% ± 15% duty cycle
2. Logic "0" = −1 V to 0.7 V
3. Logic "1" = 2.4 V to $V_{CC}$
4. Frequency of each address is to be one-half of each preceding input, with $A_0$ beginning at 100 kHZ.

e.g., $A_0$ = 100 kHz
$A_1$ = 50 kHz ± 10%
$A_2$ = 25 kHz ± 10%
$A_n$ = 1/2 $A_{n-1}$ ± 10%, etc.
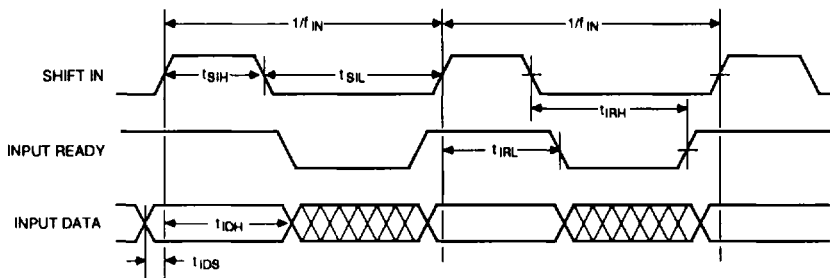
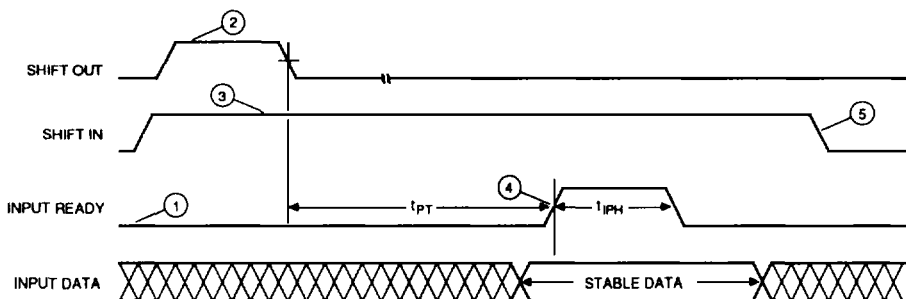**Figure 1. Input Timing**
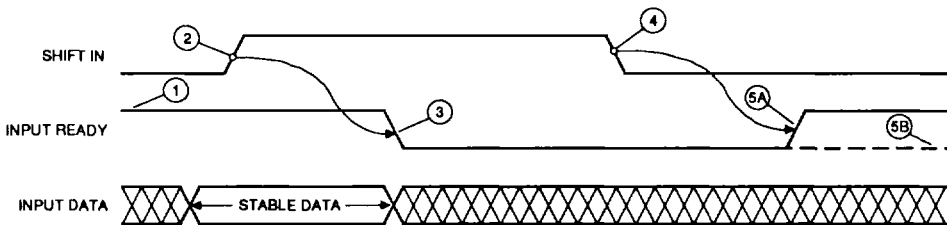


1. Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
2. Input Data is loaded into the first word.
3. Input Ready goes LOW indicating the first word is full.
4. The Data from the first word is released for "fall-through" to second word.
5. The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.
5B. If the second word is already full then the Data remains at the first word. Since the FIFO is now full InputReady remains low.
   Note: Shift in pulses applied while input Ready is LOW will be ignored (See Figure 3).

**Figure 2. The Mechanism of Shifting Data into the FIFO**



1. FIFO is initially full.
2. Shift Out pulse is applied. An empty location starts "bubbling" to the front.
3. Shift in is held HIGH.
4. As soon as Input Ready becomes HIGH the input Data is loaded into the first word.
5. The Data from the first word is released for "fall through" to second word.

**Figure 3. Data is Shifted in Whenever Shift in and Input Ready Are Both HIGH**
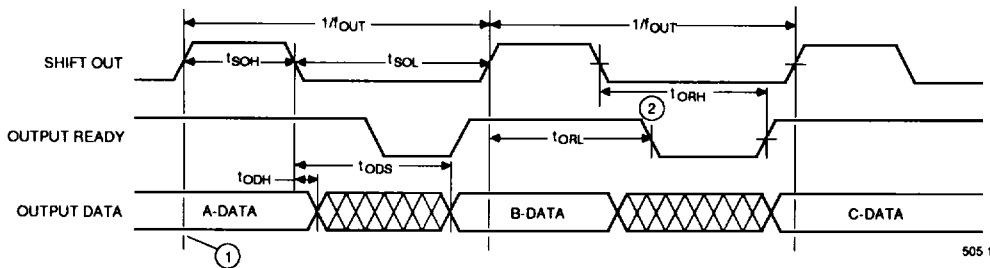
1. The diagram assumes that at this time words 63, 62, 61 are loaded with A, B, C Data, respectively.
2. Data is shifted out when Shift Out makes a HIGH to LOW transition.

**Figure 4. Output Timing**
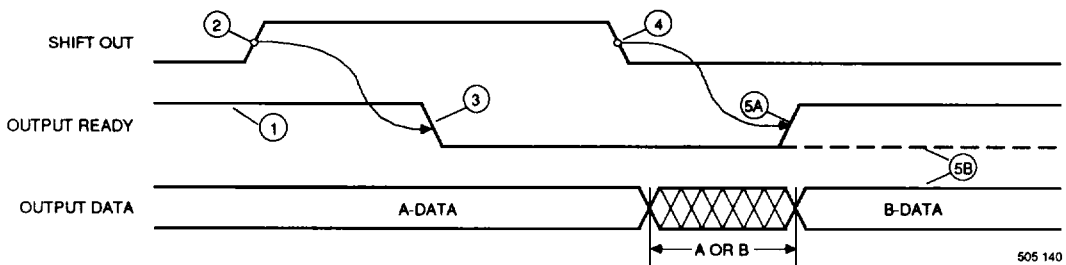


1. Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
2. Shift-Out goes HIGH causing the next step.
3. Output ready goes LOW.
4. Contents of word 62 (B-DATA) is released for "fall-through" to word 63.
5A. Output ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
5B. If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.
    Note: Shift Out pulses applied when Output Ready is LOW will be ignored (Figure 7).
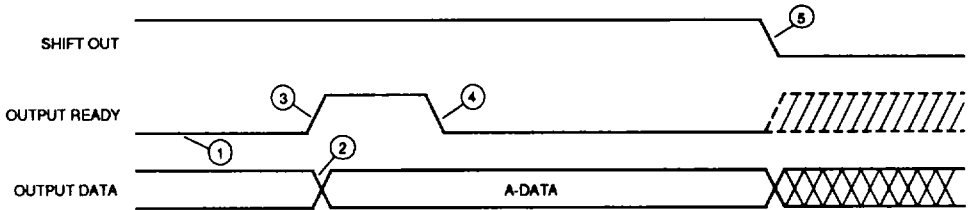
**Figure 5. The Mechanism of Shifting Data Out of the FIFO**
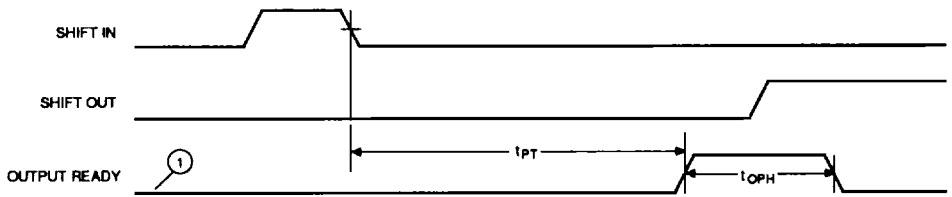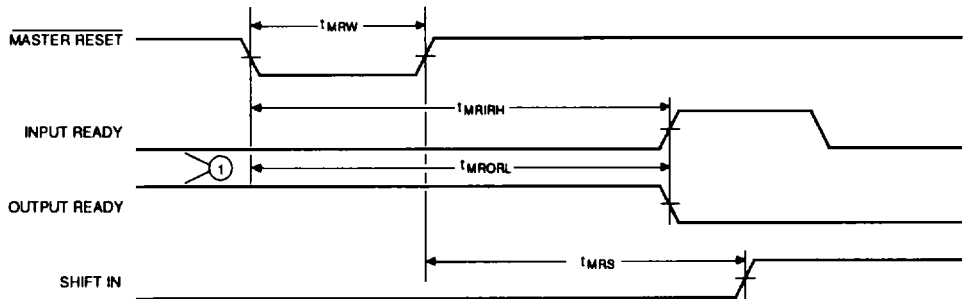
1. FIFO initially empty.

**Figure 6. $t_{PT}$ and $t_{OPH}$ Specification**



1. Word 63 is empty.
2. New data (A) arrives at the outputs (word 63).
3. Output Ready goes HIGH indicating arrival of new data.
4. Since Shift Out is held HIGH. Output Ready goes immediately LOW.
5. As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.
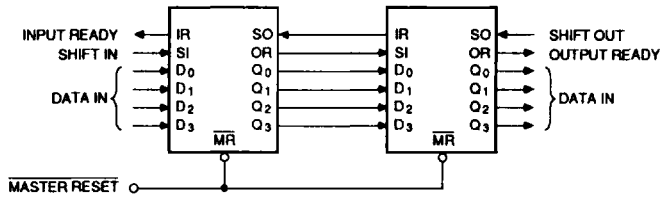
**Figure 7. Data Is Shifted Out Whenever Shift Out and Output Ready Are Both HIGH**
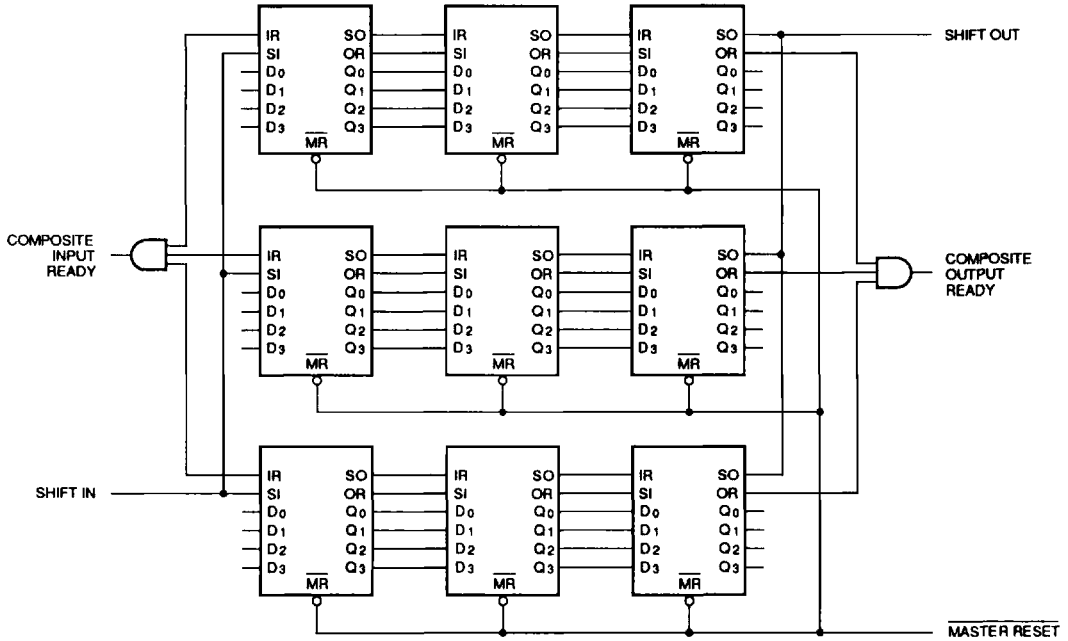


1. FIFO initially full.

**Figure 8. Master Reset Timing**

**Figure 9. Cascading FIFOs to Form 128X4 FIFO with C57401/A**

Cascadable FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.



**Figure 10. 192X12 FIFO with C57401/A**      505 145

Cascadable FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall-through times of the FIFOs.