

FEATURES

6.5 Ω (maximum) on resistance
0.8 Ω (maximum) on-resistance flatness
2.7 V to 5.5 V single supply
 ± 2.7 V to ± 5.5 V dual supply
Rail-to-rail operation
8-lead SOT-23, 8-lead MSOP
Typical power consumption (<0.1 μ W)
TTL-/CMOS-compatible inputs

APPLICATIONS

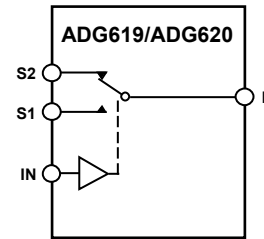
Automatic test equipment
Power routing
Communication systems
Data acquisition systems
Sample-and-hold systems
Avionics
Relay replacement
Battery-powered systems

GENERAL DESCRIPTION

The ADG619/ADG620 are monolithic, CMOS single-pole double-throw (SPDT) switches. Each switch conducts equally well in both directions when the device is on.

The ADG619/ADG620 offer a low on resistance of 4 Ω , which is matched to within 0.7 Ω between channels. These switches also provide low power dissipation, yet result in high switching speeds. The ADG619 exhibits break-before-make switching action, thus preventing momentary shorting when switching channels. The ADG620 exhibits make-before-break action.

The ADG619/ADG620 are available in an 8-lead SOT-23 and an 8-lead MSOP.

FUNCTIONAL BLOCK DIAGRAM


NOTES
1. SWITCHES SHOWN FOR A LOGIC 1 INPUT.

Figure 1.

02617-001

PRODUCT HIGHLIGHTS

1. Low on resistance (R_{ON}): 4 Ω typical.
2. Dual ± 2.7 V to ± 5.5 V or single 2.7 V to 5.5 V supplies.
3. Low power dissipation.
4. Fast t_{ON}/t_{OFF} .
5. Tiny, 8-lead SOT-23 and 8-lead MSOP.

Table 1. Truth Table for the ADG619/ADG620

| IN | Switch S1 | Switch S2 |
|----|-----------|-----------|
| 0 | On | Off |
| 1 | Off | On |

Rev. C

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REVISION HISTORY

| | |
|---|----|
| 3/07—Rev. B to Rev. C | |
| Changes to Specifications | 3 |
| 1/06—Rev. A to Rev. B | |
| Changes to R_{ON} Values in Table 2 | 2 |
| Updated Outline Dimensions | 13 |
| Changes to Ordering Guide | 13 |
| 6/03—Rev. 0 to Rev. A. | |
| Edits to Specifications | 2 |
| Changes to Ordering Guide | 4 |
| Updated Outline Dimensions | 8 |

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications -40°C to $+85^\circ\text{C}$, unless otherwise noted.

Table 2.

| Parameter | B Version ¹ | | Unit | Test Conditions/Comments |
|---|------------------------|----------------------|-------------------|---|
| | +25°C | -40°C to +85°C | | |
| ANALOG SWITCH | | | | |
| Analog Signal Range | | V_{SS} to V_{DD} | V | $V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$ |
| On Resistance (R_{ON}) | 4 | | Ω typ | $V_S = \pm 4.5\text{ V}$, $I_{DS} = -10\text{ mA}$; see Figure 15 |
| | 6.5 | 8.5 | Ω max | |
| R_{ON} Match Between Channels (ΔR_{ON}) | 0.7 | | Ω typ | $V_S = \pm 4.5\text{ V}$, $I_{DS} = -10\text{ mA}$ |
| | 1.1 | 1.35 | Ω max | |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 0.7 | 0.8 | Ω typ | $V_S = \pm 3.3\text{ V}$, $I_{DS} = -10\text{ mA}$ |
| | 1.35 | 1.4 | Ω max | |
| LEAKAGE CURRENTS | | | | |
| Source Off Leakage, I_S (Off) | ± 0.01 | | nA typ | $V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ |
| | ± 0.25 | ± 1 | nA max | $V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$; see Figure 16 |
| Channel On Leakage, I_D , I_S (On) | ± 0.01 | | nA typ | $V_S = V_D = \pm 4.5\text{ V}$; see Figure 17 |
| | ± 0.25 | ± 1 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.005 | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 2 | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | |
| ADG619 | | | | |
| t_{ON} | 80 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 120 | 155 | ns max | $V_S = 3.3\text{ V}$; see Figure 18 |
| t_{OFF} | 45 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 75 | 90 | ns max | $V_S = 3.3\text{ V}$; see Figure 18 |
| Break-Before-Make Time Delay, t_{BBM} | 40 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | 10 | ns min | $V_{S1} = V_{S2} = 3.3\text{ V}$; see Figure 19 |
| ADG620 | | | | |
| t_{ON} | 40 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 65 | 85 | ns max | $V_S = 3.3\text{ V}$; see Figure 18 |
| t_{OFF} | 200 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 330 | 400 | ns max | $V_S = 3.3\text{ V}$; see Figure 18 |
| Make-Before-Break Time Delay, t_{MBS} | 160 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | 10 | ns min | $V_S = 0\text{ V}$; see Figure 20 |
| Charge Injection | 110 | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 21 |
| Off Isolation | -67 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 22 |
| Channel-to-Channel Crosstalk | -67 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 23 |
| Bandwidth -3 dB | 190 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 24 |
| C_S (Off) | 25 | | pF typ | $f = 1\text{ MHz}$ |
| C_D , C_S (On) | 95 | | pF typ | $f = 1\text{ MHz}$ |

ADG619/ADG620

| Parameter | B Version ¹ | | Unit | Test Conditions/Comments |
|--------------------|------------------------|----------------|--|---|
| | +25°C | −40°C to +85°C | | |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.001 | 1.0 | $\mu\text{A typ}$ $\mu\text{A max}$ | $V_{DD} = +5.5\text{ V}, V_{SS} = -5.5\text{ V}$ Digital inputs = 0 V or 5.5 V |
| I_{SS} | 0.001 | 1.0 | $\mu\text{A typ}$ $\mu\text{A max}$ | Digital inputs = 0 V or 5.5 V |

¹ Temperature range for B version is −40°C to +85°C.

² Guaranteed by design, not subject to production test.

SINGLE SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$. All specifications -40°C to $+85^{\circ}\text{C}$, unless otherwise noted.

Table 3.

| Parameter | B Version ¹ | | Unit | Test Conditions/Comments |
|---|------------------------|-----------------|-------------------|---|
| | +25°C | -40°C to +85°C | | |
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 V to V_{DD} | V | $V_{DD} = 4.5\text{ V}$, $V_{SS} = 0\text{ V}$ |
| On Resistance (R_{ON}) | 7 | | Ω typ | $V_S = 0\text{ V}$ to 4.5 V , $I_{DS} = -10\text{ mA}$; see Figure 15 |
| | 10 | 12.5 | Ω max | |
| R_{ON} Match Between Channels (ΔR_{ON}) | 0.8 | | Ω typ | $V_S = 0\text{ V}$ to 4.5 V , $I_{DS} = -10\text{ mA}$ |
| | 1.1 | 1.3 | Ω max | |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 0.5 | 0.5 | Ω typ | $V_S = 1.5\text{ V}$ to 3.3 V , $I_{DS} = -10\text{ mA}$ |
| | | 1.2 | Ω max | |
| LEAKAGE CURRENTS | | | | |
| Source Off Leakage, I_S (Off) | ± 0.01 | | nA typ | $V_{DD} = 5.5\text{ V}$ |
| | ± 0.25 | ± 1 | nA max | $V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$; see Figure 16 |
| Channel On Leakage, I_D , I_S (On) | ± 0.01 | | nA typ | $V_S = V_D = 1\text{ V}/4.5\text{ V}$; see Figure 17 |
| | ± 0.25 | ± 1 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.005 | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 2 | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | |
| ADG619 | | | | |
| t_{ON} | 120 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 220 | 280 | ns max | $V_S = 3.3\text{ V}$; see Figure 18 |
| t_{OFF} | 50 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 75 | 110 | ns max | $V_S = 3.3\text{ V}$; see Figure 18 |
| Break-Before-Make Time Delay, t_{BBM} | 70 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | 10 | ns min | $V_{S1} = V_{S2} = 3.3\text{ V}$; see Figure 19 |
| ADG620 | | | | |
| t_{ON} | 50 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 85 | 110 | ns max | $V_S = 3.3\text{ V}$; see Figure 18 |
| t_{OFF} | 210 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 340 | 420 | ns max | $V_S = 3.3\text{ V}$; see Figure 18 |
| Make-Before-Break Time Delay, t_{MBB} | 170 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | 10 | ns min | $V_S = 3.3\text{ V}$; see Figure 20 |
| Charge Injection | 6 | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 21 |
| Off Isolation | -67 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 22 |
| Channel-to-Channel Crosstalk | -67 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 23 |
| Bandwidth -3 dB | 190 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 24 |
| C_S (OFF) | 25 | | pF typ | $f = 1\text{ MHz}$ |
| C_D , C_S (ON) | 95 | | pF typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.001 | | μA typ | $V_{DD} = 5.5\text{ V}$ |
| | | 1.0 | μA max | Digital inputs = 0 V or 5.5 V |

¹ Temperature range for B version is -40°C to $+85^{\circ}\text{C}$.

² Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

| Parameter | Rating |
|---|--|
| V _{DD} to V _{SS} | 13 V |
| V _{DD} to GND | −0.3 V to +6.5 V |
| V _{SS} to GND | +0.3 V to −6.5 V |
| Analog Inputs ¹ | V _{SS} − 0.3 V to V _{DD} + 0.3 V |
| Digital Inputs ¹ | −0.3 V to V _{DD} + 0.3 V or 30 mA (whichever occurs first) |
| Peak Current, S or D | 100 mA (pulsed at 1 ms, 10% duty cycle maximum) |
| Continuous Current, S or D | 50 mA |
| Operating Temperature Range Industrial (B Version) | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| MSOP | |
| θ _{JA} Thermal Impedance | 206°C/W |
| θ _{JC} Thermal Impedance | 44°C/W |
| SOT-23 | |
| θ _{JA} Thermal Impedance | 229.6°C/W |
| θ _{JC} Thermal Impedance | 91.99°C/W |
| Lead Temperature, Soldering (10 sec) | 300°C |
| IR Reflow, Peak Temperature | 220°C |

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at a time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

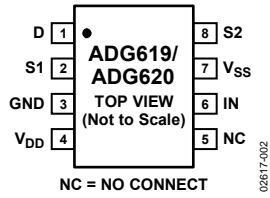


Figure 2. 8-Lead SOT-23 (RJ-8)

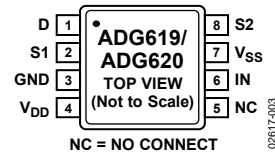


Figure 3. 8-Lead MSOP (RM-8)

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-----------------|---|
| 1 | D | Drain Terminal. Can be an input or output. |
| 2 | S1 | Source Terminal. Can be an input or output. |
| 3 | GND | Ground (0 V) Reference. |
| 4 | V _{DD} | Most Positive Power Supply. |
| 5 | NC | No Connect. Not internally connected. |
| 6 | IN | Logic Control Input. |
| 7 | V _{SS} | Most Negative Power Supply. This pin is only used in dual-supply applications and should be tied to ground in single-supply applications. |
| 8 | S2 | Source Terminal. Can be an input or output. |

TYPICAL PERFORMANCE CHARACTERISTICS

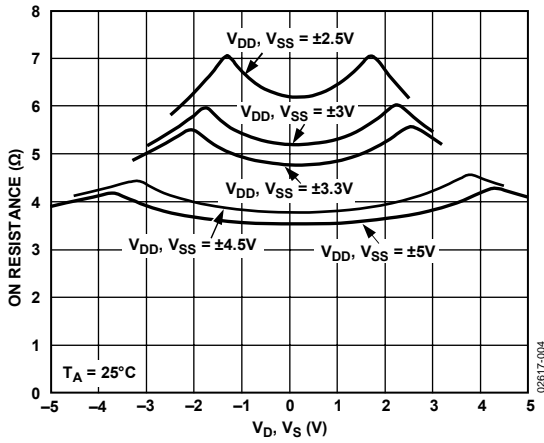


Figure 4. On Resistance vs. V_D, V_S (Dual Supply)

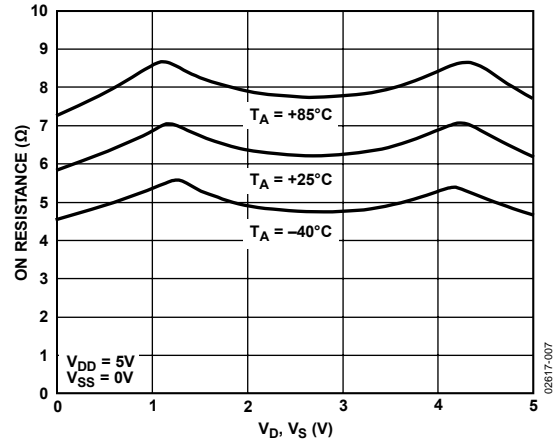


Figure 7. On Resistance vs. V_D, V_S for Different Temperatures (Single Supply)

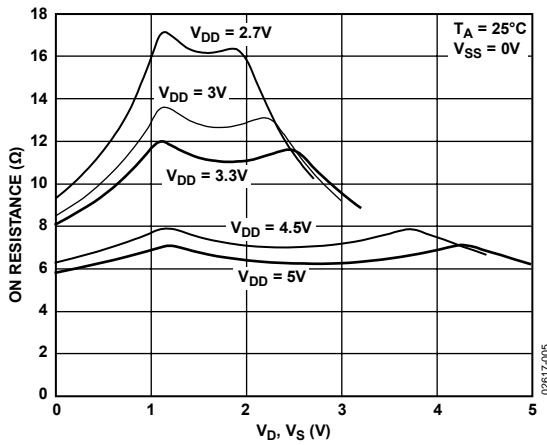


Figure 5. On Resistance vs. V_D, V_S (Single Supply)

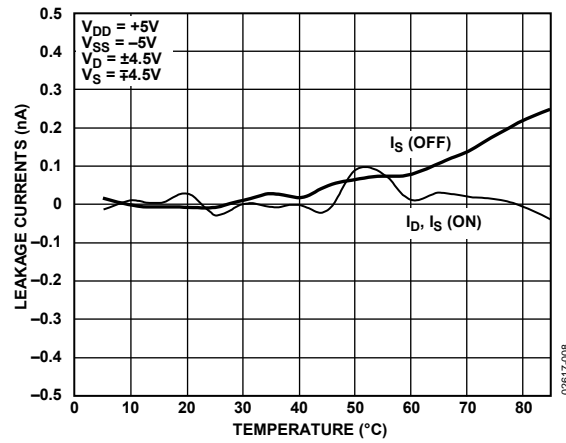


Figure 8. Leakage Currents vs. Temperature (Dual Supply)

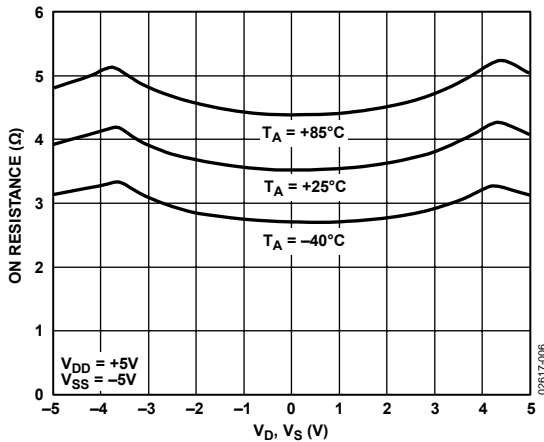


Figure 6. On Resistance vs. V_D, V_S for Different Temperatures (Dual Supply)

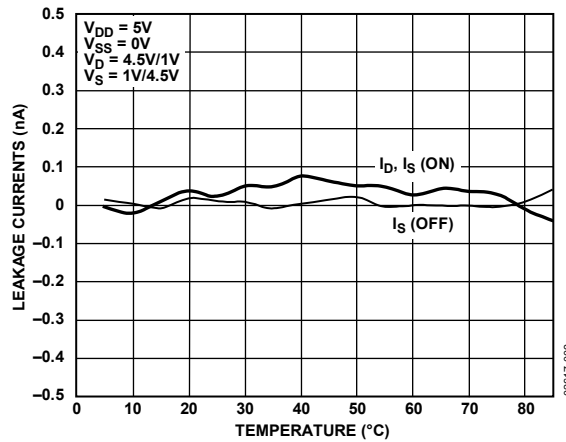


Figure 9. Leakage Currents vs. Temperature (Single Supply)



Figure 10. Charge Injection vs. Source Voltage

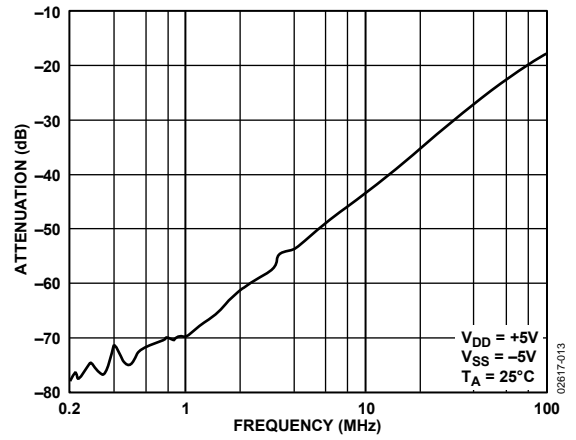


Figure 13. Crosstalk vs. Frequency



Figure 11. t_{ON}/t_{OFF} Times vs. Temperatures



Figure 14. On Response vs. Frequency

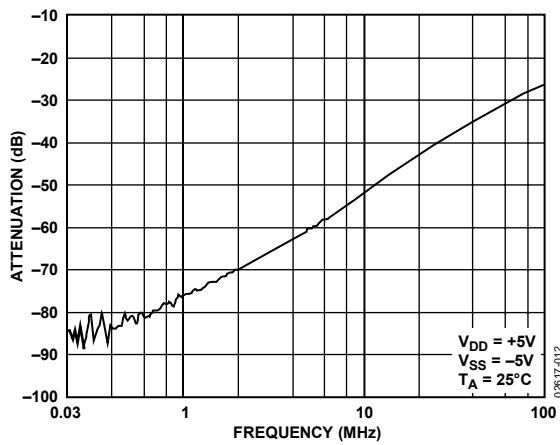


Figure 12. Off Isolation vs. Frequency

TERMINOLOGY

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

R_{ON}
Ohmic resistance between D and S terminals.

ΔR_{ON}
On resistance match between any two channels.

R_{FLAT (ON)}
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_{S (Off)}
Source leakage current with the switch off.

I_D, I_{S (On)}
Channel leakage current with the switch on.

V_D, V_S
Analog voltage on Terminal D and Terminal S.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL}, I_{INH}
Input current of the digital input.

C_{S (Off)}
Off switch source capacitance.

C_D, C_{S (On)}
On switch capacitance.

t_{ON}
Delay between applying the digital control input and the output switching on.

t_{OFF}
Delay between applying the digital control input and the output switching off.

t_{MBB}
On time is measured between the 80% points of both switches, when switching from one address state to another.

t_{BBM}
Off time or on time is measured between the 90% points of both switches, when switching from one address state to another.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk
A measure of unwanted signal coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Bandwidth
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

TEST CIRCUITS

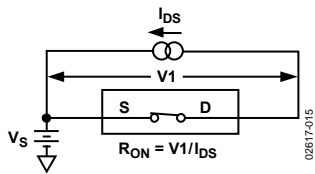


Figure 15. On Resistance



Figure 16. Off Leakage

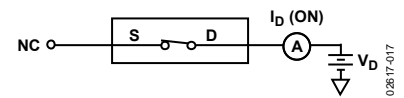


Figure 17. On Leakage

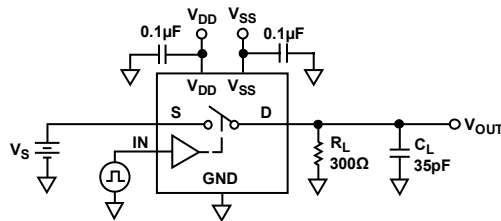


Figure 18. Switching Times

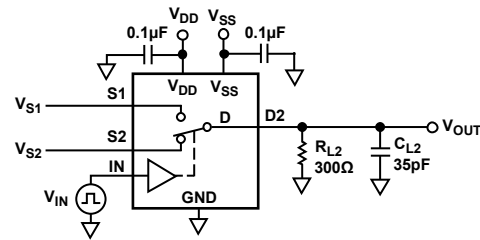
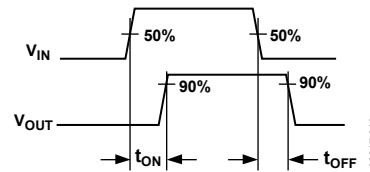


Figure 19. Break-Before-Make Time Delay, t_{BBM} (ADG619 Only)

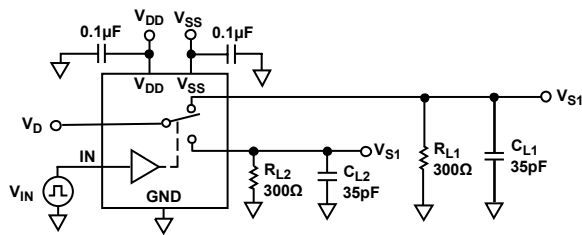


Figure 20. Make-Before-Break Time Delay, t_{MBB} (ADG620 Only)

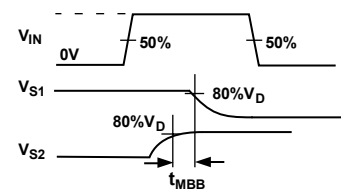


Figure 21. Charge Injection



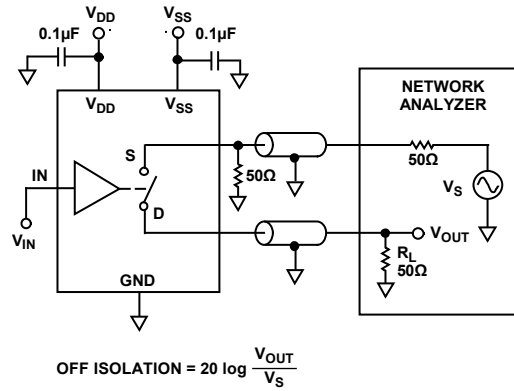


Figure 22. Off Isolation

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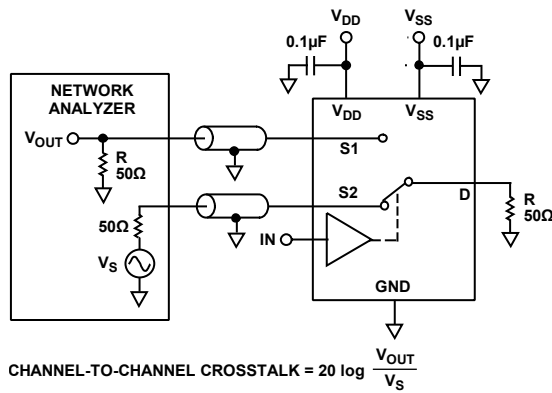


Figure 23. Channel-to-Channel Crosstalk

02817-023

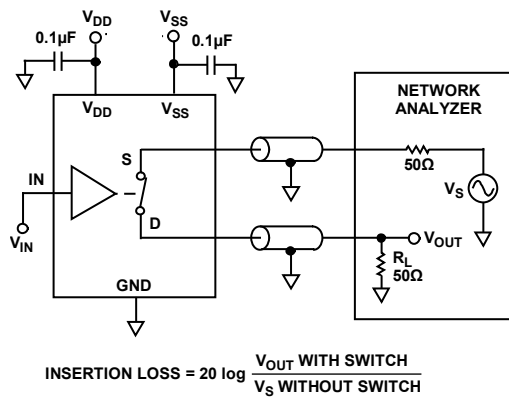


Figure 24. Bandwidth

02817-024

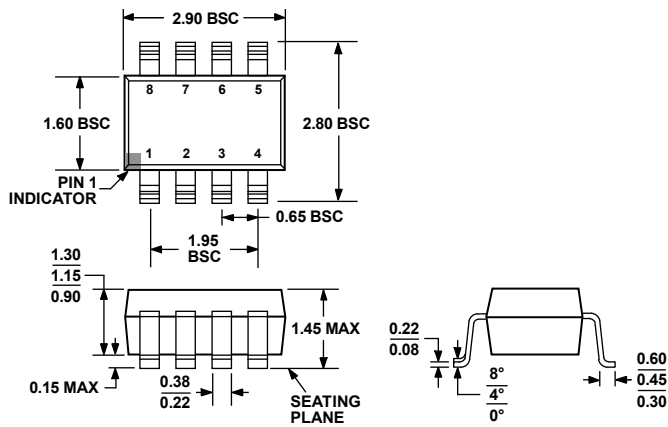
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 25. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178-BA

Figure 26. 8-Lead Small Outline Transistor Package [SOT-23] (RJ-8)

Dimensions shown in millimeters

ADG619/ADG620

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding ¹ |
|--------------------------------|-------------------|--|----------------|-----------------------|
| ADG619BRM | -40°C to +85°C | 8-Lead Mini Small Outline Package (MSOP) | RM-8 | SVB |
| ADG619BRM-REEL | -40°C to +85°C | 8-Lead Mini Small Outline Package (MSOP) | RM-8 | SVB |
| ADG619BRM-REEL7 | -40°C to +85°C | 8-Lead Mini Small Outline Package (MSOP) | RM-8 | SVB |
| ADG619BRMZ ² | -40°C to +85°C | 8-Lead Mini Small Outline Package (MSOP) | RM-8 | SCC |
| ADG619BRMZ-REEL ² | -40°C to +85°C | 8-Lead Mini Small Outline Package (MSOP) | RM-8 | SCC |
| ADG619BRMZ-REEL7 ² | -40°C to +85°C | 8-Lead Mini Small Outline Package (MSOP) | RM-8 | SCC |
| ADG619BRT-REEL | -40°C to +85°C | 8-Lead Small Outline Transistor Package (SOT-23) | RJ-8 | SVB |
| ADG619BRT-REEL7 | -40°C to +85°C | 8-Lead Small Outline Transistor Package (SOT-23) | RJ-8 | SVB |
| ADG619BRT-500RL7 | -40°C to +85°C | 8-Lead Small Outline Transistor Package (SOT-23) | RJ-8 | SVB |
| ADG619BRTZ-REEL ² | -40°C to +85°C | 8-Lead Small Outline Transistor Package (SOT-23) | RJ-8 | SCC |
| ADG619BRTZ-REEL7 ² | -40°C to +85°C | 8-Lead Small Outline Transistor Package (SOT-23) | RJ-8 | SCC |
| ADG619BRTZ-500RL7 ² | -40°C to +85°C | 8-Lead Small Outline Transistor Package (SOT-23) | RJ-8 | SCC |
| ADG620BRM | -40°C to +85°C | 8-Lead Mini Small Outline Package (MSOP) | RM-8 | SWB |
| ADG620BRM-REEL | -40°C to +85°C | 8-Lead Mini Small Outline Package (MSOP) | RM-8 | SWB |
| ADG620BRM-REEL7 | -40°C to +85°C | 8-Lead Mini Small Outline Package (MSOP) | RM-8 | SWB |
| ADG620BRMZ ² | -40°C to +85°C | 8-Lead Mini Small Outline Package (MSOP) | RM-8 | S21 |
| ADG620BRT-REEL | -40°C to +85°C | 8-Lead Small Outline Transistor Package (SOT-23) | RJ-8 | SWB |
| ADG620BRT-REEL7 | -40°C to +85°C | 8-Lead Small Outline Transistor Package (SOT-23) | RJ-8 | SWB |
| ADG620BRTZ-REEL7 ² | -40°C to +85°C | 8-Lead Small Outline Transistor Package (SOT-23) | RJ-8 | S21 |

¹ Branding on SOT-23 and MSOP is limited to three characters due to space constraints.

² Z = RoHS Compliant Part.

NOTES

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