

FEATURES

44 V supply maximum ratings
V_{SS} to V_{DD} analog signal range
Low on resistance: <35 Ω
Ultralow power dissipation: <35 μW
Fast transition time: 145 ns maximum
Break-before-make switching action
Plug-in replacement for DG419
Supports defense and aerospace applications
(AQEC standard)
Military temperature range: -55°C to +125°C
Controlled manufacturing baseline
One assembly/test site
One fabrication site
Enhanced product change notification
Qualification data available on request

APPLICATIONS

Precision test equipment
Precision instrumentation
Battery-powered systems
Sample-and-hold systems

GENERAL DESCRIPTION

The ADG419-EP is a monolithic CMOS SPDT switch. This switch is fabricated on an enhanced LC²MOS process that provides low power dissipation yet gives high switching speed, low on resistance, and low leakage current.

The on resistance profile of the ADG419-EP is very flat over the full analog input range, ensuring excellent linearity and low distortion. The part also exhibits high switching speed and high signal bandwidth. CMOS construction ensures ultralow power dissipation, making the part ideally suited for portable and battery-powered instruments.

Each switch of the ADG419-EP conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. The ADG419-EP exhibits break-before-make switching action.

Full details about this enhanced product are available in the [ADG419](#) data sheet, which should be consulted in conjunction with this data sheet.

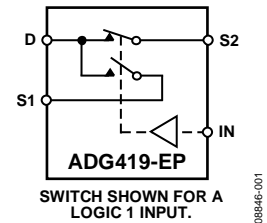
FUNCTIONAL BLOCK DIAGRAM

Figure 1.

PRODUCT HIGHLIGHTS

1. **Extended Signal Range.**
The ADG419-EP is fabricated on an enhanced LC²MOS process, giving an increased signal range that extends to the supply rails.
2. **Ultralow Power Dissipation.**
3. **Low R_{ON}.**
4. **Single-Supply Operation.**
For applications where the analog signal is unipolar, the ADG419-EP can be operated from a single rail power supply. The part is fully specified with a single 12 V power supply and remains functional with single supplies as low as 5 V.

Rev. 0

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REVISION HISTORY

7/10—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $V_L = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

| Parameter | +25°C | -40°C to +85°C | -55°C to +125°C | Unit | Test Conditions/Comments |
|--|-------------------------|--------------------------|--------------------------|--|--|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | V_{SS} to V_{DD} | V | |
| R_{ON} | 25 35 | 45 | 45 | Ω typ Ω max | $V_D = \pm 12.5\text{ V}$, $I_S = -10\text{ mA}$; see Figure 9 $V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$; see Figure 9 |
| LEAKAGE CURRENT | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.1 ± 0.25 | ± 5 | ± 15 | nA typ nA max | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ $V_D = \pm 15.5\text{ V}$, $V_S = \mp 15.5\text{ V}$; see Figure 10 |
| Drain Off Leakage, I_D (Off) | ± 0.1 ± 0.75 | ± 5 | ± 30 | nA typ nA max | $V_D = \pm 15.5\text{ V}$, $V_S = \mp 15.5\text{ V}$; see Figure 10 |
| Channel On Leakage, I_D , I_S (On) | ± 0.4 ± 0.75 | ± 5 | ± 30 | nA typ nA max | $V_S = V_D = \pm 15.5\text{ V}$; see Figure 11 |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | 2.4 | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | | ± 0.005 ± 0.5 | ± 0.005 ± 0.5 | μA typ μA max | $V_{IN} = V_{INL}$ or V_{INH} |
| DYNAMIC CHARACTERISTICS¹ | | | | | |
| $t_{TRANSITION}$ | 145 | 200 | 200 | ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_{S1} = \pm 10\text{ V}$, $V_{S2} = \mp 10\text{ V}$; see Figure 12 |
| Break-Before-Make Time Delay, t_D | 30 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_{S1} = V_{S2} = \pm 10\text{ V}$; see Figure 13 |
| Off Isolation | 5 80 | | | ns min dB typ | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$; see Figure 14 |
| Channel-to-Channel Crosstalk | 90 | | | dB typ | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$; see Figure 15 |
| C_S (Off) | 6 | | | pF typ | $f = 1\text{ MHz}$ |
| C_D , C_S (On) | 55 | | | pF typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 0.0001 1 | 2.5 | 2.5 | μA typ μA max | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ $V_{IN} = 0\text{ V}$ or 5 V |
| I_{SS} | 0.0001 1 | 2.5 | 2.5 | μA typ μA max | |
| I_L | 0.0001 1 | 2.5 | 2.5 | μA typ μA max | $V_L = 5.5\text{ V}$ |

¹ Guaranteed by design; not subject to production test.

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SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $V_L = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

| Parameter | +25°C | -40°C to +85°C | -55°C to +125°C | Unit | Test Conditions/Comments |
|--|------------|-------------------|--------------------|------------------------------|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 to V_{DD} | V | |
| R_{ON} | 40 | 60 | 70 | Ω typ Ω max | $V_D = 3\text{ V}, 8.5\text{ V}, I_S = -10\text{ mA}$; see Figure 9 $V_{DD} = 10.8\text{ V}$; see Figure 9 |
| LEAKAGE CURRENT | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.1 | | | nA typ | $V_{DD} = 13.2\text{ V}$ $V_D = 12.2\text{ V}/1\text{ V}, V_S = 1\text{ V}/12.2\text{ V}$; see Figure 10 |
| Drain Off Leakage, I_D (Off) | ± 0.25 | ± 5 | ± 15 | nA max | |
| Channel On Leakage, I_D, I_S (On) | ± 0.1 | | | nA typ | $V_D = 12.2\text{ V}/1\text{ V}, V_S = 1\text{ V}/12.2\text{ V}$; see Figure 10 |
| | ± 0.75 | ± 5 | ± 30 | nA max | |
| | ± 0.4 | | | nA typ | $V_S = V_D = 12.2\text{ V}/1\text{ V}$; see Figure 11 |
| | ± 0.75 | ± 5 | ± 30 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | 2.4 | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | | ± 0.005 | ± 0.005 | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | ± 0.5 | ± 0.5 | μA max | |
| DYNAMIC CHARACTERISTICS¹ | | | | | |
| $t_{TRANSITION}$ | 170 | 250 | 250 | ns max | $R_L = 300\ \Omega, C_L = 35\text{ pF}; V_{S1} = 0\text{ V}/8\text{ V}, V_{S2} = 8\text{ V}/0\text{ V}$; see Figure 12 |
| Break-Before-Make Time Delay, t_D | 60 | | | ns typ | $R_L = 300\ \Omega, C_L = 35\text{ pF}; V_{S1} = V_{S2} = 8\text{ V}$; see Figure 13 |
| Off Isolation | 80 | | | dB typ | $R_L = 50\ \Omega, f = 1\text{ MHz}$; see Figure 14 |
| Channel-to-Channel Crosstalk | 70 | | | dB typ | $R_L = 50\ \Omega, f = 1\text{ MHz}$; see Figure 15 |
| C_S (Off) | 13 | | | pF typ | $f = 1\text{ MHz}$ |
| C_D, C_S (On) | 65 | | | pF typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 0.0001 | | | μA typ | $V_{DD} = 13.2\text{ V}$ $V_{IN} = 0\text{ V}$ or 5 V |
| | 1 | 2.5 | 2.5 | μA max | |
| I_L | 0.0001 | | | μA typ | $V_L = 5.5\text{ V}$ |
| | 1 | 2.5 | 2.5 | μA max | |

¹ Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

| Parameter | Rating |
|---|---|
| V_{DD} to V_{SS} | 44 V |
| V_{DD} to GND | -0.3 V to +25 V |
| V_{SS} to GND | +0.3 V to -25 V |
| V_L to GND | -0.3 V to $V_{DD} + 0.3$ V |
| Analog, Digital Inputs ¹ | $V_{SS} - 2$ V to $V_{DD} + 2$ V or 30 mA, whichever occurs first |
| Continuous Current, Sx or D | 30 mA |
| Peak Current, Sx or D (Pulsed at 1 ms, 10% Duty Cycle Maximum) | 100 mA |
| Operating Temperature Range | -55°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| Power Dissipation (MSOP) | 315 mW |
| Thermal Impedance, θ_{JA} | 205°C/W |
| Lead Temperature, Soldering | As per JEDEC J-STD-020 |

¹ Overvoltages at IN, Sx, or D are clamped by internal diodes. Limit current to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one maximum rating may be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADG419-EP

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

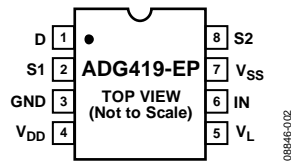


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-----------------|--|
| 1 | D | Drain Terminal. Can be an input or an output. |
| 2 | S1 | Source Terminal. Can be an input or an output. |
| 3 | GND | Ground Reference (0 V). |
| 4 | V _{DD} | Most Positive Power Supply Potential. |
| 5 | V _L | Logic Power Supply (5 V). |
| 6 | IN | Logic Control Input. |
| 7 | V _{SS} | Most Negative Power Supply Potential in Dual-Supply Applications. In single-supply applications, this pin can be connected to GND. |
| 8 | S2 | Source Terminal. Can be an input or an output. |

Table 5. Truth Table

| Logic | Switch 1 | Switch 2 |
|-------|----------|----------|
| 0 | On | Off |
| 1 | Off | On |

TYPICAL PERFORMANCE CHARACTERISTICS

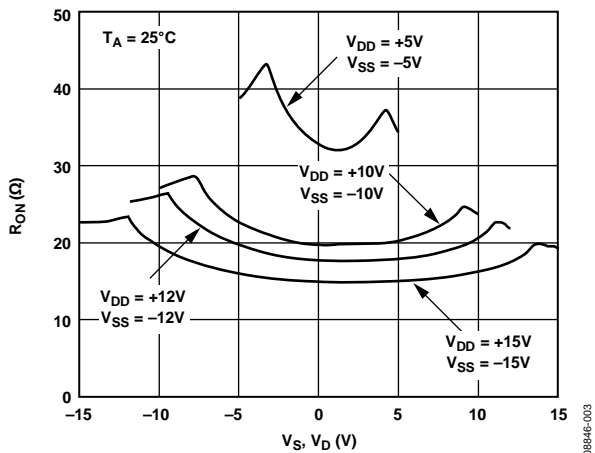


Figure 3. R_{ON} as a Function of V_D (V_S), Dual-Supply Voltage

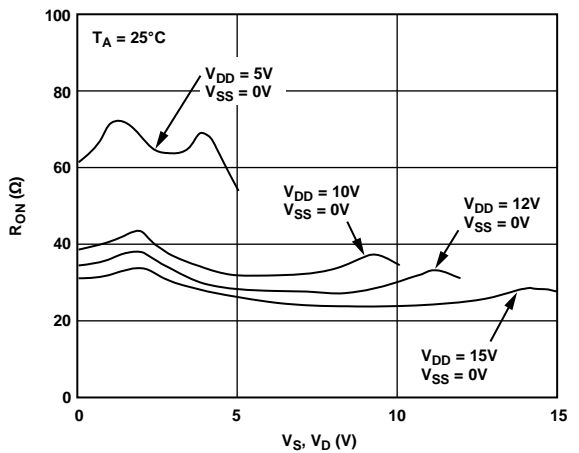


Figure 6. R_{ON} as a Function of V_D (V_S), Single-Supply Voltage

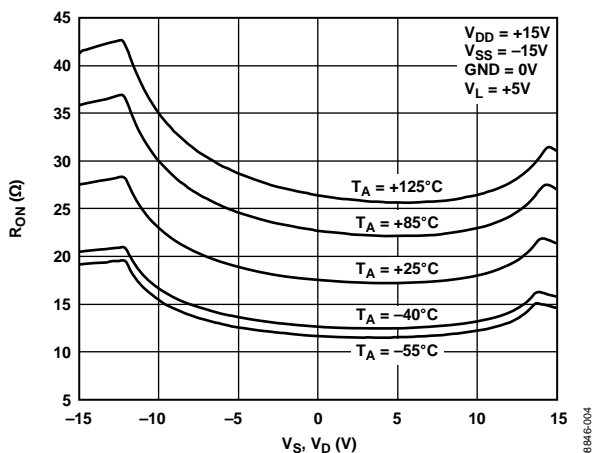


Figure 4. R_{ON} as a Function of V_D (V_S) for Different Temperatures, Dual-Supply Voltage

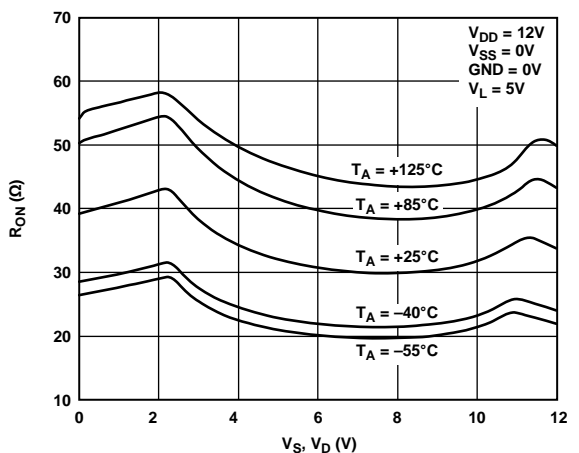


Figure 7. R_{ON} as a Function of V_D (V_S) for Different Temperatures, Single-Supply Voltage

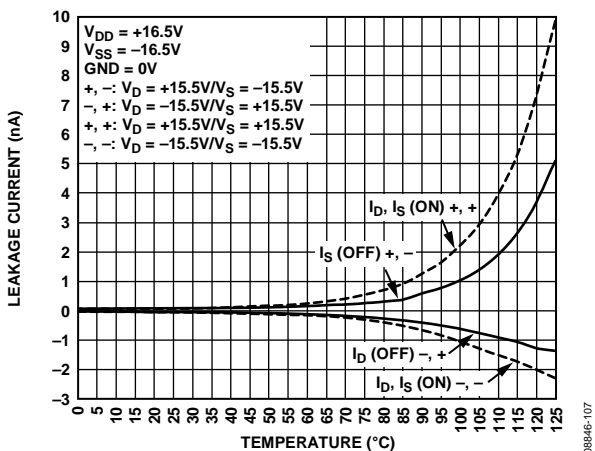


Figure 5. Leakage Current vs. Temperature, Dual-Supply Voltage

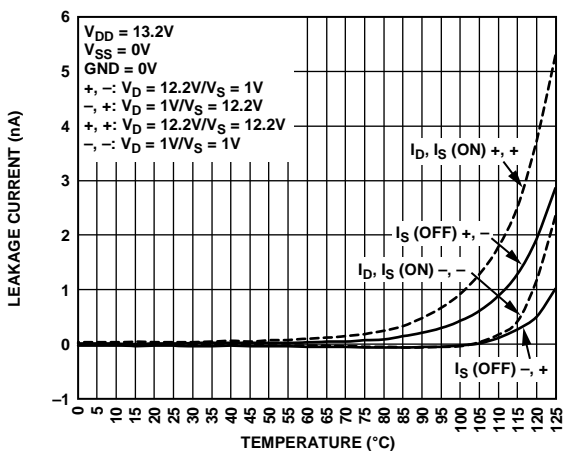


Figure 8. Leakage Current vs. Temperature, Single-Supply Voltage

TEST CIRCUITS

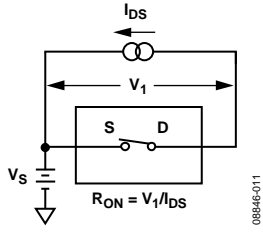


Figure 9. On Resistance

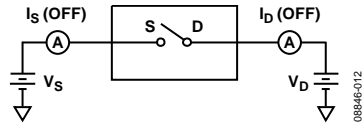


Figure 10. Off Leakage

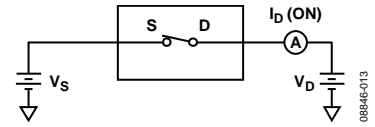


Figure 11. On Leakage

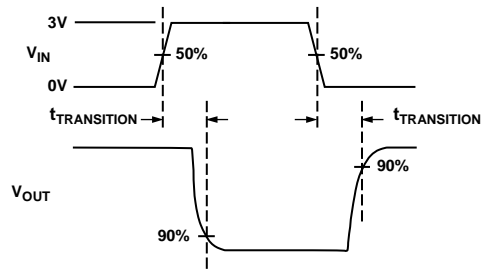
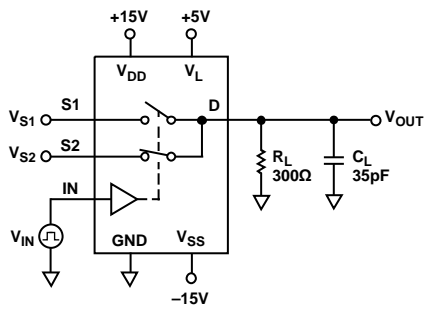


Figure 12. Transition Time, $t_{\text{TRANSITION}}$

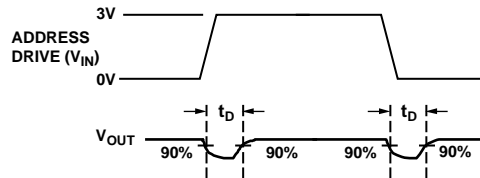
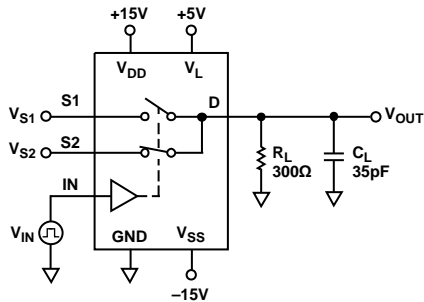
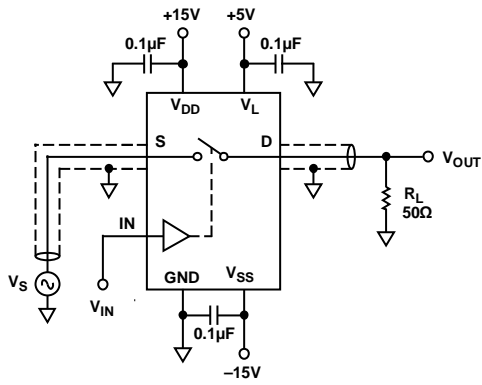
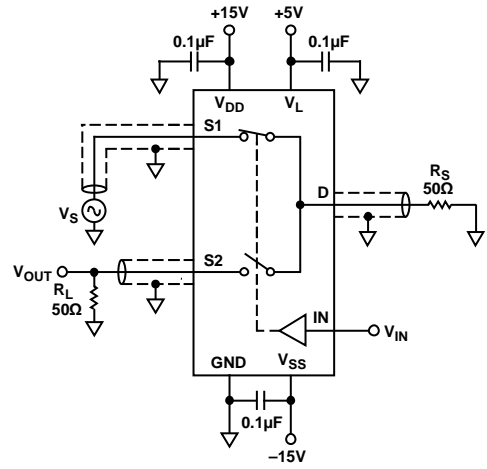


Figure 13. Break-Before-Make Time Delay, t_D



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Figure 14. Off Isolation



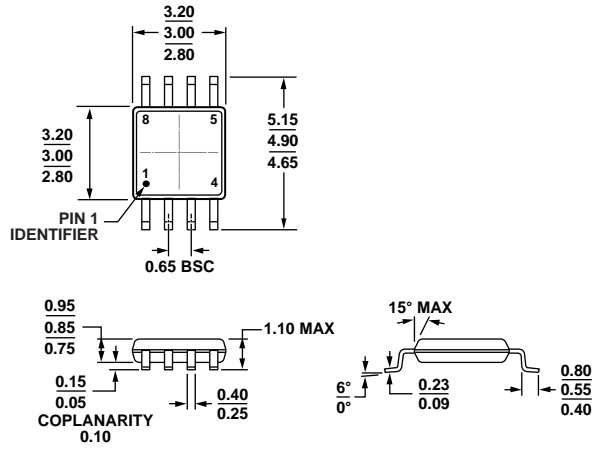
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CHANNEL-TO-CHANNEL CROSSTALK = $20 \times \log |V_S/V_{OUT}|$

Figure 15. Crosstalk

ADG419-EP

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 16. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters

1000705-B

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option | Branding |
|--------------------|-------------------|--|----------------|----------|
| ADG419SRMZ-EP-RL7 | -55°C to +125°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | S3U |

¹ Z = RoHS Compliant Part.

NOTES

ADG419-EP

NOTES