CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX882

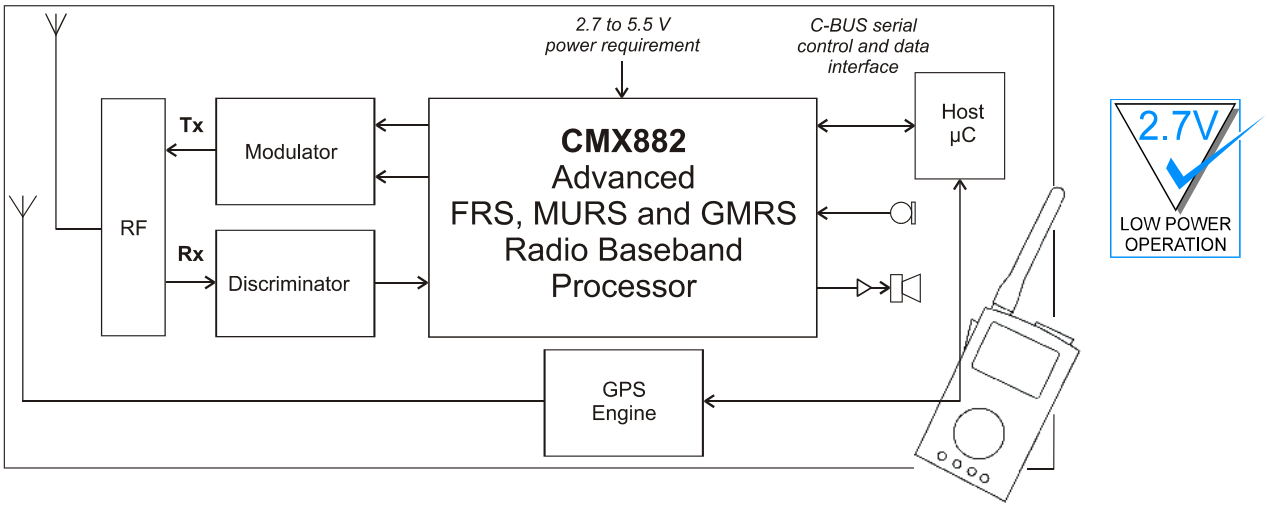
Baseband Processor for 'Leisure' Radios with Data

D/882/18 April 2009

Full-Feature Audio-Processing, Signalling and GPS Data for Half Duplex FRS, MURS, PMR446 and GMRS 'Leisure' Radios

Features

- Automatic signal type scanning and IRQ on detection of valid Rx signals, level or RSSI
- Tone generator for caller recognition tunes
- Programmable power down control
- Programmable signal detection thresholds
- Low Power operation with Zero Power mode
- Uncommitted Aux ADC with switchable input to monitor signals
- Silent operation by removal of unwanted calls
- Selectable voice companding
- XTCSS channel and data signalling
- Robust automatic packet data protocol with: Error correction and detection, Interleaving and data scrambling/privacy coding.
- Voice processing facilities, including Tx and Rx gain setting and voice/subaudio filtering
- C-BUS serial host interface
- RF interface allowing 1 or 2 point modulation
- Programmable soft limiter
- Enhanced CTCSS and 23/24 bit DCS codecs
- Zero 'talk down' CTCSS decoder performance prevents dropouts
- 'All call code' and 'monitor' modes for CTCSS
- Audio scrambling
- Robust Half Duplex FFSK/MSK modem, 1200/2400 bps, gets data through when signal is too degraded for voice – for text messaging/paging, location transfer, etc. applications.



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1.1 Brief Description

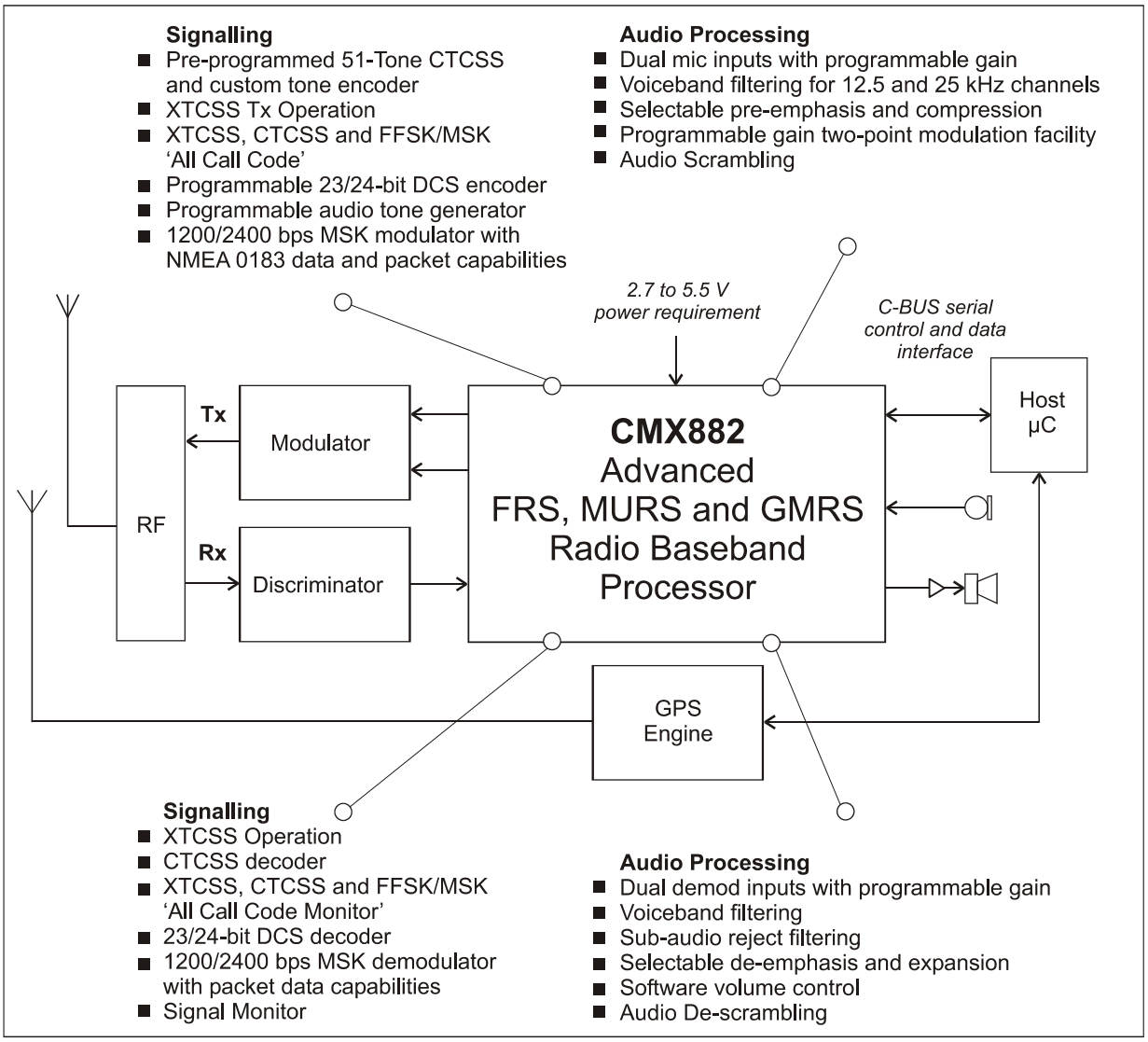
CMX882, a full-function half-duplex audio and signalling processor IC for FRS and PMR446 type facilities suitable for both complex and simple end-designs. Under the control of the host µC, all voiceband requirements are catered for: voiceband and sub-audio filtering, pre/de-emphasis, compression and expansion and audio routing and global level setting with single or two-point modulation in the transmit path.

The combination of new and standard signalling functions of this product offer, under software control, increased functionality, versatility and privacy. Standard Extended-Code CTCSS and DCS functions are integrated with the new XTCSS code implementation. XTCSS provides additional and improved squelch-centred privacy codes with the added advantage of 'silent operation'; no annoying interference from other sub-audio users. XTCSS fitted radios enjoy more privacy and flexibility of operation.

For advanced and enhanced radio operation, the CMX882 provides a 1200/2400 bps free-format and packet data FFSK/MSK modem for text messaging/paging, passing GPS location data (compatible with NMEA 0183) and other data applications.

With ultra low power requirements and graduated powersave, this product only requires a smaller, lower-power µC than existing FRS/PMR446 solutions. It is available in compact SSOP and TSSOP packages.

CMX882 Functions and Facilities



Half Duplex Operation

Working in a half duplex mode, when the product is in Tx the Rx sections can be powered down to extend battery life, conversely in Rx major sections of the Tx can be treated in the same manner.

Serial Control and Data Interfaces

C-BUS: Serial control, data and command program interface compatible with SCI, SPI and Microwire type interfaces.

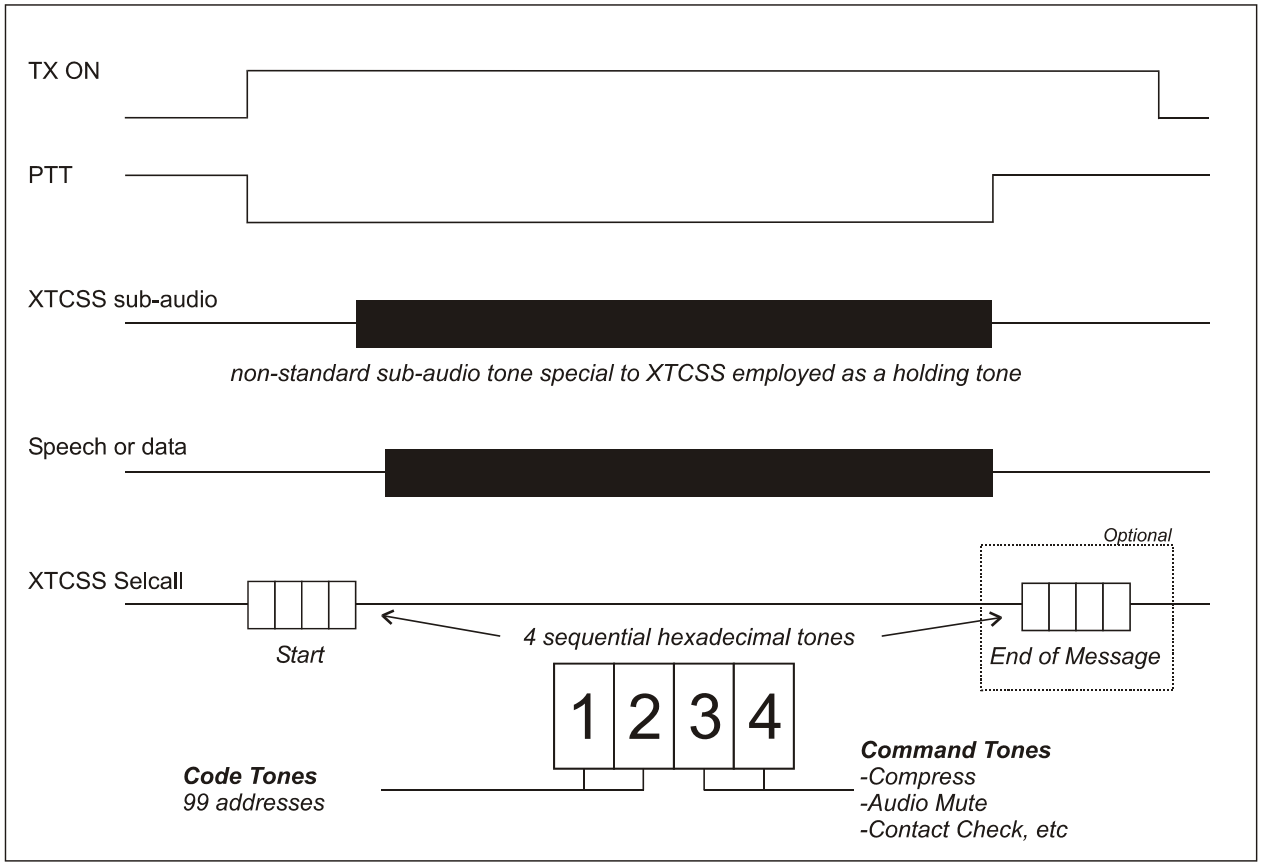
Power Requirements and Economy

With an ultra low power requirement, the CMX882 operates from a single 2.7 to 5.5 Volt supply with graduated 'Sleep Mode' powersaving facilities for both Rx and Tx modes.

Signalling:

XTCSS

A state-of-the-art (squelch) signalling format, employing both sub-audio (CTCSS) and in-band (XTC) signalling concurrently, which offers more than twice as many privacy codes as standard CTCSS operation and completely eliminates interference caused by other traffic on the channel (quiet operation). Additionally the XTCSS signalling can be employed as an over-air control for such features as voice-compression. XTCSS is fully compatible with both conventional and enhanced CTCSS signalling operations and will implement the *All Call Code* function.



CTCSS

'Zero talkdown' performance eliminates unwanted breaks in communication. The CMX882 is pre-programmed with 39 standard CTCSS (+ Notone and DCS 'turn off' tone) and 12 additional 'split-tone' frequencies. Any one of these can be selected for reception or transmission. Decoding is aided by the use of adjustable decode bandwidths and threshold levels. Decoding is carried out rapidly thus avoiding the loss of the beginning of speech or data signals. A CTCSS configuration of this product enables 'Tone Cloning'.

Two unique features of this product are its CTCSS 'All Call Code' and 'All Codes Monitor' modes:
All Call Code – transmissions using this code will be heard by all CMX882 enhanced radios regardless of their selected CTCSS code. This provides an important benefit to both safety and convenience.
All Codes Monitor – selection of this code at the receiver enables all transmissions that are using a CTCSS tone to be heard, and the tone number to be reported. Open channel noise or calls lacking coding, will go unheard. This is a superior method of 'channel monitoring', which allows miscoded calls from conventional CTCSS-party radios to be heard and directly responded to.

DCS

The DCS code is in NRZ format and is transmitted at 134.4b/s in either 23 or 24 bit patterns. The code,

for transmission or reception is programmed via the host µC with the 'turn off' tone being supplied from the CTCSS facility. Decoding is carried out rapidly thus avoiding the loss of the beginning of speech or data signals.

FFSK/MSK Modem

This high performance modem facilitates data transfers (e.g. text messaging/paging caller identification, caller location, digital poll of remote radio location, GPS information, etc.) by providing a 1200/2400 bps MSK data packet encoder (suitable for NMEA 0183 data transfer). Software selectable interleaving, error correction (FEC), error checking (CRC) and data scrambling functions provide multiple communication types to select from robustness, speed and privacy options. In the Rx path, a 1200/2400 bps data packet decoder features automatic bit-rate recognition, 16-bit frame-sync detector, error correction and checking, data de-scrambling and packet disassembly. High performance allows the modem to be used even when radio link quality is too degraded for voice communications.

Modulation type is optimised to maximise robustness and data rate and simplify hardware connections to voice radio Tx and Rx circuits with virtually no modification. The modulation type also is appropriate to develop F2D type emissions, as required by certain regulations. (F2D = frequency modulation, digital modulation with modulated subcarrier, transmitted information is data/telemetry/telecommand).

Signal Monitor

An auxiliary circuit intended for the monitoring of any signal or level; both internal and external. This function can be used in conjunction with the host µC to allow such activities as: VOX operation and/or the 'wake-up' of powered-down circuitry.

Audio Processing:

Adjustable Gain Input Amplifiers

Selectable, component adjustable inputs are available for microphone or line voiceband or discriminator inputs. In either mode (Tx or Rx) the selected input can be further level adjusted under the control of the host µC prior to signal or audio- processing.

Voiceband and Sub-Audio Filtering with Limiting

Both Rx and Tx paths present voiceband filtering; the Tx path filter can be configured to either 12.5 or 25 kHz channel spacing whilst the Rx path also includes a sub-audio passband filter.

Voiceband Pre-emphasis and De-emphasis

Voiceband pre-emphasis is selectable to either 12.5 or 25 kHz channel configurations in the Tx path; de-emphasis at -6dB/ octave is selectable in the Rx path.

Software Adjustable Gains, Volume, Mixing and Routing

Providing total flexibility of operation, this product, under µC control has the ability to select and route functions and audio and signal paths, set bandwidths and threshold levels, mix audio and sub bands and vary both input and out gain/attenuation levels. Output levels from all analogue ports can be 'ramped' up and down at independently programmed rates.

Attenuation-Adjustable Single/Two-Point Modulation Outputs

To facilitate a wide range of transmitter types, the CMX882 has the ability to provide, independently programmable, modulation outputs; for single or two-point modulation schemes.

Scrambler

An optional frequency inversion scrambler is provided in both transmit and receive modes.

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It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

1.2 Block Diagram

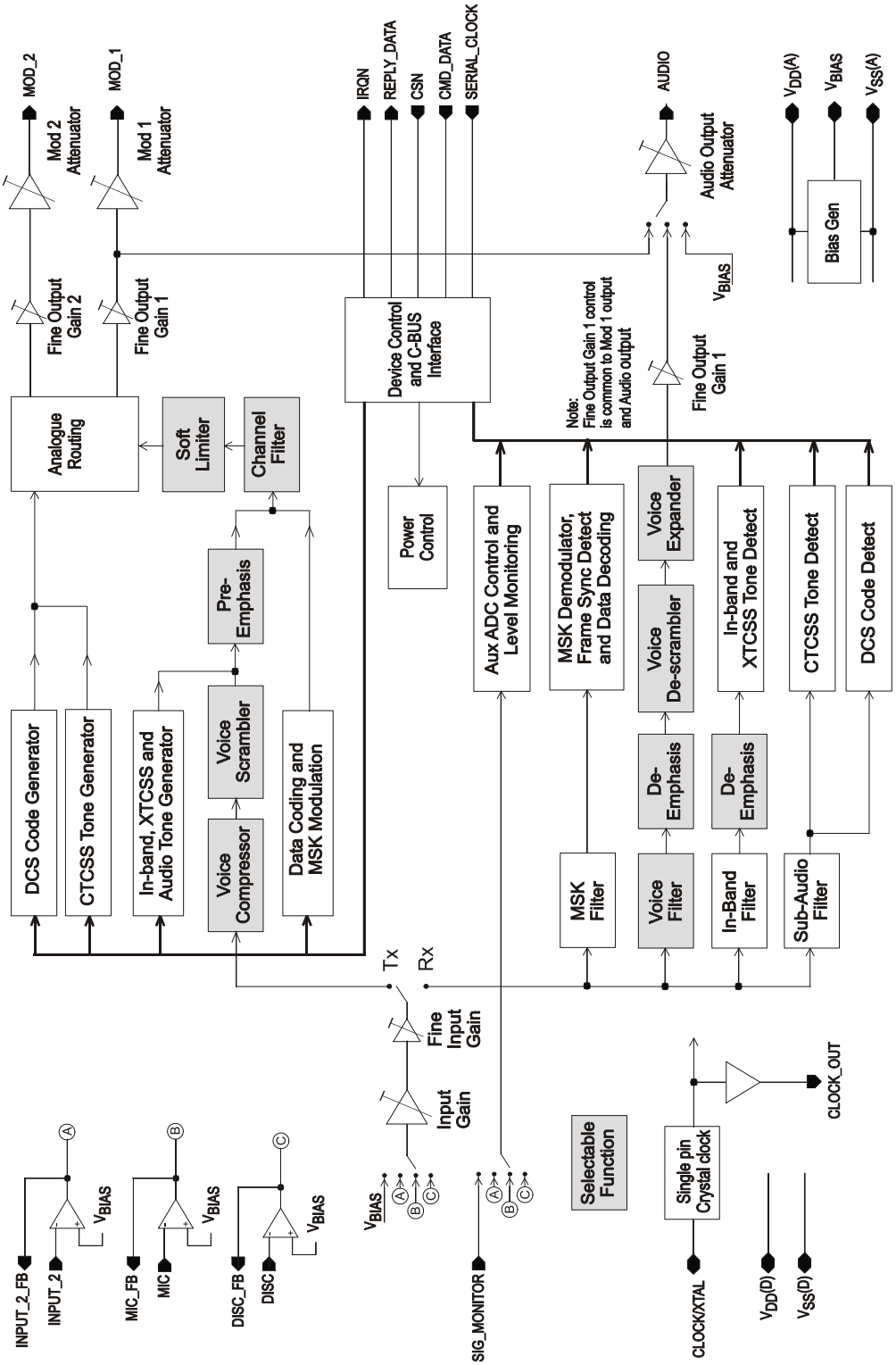


Figure 1 Block Diagram

1.3 Signal List

Package D6, E1	Signal		Description
Pin No.	**Name**	**Type**	
23	$V_{DD(D)}$	Power	The digital positive supply rail. This pin should be decoupled to $V_{SS(D)}$ by a capacitor mounted close to the device pins.
5	$V_{SS(D)}$	Power	The negative supply rail (digital ground).
18	$V_{DD(A)}$	Power	The analogue positive supply rail. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to $V_{SS(A)}$ by a capacitor mounted close to the device pins.
9, 21	$V_{SS(A)}$	Power	The negative supply rail. Both pins must be connected to analogue ground.
1, 2		NC	No connection should be made to these pins.
3	IRQN	O/P	A 'wire-ORable' output for connection to the Interrupt Request input of the host. This output is pulled down to $V_{SS(D)}$ when active and is high impedance when inactive. An external pull-up resistor is required.
4	REPLY_DATA	T/S	The C-BUS serial data output to the host. This output is held at high impedance when not sending data to the host.
6	SERIAL_CLOCK	I/P	The C-BUS serial clock input from the host.
7	CMD_DATA	I/P	The C-BUS serial data input from the host.
8	CSN	I/P	The C-BUS data loading control function. Data transfer sequences are initiated, and completed by the CSN signal.

1.3 Signal List (continued)

Package D6, E1	Signal		Description
Pin No.	**Name**	**Type**	
10	V_{BIAS}	O/P	Internally generated bias voltage of approximately $V_{DD(A)}/2$, except when bias is power-saved when V_{BIAS} will discharge to $V_{SS(A)}$. This pin should be decoupled to $V_{SS(A)}$ by a capacitor mounted close to the device pins.
11	DISC	I/P	Input terminal of discriminator input amplifier.
12	DISC_FB	O/P	Output / feedback terminal of discriminator input amplifier.
13	INPUT_2	I/P	Input terminal of amplifier 2, for either a second microphone or discriminator input.
14	INPUT_2_FB	O/P	Output / feedback terminal of input amplifier 2.
15	MIC	I/P	Input terminal of microphone input amplifier.
16	MIC_FB	O/P	Output / feedback terminal of microphone input amplifier.
17	SIG_MONITOR	I/P	Signal Monitor input to the internal level detecting circuit.
19	MOD_1	O/P	Modulator 1 output.
20	MOD_2	O/P	Modulator 2 output.
22	AUDIO	O/P	Output of the audio section.
24	CLOCK/XTAL	I/P	The input to the on-chip oscillator for an external crystal or a clock circuit.
25	CLOCK_OUT	O/P	Buffered (un-inverted) clock output available for use by other devices in the system.
26		I/P	Test input, connect to $V_{SS(D)}$.
27, 28		NC	No connection should be made to these pins.

Notes: I/P = Input
O/P = Output
T/S = 3-state Output
NC = No Connection

1.4 External Components

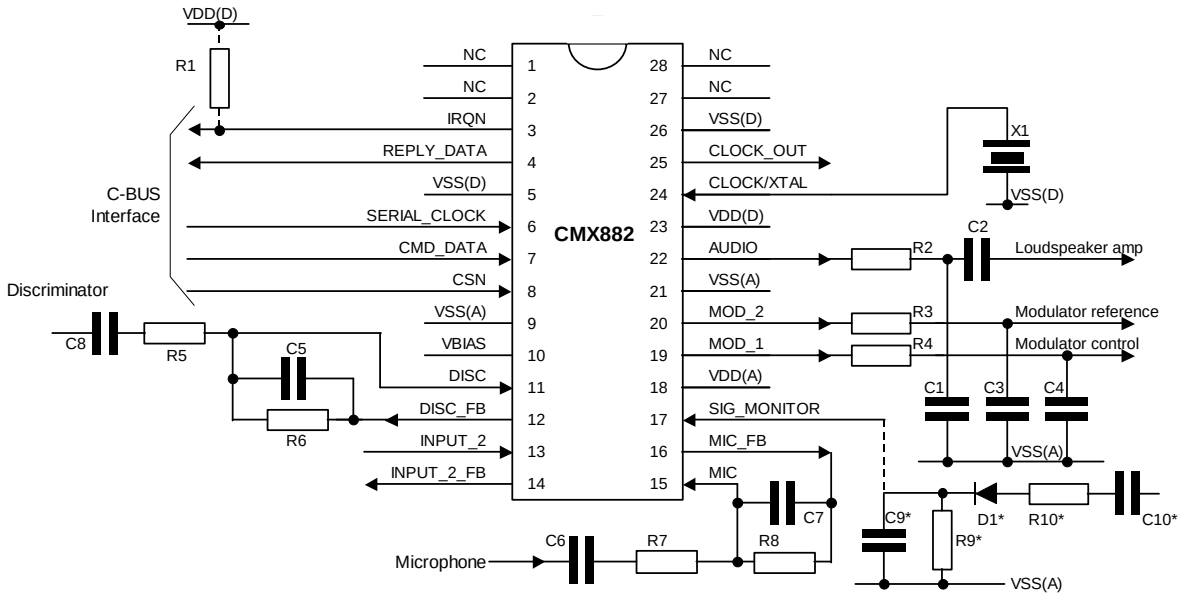


Figure 2 Recommended External Components

R1	100kΩ	R9	See note 6	C6	See note 4	
R2	100kΩ	R10	See note 6	C7	200pF	
R3	100kΩ			C8	See note 4	
R4	100kΩ	C1	100pF	C9/10	See note 6	
R5	See note 2	C2	1nF			
R6	100kΩ	C3	100pF	X1	18.432MHz	See note 1
R7	See note 3	C4	100pF			
R8	100kΩ	C5	100pF	D1	See note 6	

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The clock drift requirement is defined in section 1.8.1. The tracks between the crystal and pin 24 and pin 5 should be as short as possible to achieve maximum stability and best start up performance.

2. R5 should be selected to provide the desired dc gain (assuming C8 is not present) of the discriminator input, as follows:

$$|GAIN_{Disc}| = 100k\Omega / R5$$

The gain should be such that the resultant output at the DISC_FB pin is within the discriminator input signal range specified in section 1.8.1.

3. R7 should be selected to provide the desired dc gain (assuming C6 is not present) of the microphone input as follows:

$$|GAIN_{Mic}| = 100k\Omega / R7$$

The gain should be such that the resultant output at the MIC_FB pin is within the microphone input signal range specified in section 1.8.1. For optimum performance with low signal microphones, an additional external gain stage may be required.

4. C6 and C8 should be selected to maintain the lower frequency roll-off of the microphone and discriminator inputs as follows:

$$C6 = 30nF \times |GAIN_{Mic}|$$
$$C8 = 1\mu F \times |GAIN_{Disc}|$$

5. INPUT_2 and INPUT_2_FB connections allow the user to have a second discriminator or microphone input. Component connections and values are as for the networks around pins 11 and 12 or pins 15 and 16 respectively. If this input is not required pin 13 must be connected to pin 14.

6. The circuit formed by D1, C9, C10, R9 and R10 is a peak detector, this is only required when the signal monitor is connected to an ac signal (e.g. microphone or received signal). For a dc type signal (e.g. RSSI) these components are not required. The values of C9 and R10 set the attack time, C9 and R9 set the decay time. D1 can be any suitable small signal diode. R10 should be a high enough value so as not to distort the signal source.

1.4.1 PCB Layout Guidelines and Power Supply Decoupling

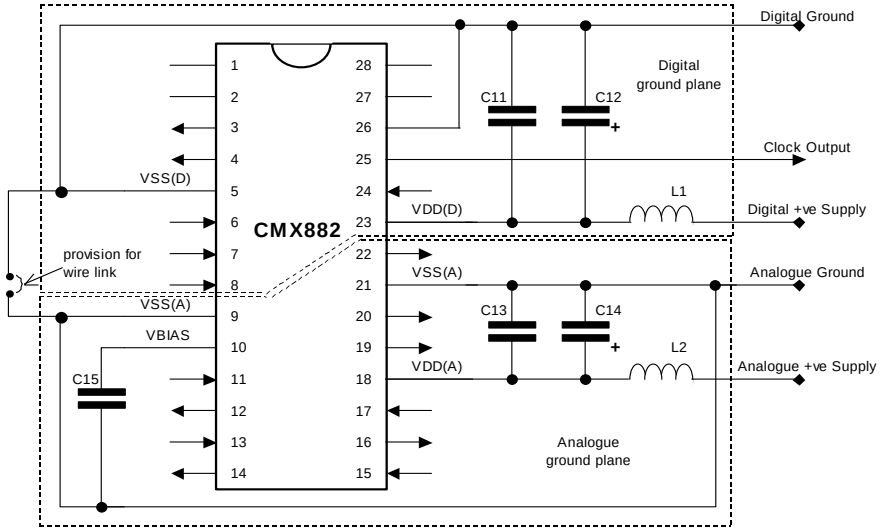


Figure 3 Power Supply Connections and De-coupling

C11	10nF	C14	10µF	L1	100nH	See note 7
C12	10µF	C15	100nF	L2	100nH	See note 7
C13	10nF					

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:
7. The inductors L1 and L2 can be omitted but this may degrade system performance.

It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the CMX882 and the supply and bias de-coupling capacitors. The de-coupling capacitors C11, C12, C13 and C14 should be as close as possible to the CMX882, particularly C11 and C13. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the V_{SS}(A) and V_{SS}(D) in the area of the CMX882, with provision to make a link between them close to the CMX882.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it must be buffered with a high input impedance buffer.

The single ended microphone input(s) and audio output must be ac coupled as shown, so their return paths can be connected to V_{SS}(A) without introducing dc offsets. Further buffering of the audio output is advised.

The crystal X1 can be replaced with an external clock source if required/desired. The internal clock generating circuit can be placed in power-save mode if the clock is provided externally.

1.4.2 Modulator Outputs

The combination of CMX882 and the modulator output components, R3/C3 and R4/C4, achieve roll-off rates better than –60dB/decade. If required this can be increased to better than –100dB/decade by replacing R3/C3 and R4/C4 with the active filter circuit shown in Figure 4.

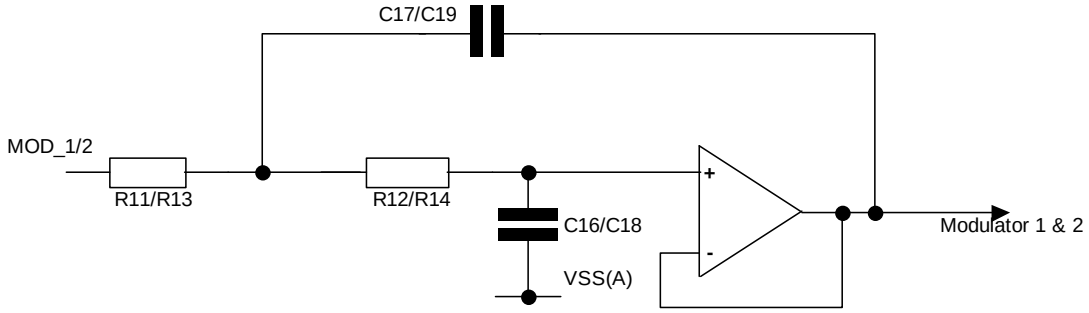


Figure 4 Modulator output components to achieve -100dB/decade roll-off

R11	120kΩ	C16	220pF	
R12	120kΩ	C17	440pF	(2 x C16)
R13	120kΩ	C18	220pF	
R14	120kΩ	C19	440pF	(2 x C18)

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

8. The external op-amp must be chosen to ensure that the required signal output level can be driven within acceptable distortion limits.

1.5 General Description

The CMX882 is intended for use in half duplex analogue two way land mobile radio (LMR) equipment and is particularly suited to enhanced MURS / GMRS / FRS with GPS terminal designs. The CMX882 provides radio signal encoder and decoder functions for: Voice, in-band tones, XTCSS, CTCSS, DCS and FFSK/MSK data permitting simple to sophisticated levels of tone control and data transfer. Power control facilities allow the device to be placed in varying levels of sleep allowing the user to fine tune the power depending on system requirements. The CMX882 includes a crystal clock generator, with buffered output, to provide a common system clock if required. A block diagram of the CMX882 is shown in Figure 1.

Tx functions

Audio

- Single/dual microphone inputs with input amplifier and programmable gain adjustment
- Filtering selectable for 12.5kHz and 25kHz channels
- Selectable pre-emphasis
- Selectable compression
- Selectable frequency inversion voice scrambling
- 2-point modulation outputs with programmable level adjustment

Signalling

- Pre-programmed 51 tone CTCSS encoder
- Programmable 23/24bit DCS encoder
- Programmable audio tone generator (for custom audio tones)
- Pre-programmed XTCSS and in-band tone encoder
- 1200/2400bps MSK data packet encoder (suitable for text messaging/paging, caller identification, caller location, digital poll of remote radio location, GPS information via NMEA 0183 data transfer etc.), incorporating interleaving, FEC, CRC and data scrambler

Rx functions

Audio

- Single/dual demodulator inputs with input amplifier and programmable gain adjustment
- Voice-band and sub-audio rejection filtering
- Selectable de-emphasis
- Selectable expansion
- Selectable frequency inversion voice de-scrambling
- Software volume control

Signalling

- 1 from 51 CTCSS decoder + Tone Clone mode
- 23/24bit DCS decoder
- Pre-programmed in-band tone decode with XTCSS 4 tone addressing
- 1200/2400bps MSK data packet decoder with automatic bit rate recognition, 16 bit frame sync detector, error correction, data de-scrambler and packet disassembly
- Signal Monitor (RSSI / Microphone / Rx channel level monitor)

Voice Processing Combinations
Table 1 shows the valid voice processing combinations.

Table 1 Voice Processing Combinations

	TX				RX			
	Compress	Scramble	Pre-Emphasis	Filter	Filter	De-Emphasis	De-Scramble	Expand
1				✓	✓			
2			✓	✓	✓	✓		
3		✓	✓	✓	✓	✓	✓	
4		✓		✓	✓		✓	
5	✓		✓	✓	✓	✓		✓
6	✓		✓	✓				✓
Not Valid								
7	✓	✓	✓	✓	✓	✓	✓	✓
Not Recommended								
8[1]	✓	✓		✓	✓		✓	✓

Host Interface
A serial data interface (C-BUS) is used for command, status and data transfers between the CMX882 and the host μC; this interface is compatible with microwire, SPI etc. Interrupt signals notify the host μC when a change in status has occurred and the μC should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 1.6.15.

Auxiliary (Signal Monitor) analogue signal
The CMX882 includes a Signal level monitor. This is an 8-bit successive approximation ADC and a two level signal sensor. The two level sensor facility can be used in conjunction with the power saving mode to wake up powered down blocks, and issue an interrupt on the IRQN line when the Signal exceeds the preset threshold level. The auxiliary ADC voltage reference is taken directly from the V_{DD}(A) supply, so the Signal level being monitored should be derived from this supply voltage.

[1] Audio quality is somewhat degraded.

1.5.1 Sleep Mode and Auto Start Up

A power-on reset signal remains asserted for approximately 256 x xtal clock cycles after power is applied and the clock or xtal oscillator is established. It performs the same function as the C-BUS General Reset command ($01), further details of which are given in section 1.6.2. A temporary loss of power may cause the power-on reset signal to be re-asserted. If this happens, both the C-BUS registers and the Programming register block should be reprogrammed, once power has been restored and a C-BUS General Reset command has been issued. This is to prevent any possibility of data corruption within the device.

Power-on reset or C-BUS general reset places the CMX882 into sleep mode, which results in all internal blocks, except the xtal clock circuit, being placed in power-saved mode. The xtal clock circuit can be power-saved but this must be done by an explicit C-BUS command. Power saving is achieved by turning off bias current sources or disabling local clocks, as appropriate.

During system standby periods, parts of the device can be put into sleep mode by the host to conserve power. The Auxiliary ADC can be programmed so that when the level exceeds a threshold, an interrupt is issued over the C-BUS and the selected mode (Tx or Rx) “woken up” within 400µs. If this time is too long to ensure no part of the signal is lost, the DISC or MIC input and ADC path can be kept powered up whilst in standby mode. The receive modes and transmit modes can also be activated by commands from the C-BUS. On wake up, activation of the various signal path stages are phased appropriately to avoid causing unwanted transients. More details are provided in section 1.6.4 on Signal Routing.

The CMX882 can be programmed to wake up its receive path automatically (automatic start-up) when the DISC input level exceeds the ‘high’ level threshold. While the CMX882 is in automatic receive start-up mode the DISC input must also be selected for the signal path. When not in automatic start-up mode it is recommended that the required input is selected during Auxiliary ADC operation to avoid subsequent switching of the input signal source.

1.5.2 Auxiliary ADC

This section of the CMX882 operates in both Tx and Rx modes and can be used to monitor one of 4 signal sources: Sig_Monitor pin, MIC1, Input_2 or DISC inputs. Activity on the selected input will optionally issue an interrupt if host intervention is required. During idle periods the majority of the CMX882 can be placed into low power mode. If monitoring ac signals connected to the Sig_Monitor pin they must be rectified and filtered using passive external circuitry.

The Auxiliary ADC facility comprises an 8-bit ADC, a comparator, an 8-bit result data word and two 8-bit threshold registers, one defining the ‘Signal high’ level and the other the ‘Signal low’ level. The two threshold registers are combined into one 16-bit C-BUS register word. The ADC measures the Signal level at intervals that are set by C-BUS command. It is advised that the interval be set to <125µs while waiting for a new incoming signal so that the CMX882 and host µC can be powered up and put into the correct mode in time to avoid missing any part of the signal. The default interval period following a reset is 20.8µs. Power dissipation of the Auxiliary ADC can be reduced by increasing the conversion interval time.

The result of the most recent Auxiliary ADC measurement can be read over the C-BUS whenever the Signal Processing and Aux ADC circuits are powered up.

The Auxiliary ADC compares each conversion result with the values in the ‘Signal high’ or the ‘Signal low’ threshold registers. The CMX882 can, for example, issue an interrupt to the host µC to wake up the receive path when the Auxiliary ADC input exceeds the ‘high’ level threshold. The CMX882 can also issue an interrupt to the host µC to indicate a weak or absent signal when it falls below the ‘low’ level threshold. This provides a user programmable hysteresis facility. The host must ensure that the value in the ‘low’ register is always less than that of the ‘high’ register. The options for issuing interrupts and for automatic start-up are selected by C-BUS command.

The Auxiliary ADC options are controlled by the $B2, $B3 and $C0 C-BUS registers. The auxiliary ADC data can be read from the $B4 C-BUS register.

The Auxiliary ADC requires the Auxiliary ADC, BIAS and Xtal clock to all be enabled in the Power Down Control register.

1.5.3 Receive Mode

The CMX882 can receive voice and various signal formats: CTCSS tone, DCS code, XTCSS / In-band tones and FFSK/MSK data at 1200 and 2400bps. Reception of each of these signal types can be independently enabled/disabled by C-BUS command. If enabled, an interrupt will be issued to notify the host μC of the presence and type of the incoming signal.

In receive mode the CMX882 performs signal type identification in 2 frequency bands, sub-audio (60 - 260Hz) and voice band (300 - 3kHz), to determine what type of signal is being received. When an enabled signal is detected this will be indicated to the host over the C-BUS and the CMX882 will continue to process the received signal in its band. Identification / process mode will continue in the other band. The CMX882 can process voice and simultaneously identify and process at least 2 other signal types. See Table 2 for valid combinations. These combinations can be used with Voice Processing, if desired.

The receive gain and audio output amplifier gain can be adjusted by the host μC, via C-BUS command, to provide receive signal level adjustment and output volume control or muting.

Table 2 Concurrent Rx Signalling Modes Supported by the CMX882

	Sub-Audio *All combinations of:*	Voice band signalling *Any one of A - C:*
With Rx Voice Processing[1] or Audio Tone generation	DCS Inverted DCS CTCSS	A: None B: XTCSS[3, 4] C: 1200bps FFSK/MSK

	Sub-Audio *All combinations of:*	Voice band signalling *Any one of A:*
With Rx Voice Processing[2]	DCS Inverted DCS CTCSS	A: None

	Sub-Audio *All combinations of:*	Voice band signalling *Any one of A - G:*
No Voice Processing or Audio Tone generation	DCS Inverted DCS CTCSS	A: None B: XTCSS[3] C: 1200bps FFSK/MSK D: 2400bps FFSK/MSK E: 1200 & 2400 bps FFSK/MSK F: XTCSS[3] & 1200bps FFSK/MSK G: XTCSS[3] & 2400bps FFSK/MSK

	Sub-Audio *All combinations of:*	Voice band signalling *Any one of A - H:*
No Voice Processing or Audio Tone generation	No Subaudio processing	A: None B: XTCSS[3] C: 1200bps FFSK/MSK D: 2400bps FFSK/MSK E: 1200 & 2400 bps FFSK/MSK F: XTCSS[3] & 1200bps FFSK/MSK G: XTCSS[3] & 2400bps FFSK/MSK H: XTCSS[3] & 1200bps & 2400bps FFSK/MSK

1 Including optional de-emphasis, but excluding voice companding and scrambling

2 Including voice companding and scrambling

3 XTCSS or In-band tone signalling.

4 XTCSS or In-band tone can only be used with DCS disabled and, if enabled, CTCSS not operating in tone-clone mode.

By disabling all the decoding modes, the device can be configured to receive voice only signals with no decoding of the voice band, CTCSS or DCS signalling. This will result in reception of all signals as if they are voice. In this case it is up to the user/host μC to respond appropriately to incoming signals.

The CMX882 operates in half duplex, so whilst in receive mode the transmit path (microphone input and modulator output amplifiers) can be disabled and powered down if required. The AUDIO output signal level is equalised (to V_{BIAS}) before switching between the audio port and the modulator ports, to minimise unwanted audible transients. The Off/Power-save level of the modulator outputs is the same as the V_{BIAS} pin, so the audio output level must also be at this level before switching.

1.5.3.1 Receiving Voice Band Signals

When a voice based signal is being received, it is up to the μC, in response to signal status information provided by the CMX882, to control muting/enabling of the voice band signal to the AUDIO output.

The discriminator path through the device has a programmable gain stage. Whilst in receive mode this should normally be set to 0dB (the default) gain.

Receive Filtering

The incoming signal is filtered, as shown in Figure 5, to remove sub-audio components and to minimise high frequency noise. When appropriate the voice signal can then be routed to the AUDIO output.

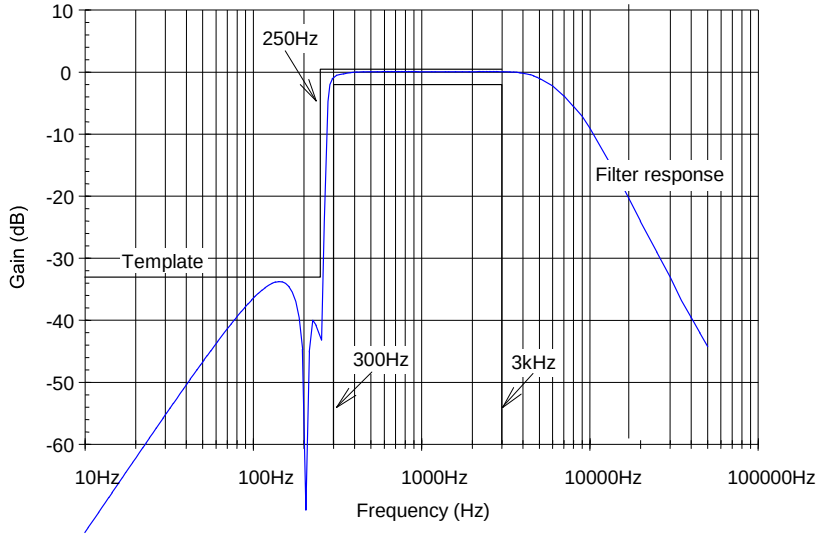


Figure 5 Rx Audio Filter Frequency Response

De-emphasis

Optional de-emphasis at -6dB per octave from 300Hz to 3000Hz (shown in Figure 6) can be selected to facilitate compliance with TIA/EIA-603.

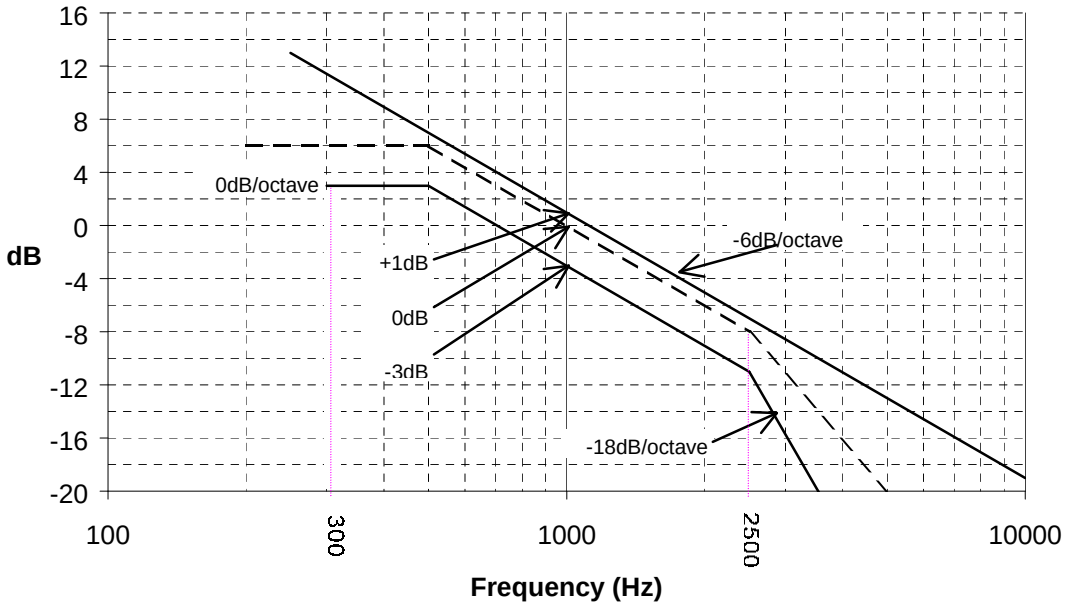


Figure 6 De-emphasis Curve for TIA/EIA-603 Compliance

Rx Companding (Expanding)
The CMX882 incorporates an optional syllabic compandor in both transmit and receive modes. This expands received voice band signals that have been similarly compressed in the transmitter to enhance dynamic range. The compandor attack, decay and 0dB point are defined in section 1.8.1. See section 1.6.9 for details of how to control this function.

Audio De-Scrambling
The CMX882 incorporates an optional frequency inversion de-scrambler in receive mode. This de-scrambles received voice band signals that have been scrambled in the transmitter. See section 1.6.9 for details of how to control this function.

Voice Processing Combinations
Table 1 shows the valid voice processing combinations. (See section 1.5).

1.5.3.2 Receiving and Decoding CTCSS Tones

The CMX882 is able to accurately detect valid CTCSS tones quickly to avoid losing the beginning of voice or possibly data transmissions, and is able to continuously monitor the detected tone with minimal probability of falsely dropping out. The received signal is filtered in accordance with the template shown in Figure 7, to prevent signals outside the sub-audio range from interfering with the sub-audio tone detection.

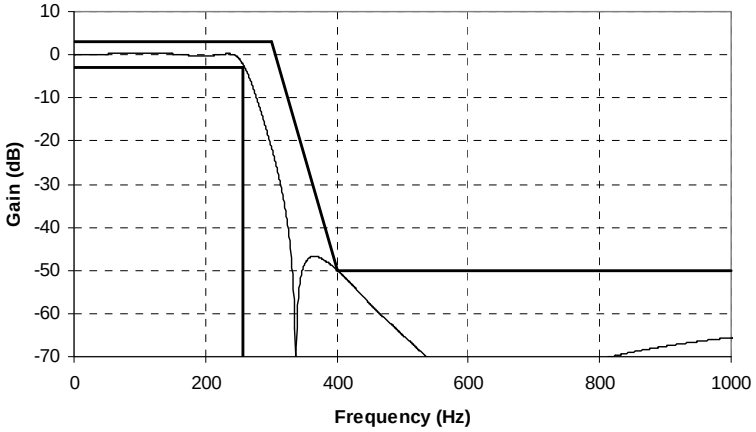


Figure 7 Low Pass Sub-Audio Band Filter for CTCSS and DCS

Once a valid CTCSS tone has been detected, the voice band signal can be passed to the audio output. The voice band signal is extracted from the received signal by band pass filtering as shown in Figure 5.

To help decode received CTCSS tones adjustable decoder bandwidths and threshold levels permit decode certainty and signal to noise performance to be traded when congestion or range limits the system performance. This entails setting the tone decoder bandwidth and threshold level in P2.1 of the Programming register ($C8) and programming the Audio & Device Address Control register with the desired tone.

Tone Cloning™:
Tone Cloning™ facilitates the detection of CTCSS tones 1 to 39 in receive mode. This allows the device to non-predictively detect any tone in this range. The received tone number will be reported in the Tones Status register. This tone code can then be programmed into the 'Audio and Device Address Control' register, by the host µC. The cloned tone will only be active when CTCSS is enabled in the Mode register.

™ Tone Cloning is a trademark of CML Microsystems Plc.

Tone cloning should not be used in systems where tones 41 to 51 or other split tones (tones between the frequencies of tones 1 to 40) may be received. The all call tone 40 can still be used after tone cloning has been performed.

It is recommended that the CTCSS bandwidth selected in Programming Register word P2.1 is set to be sufficiently low to ensure no overlapping of adjacent tones.

CTCSS Tones

Table 3 lists the CTCSS tones available. The tone numbers are decimal equivalents of the numbers written to the Audio & Device Address Control register ($C2) and reported in the Tone Status register ($CC).

Table 3 CTCSS Tones

Tone Number	Freq. (Hz)	Tone Number	Freq. (Hz)	Tone Number	Freq. (Hz)
00[1]	No Tone	20	131.8	40[2]	62.5*
01	67.0	21	136.5	41	159.8*
02	71.9	22	141.3	42	165.5*
03	74.4	23	146.2	43	171.3*
04	77.0	24	151.4	44	177.3*
05	79.7	25	156.7	45	183.5*
06	82.5	26	162.2	46	189.9*
07	85.4	27	167.9	47	196.6*
08	88.5	28	173.8	48	199.5*
09	91.5	29	179.9	49	206.5*
10	94.8	30	186.2	50	229.1*
11	97.4	31	192.8	51	254.1*
12	100.0	32	203.5	*52-54*	*Reserved*
13	103.5	33	210.7	*55*[3]	*Invalid*
14	107.2	34	218.1		*tone*
15	110.9	35	225.7	*>=56*	*Reserved*
16	114.8	36	233.6		
17	118.8	37	241.8		
18	123.0	38	250.3		
19	127.3	39	69.3		

* Subaudio tone not in TIA-603A standard.

Notes:

1 Tone number 00 in the Tone Status register ($CC) indicates that none of the above subaudio tones is being detected - see also section 1.6.19. If tone number 00 is programmed into the Audio & Device Address Control register ($C2) only tone 40 will be scanned for - see note 2. If CTCSS transmit is selected this tone setting will cause the CTCSS generator to output no signal.

2 Tone number 40 provides an all user CTCSS tone option; regardless of the subaudio tones set, the CMX882 will indicate to the host when this tone is detected whenever the CTCSS detector is enabled. This feature is useful for implementing emergency type calls e.g. all call.

3 Tone number 55 is reported in the Tone Status register ($CC), when CTCSS receive is enabled and a subaudio tone is detected that does not correspond to the selected tone or the all-call tone (tone number 40). This could be a tone in the subaudio band which is not in the table or a tone in the table which is not the selected tone or all-call tone.

1.5.3.3 Receiving and Decoding DCS Codes

DCS Code is in NRZ format and transmitted at 134.4 ±0.4bps. The CMX882 is able to decode any 23 or 24 bit pattern in either of the two DCS modulation modes defined by TIA/EIA-603 and described in Table 4. The CMX882 can detect a valid DCS Code quickly enough to avoid losing the beginning of voice transmissions.

Table 4 DCS Modulation Modes

Modulation Type:	Data Bit:	FM Frequency Change:
A	0	Minus frequency shift
	1	Plus frequency shift
B	0	Plus frequency shift
	1	Minus frequency shift

The CMX882 detects the DCS code that matches the programmed code defined in the 'DCS Code' words (P2.2-3) in the Programming register ($C8).

To detect the pre-programmed DCS code the signal is low pass filtered to suppress all but the sub-audio band using the filter shown in Figure 7. Further equalisation filtering, signal slicing and level detection are done to extract the code being received. The extracted code is then matched with the programmed 23 or 24-bit DCS code to be recognised, in the order least significant first through to most significant DCS code bit last. Table 5 shows a selection of valid 23-bit DCS codes, this does not preclude other codes being programmed. Recognition of a valid DCS Code will be flagged if the decode is successful (3 or less errors). A failure to decode is indicated by a '0' flag. This flag is updated after the decoding of every 4th bit of the incoming signal.

Once a valid DCS Code has been detected, the voice band signal can be passed to the AUDIO output under the control of the host µC. The voice signal is extracted from the received input signal by band pass filtering; see Figure 5. More details for programming DCS Codes are provided in section 1.6.20.3.

The end of DCS transmissions is indicated by a 134.4 ±0.5Hz tone for 150-200ms. To detect the DCS turn off tone while receiving DCS, the DCS turn off tone option must be selected in the Audio and Device Address Control ($C2) register. When a DCS turn off tone is detected it will cause a DCS interrupt; the receiver audio output can then be muted by the host.

Table 5 DCS 23 Bit Codes

DCS Code	DCS bits 22-12	DCS bits 11-0	DCS Code	DCS bits 22-12	DCS bits 11-0	DCS Code	DCS bits 22-12	DCS bits 11-0
023	763	813	174	18B	87C	445	7B8	925
025	6B7	815	205	6E9	885	464	27E	934
026	65D	816	223	68E	893	465	60B	935
031	51F	819	226	7B0	896	466	6E1	936
032	5F5	81A	243	45B	8A3	503	3C6	943
043	5B6	823	244	1FA	8A4	506	2F8	946
047	0FD	827	245	58F	8A5	516	41B	94E
051	7CA	829	251	627	8A9	532	0E3	95A
054	6F4	82C	261	177	8B1	546	19E	966
065	5D1	835	263	5E8	8B3	565	0C7	975
071	679	839	265	43C	8B5	606	5D9	986
072	693	83A	271	794	8B9	612	671	98A
073	2E6	83B	306	0CF	8C6	624	0F5	994
074	747	83C	311	38D	8C9	627	01F	997
114	35E	84C	315	6C6	8CD	631	728	999
115	72B	84D	331	23E	8D9	632	7C2	99A
116	7C1	84E	343	297	8E3	654	4C3	9AC
125	07B	855	346	3A9	8E6	662	247	9B2
131	3D3	859	351	0EB	8E9	664	393	9B4
132	339	85A	364	685	8F4	703	22B	9C3
134	2ED	85C	365	2F0	8F5	712	0BD	9CA
143	37A	863	371	158	8F9	723	398	9D3
152	1EC	86A	411	776	909	731	1E4	9D9
155	44D	86D	412	79C	90A	732	10E	9DA
156	4A7	86E	413	3E9	90B	734	0DA	9DC
162	6BC	872	423	4B9	913	743	14D	9E3
165	31D	875	431	6C5	919	754	20F	9EC
172	05F	87A	432	62F	91A			

1.5.3.4 Receiving and Decoding In-band Tones

In-band tones can be used to flag the start of a call or to confirm the end of a call. If they occur during a call the tone may be audible at the receiver. When enabled, an interrupt will be issued when a signal matching a valid In-band tone is detected and when a present In-band tone turns off or changes (i.e. at the start and at the end of each In-band tone).

The CMX882 implements QTC coding using the EEA tone set. Other addressing and data formats can be implemented but will require more host intervention. The custom tones (1-4) permit other audio tones to be encoded or decoded, the frequency of each tone is defined in the program registers P1.2-5.

In receive the CMX882 scans through the tone table sequentially, the code reported will be the first one that matches the incoming frequency.

Adjustable decoder bandwidths, threshold levels are programmable via the Programming register and permits certainty of detection and signal to noise performance to be traded when congestion or range limits the system performance. The In-band signal is derived from the received input signal after the band pass filtering shown in Figure 5.

Table 6 In-band Tones

Special / Information Tones (5^{th} bit = 0)		
4 bit Code		Freq.
Dec	Hex	(Hz)
0	0	No Tone
1	1	Custom Tone 0 P1.2[1]
2	2	Custom Tone 1 P1.3[1]
3	3	Custom Tone 2 P1.4[1]
4	4	Custom Tone 3 P1.5[1]
5	5	Reserved
6	6	
7	7	
8	8	
9	9	
10	A	
11	B	
12	C	
13	D	
14	E	
15	F	Unrecognised tone

Normal Tones (5^{th} bit = 1)		
4 bit Code		Freq.
Dec	Hex	(Hz)
0	0	1981
1	1	1124
2	2	1197
3	3	1275
4	4	1358
5	5	1446
6	6	1540
7	7	1640
8	8	1747
9	9	1860
10	A	1055
11	B	930
12	C	2247
13	D	991
14	E	2110[2]
15	F	Unrecognised tone

Notes:

1 Special tones 1-4 provide user programmable tone options for both transmit and receive modes as set in the indicated Program register, for programming information see section 1.6.20.2.

2 Normal tone 14 is the repeat tone, this code must be used in transmit when the new code to be sent is the same as the previous one. e.g. to send '333' the sequence '3R3' should be sent, where 'R' is the repeat tone. When receiving Selcall tones the CMX882 will indicate the repeat tone when it is received, it is up to the host to interpret this and decode tones accordingly.

1.5.3.5 Receiving FFSK Signals

The CMX882 can decode incoming FFSK/MSK signals at either 1200 or 2400 baud data rates. It can achieve this by deriving the baud rate from the received signal. Alternatively a control word may set the baud rate, in which case the device only responds to signals operating at that rate. The form of FFSK/MSK signals for these baud rates, excluding noise, is shown in Figure 11.

The received signal is filtered and data is extracted. A PLL is used to extract the clock from the recovered serial data stream. The recovered data is stored in a 2 or 4 byte buffer (grouped into 16-bit words) and an interrupt issued to indicate received data is ready. Data is transferred over the C-BUS, controlled by host instructions. If this data is not read before the next data is decoded it will be overwritten. The MSK bit clock is not output externally. It is up to the user to ensure that the data is transferred at an adequate rate following data ready being flagged, see Table 9.

The extracted data is compared with the 16 bit programmed frame sync pattern. It is preset to $CB23 following a RESET command. An interrupt will be flagged when the programmed frame sync pattern is detected or when the following Frame Head is decoded, see section 1.5.5. The host may stop the frame sync search by disabling the MSK demodulator.

If set to decode a Frame Head before interrupting, the CMX882 will check the CRC portion of the Frame Head Control Field. If this indicates a corrupt Frame Head a search for a new Frame Sync pattern will be automatically restarted.

FFSK may be transmitted in conjunction with a CTCSS or DCS sub-audio component. The device will handle the sub-audio signals as already described. If a sub-audio signal turns off during reception of FFSK, it is up to the host μC to turn off the FFSK decoding as the device will continue receiving and processing the incoming signal until commanded otherwise by the host μC.

The host must keep track of the message length or otherwise determine the end of reception (e.g. by using sub-audio information or the Auxiliary ADC to check for signal level) and disable the FFSK demodulator at the appropriate time. Note that when using packets with embedded size information the CMX882 will indicate when the last data block has been received.

1.5.3.6 Receiving XTCSS Signals

The CMX882 can decode and monitor for XTCSS signalling. XTCSS is used to identify the start and optionally the end of voice/data/other calls. It provides additional information and control over the basic CTCSS method of channel coding.

XTCSS coding starts with a 4 tone sequence indicating the address and content of the following message. Immediately after the 4 tone sequence a sub-audio maintenance tone is sent for the duration of the call. At the end of the call the maintenance tone is removed and an optional 4 tone sequence sent indicating the end of message (EOM). For further details on XTCSS see section 1.5.6.

By enabling XTCSS reception the host instructs the CMX882 to search for a valid 4 tone sequence, an interrupt (if enabled) will be generated when this occurs. The 4 tone sequence will be indicated in the C-BUS register ($C9) for the host to read out using the tone numbers in Table 6.

The sub-audio tone will be searched for after a valid 4 tone In-band sequence if CTCSS detection is also enabled. CTCSS codes will be decoded and reported as defined in section 1.5.3.2. It is necessary to enable CTCSS in the Mode Control register for the device to search for the XTCSS sub audio tone.

In receive, whenever the XTCSS detect bit is set the CMX882 will search for a valid 4 tone In-band sequence, however detection of a CTCSS tone will inhibit the search for 4 tone sequences. To be valid the 4 tones must be preceded and followed by silence in the audio band (in receive mode, silence is considered to be either unrecognised tones or signals below the audio detect level - see program register P1.1) for the programmed no tone time. The presence (or absence) of the sub-audio maintenance tone will only be indicated to the host if the XTCSS and CTCSS detect bits are both set in the Mode Control register. After the 4 tone sequence is detected the maintenance tone can be used by the host to detect fades and the end of the message and hence can disable the audio path in sympathy with this tone being absent. At any time the XTCSS enable bit is set and maintenance tone is not decoded the 4 tone set will be automatically searched for.

It is possible (although unlikely) that a fade will exactly coincide and obliterate 2 lots of 4 tone sequence indicating an EOM and the start of a new message. In this case, the host could misinterpret the received signal as a long fade and enable the voice when the maintenance tone reappears. It is therefore recommended that the host operates a timer that is started on loss of maintenance tone. If this times out the host can then assume that the fade is long enough that the original call is lost or has become so corrupted that it is not worth continuing with. The host could then choose only to restore the audio path on the next occurrence of a valid XTCSS tone set. Note that the XTCSS detector operates independently and the host may enable or disable the audio path at any time.

1.5.4 Transmit Mode

The device operates in half duplex, so when the device is in transmit mode the receive path (discriminator and audio output amplifiers) should be disabled, and can be powered down, by the host μC.

Two modulator outputs with independently programmable gains are provided to facilitate single or two-point modulation, separate sub-audio and voice band outputs. If one of the modulator outputs is not used it can be disabled to conserve power.

To avoid erroneous transmission of out of band frequencies when changing from Rx to Tx the MOD_1 and MOD_2 outputs are ramped to the quiescent modulator output level, V_{BIAS} before switching. Similarly, when starting a transmission, the transmitted signal strength is ramped up from the quiescent V_{BIAS} level and when ending a transmission the transmitted signal strength is ramped down to the quiescent V_{BIAS} level. The ramp rates are set in the Programming register P4.6. When the modulator outputs are disabled, their outputs will be set to V_{BIAS}. When the modulator output drivers are powered down, their outputs will be floating (high impedance), so the RF modulator will need to be turned off.

Table 7 Concurrent Tx Modes Supported by the CMX882

Sub-Audio		Voice band
CTCSS		
CTCSS	+	Voice
CTCSS	+	In-band tone
CTCSS	+	FFSK/MSK
CTCCS^	+	Voice
DCS		
DCS	+	Voice
DCS	+	In-band tone
DCS	+	FFSK/MSK
		Voice
		In-band
		FFSK/MSK
		XTCSS

^ Special XTCSS subaudio maintenance tone only

For all transmissions the host must only enable signals after the appropriate data and settings for those signals are loaded into the C-BUS registers. As soon as any signalling is enabled the CMX882 will use the settings to control the way information is transmitted.

A programmable gain stage in the microphone input path facilitates a host controlled VOGAD capability.

1.5.4.1 Processing Voice Signals for Transmission over Analogue Channels

The microphone input(s), with programmable gain, can be selected as the voice input source. Pre-emphasis is selectable with either version of the 2 analogue Tx audio filters (for 12.5kHz and 25kHz channel spacing). These are designed for use in ETS-300-086 and/or TIA/EIA-603 compliant applications. Both filters attenuate sub-audio frequencies below 250Hz by more than 33dB wrt the signal level at 1kHz. These filters together with a built in limiter help ensure compliance with ETS-300-086 (25kHz and 12.5kHz channel spacing) when levels and gain settings are set up correctly in the target system.

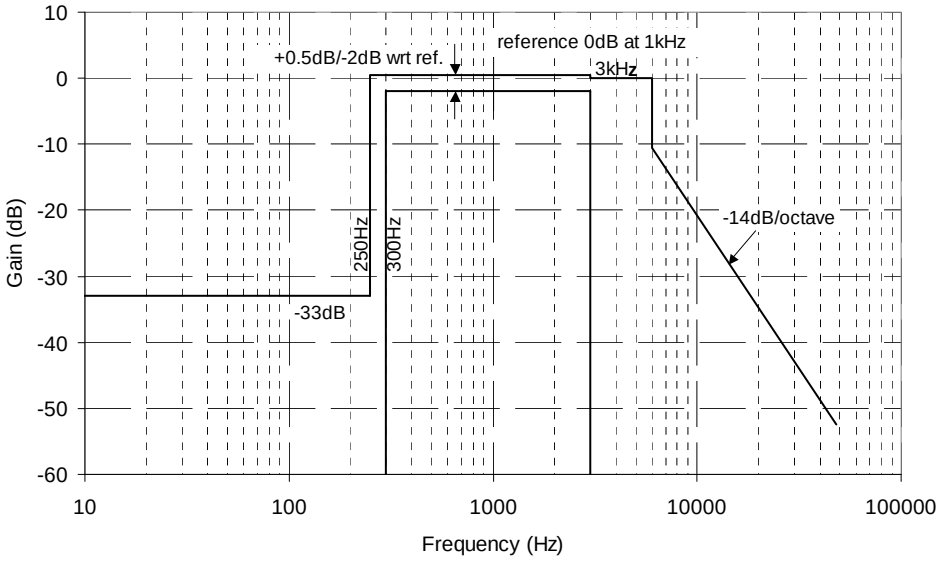


Figure 8 25kHz Channel Audio Filter Response Template

The filter characteristics of the 12.5kHz channel filter fits the filter template shown in Figure 9 (solid outline). This filter also facilitates implementation of systems compliant with TIA/EIA-603 'A' and 'B' bands. To achieve attenuation above 3kHz of better than −100dB/decade for TIA/EIA-603 'C' bands (dashed outline), additional external circuitry is required, such as suggested in section 1.4.2.

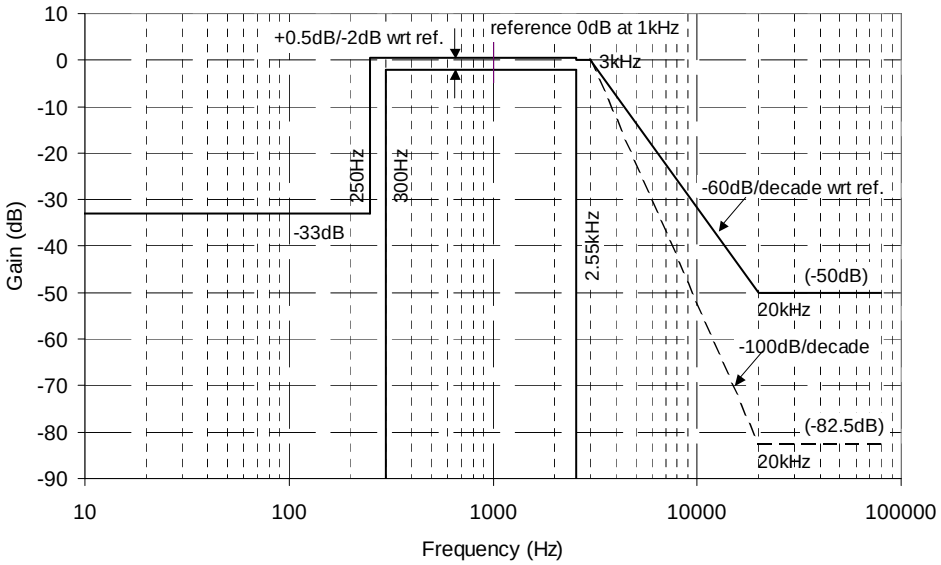


Figure 9 12.5kHz Channel Audio Filter Response Template

The CMX882 provides selectable pre-emphasis filtering of +6dB per octave from 300Hz to 3000Hz, matching the template shown in Figure 10.

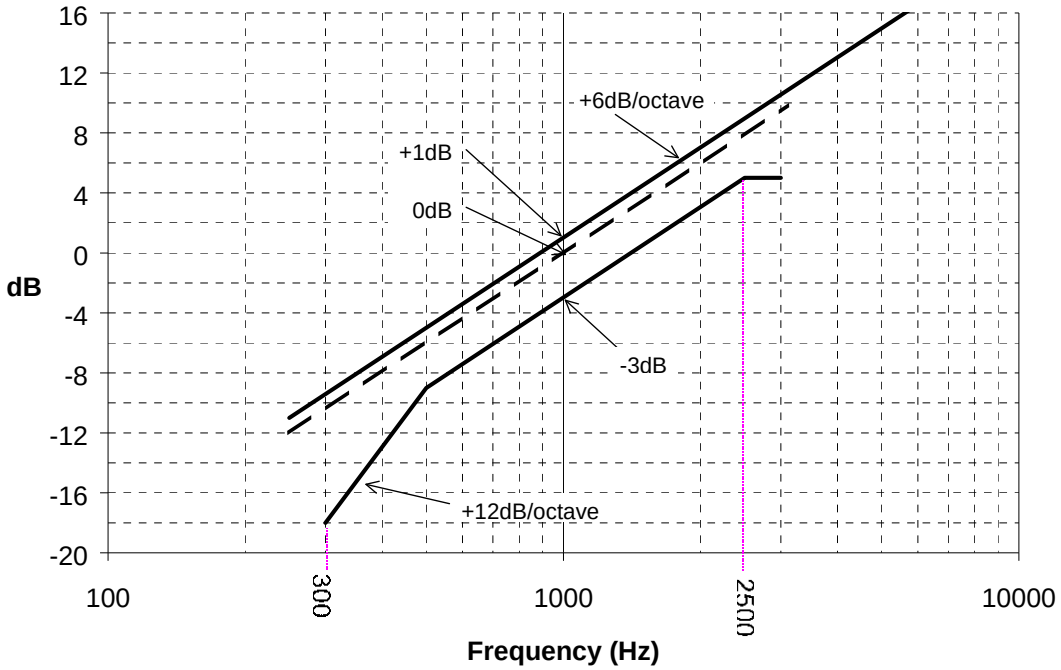


Figure 10 Audio Frequency Pre-emphasis Template

Modulator Output Routing
The sub-audio component can be combined with the voice band signal and this composite signal routed to both MOD_1 and MOD_2 outputs, or the sub-audio and voice band signal can be output separately (sub-audio to MOD_2 and voice band to MOD_1), in accordance with the settings of the Signal Routing register ($B1).

Tx Companding (Compressing)
The CMX882 incorporates an optional syllabic compandor in both transmit and receive mode. This compresses voice band signals before transmission to enhance dynamic range. The compandor attack, decay and 0dB point are defined in section 1.8.1. See section 1.6.9 for details of how to control this function.

Audio Scrambling
The CMX882 incorporates an optional frequency inversion scrambler in transmit mode. This scrambles voice band signals to be de-scrambled in the receiver. See section 1.6.9 for details of how to control this function.

Voice Processing Combinations
Table 1 shows the valid voice processing combinations (see section 1.5)

1.5.4.2 CTCSS Tone
The sub-audio CTCSS tone generated is defined in the Audio & Device Address Control register ($C2). Table 3 lists the CTCSS tones and the corresponding value for programming the TX TONE bits.

1.5.4.3 DCS Code
A 23 or 24-bit sub-audio DCS Code can be generated, as defined by the 'DCS Code' words (P2.2-3) of the Programming register ($C8); the same DCS Code pattern is used for detection and transmission. The DCS Code is NRZ encoded at 134.4±0.4 bits/s, low pass filtered and added to the voice band signal, prior

to passing the signal to the modulator output stages. Valid 23-bit DCS codes and the corresponding settings for the DCS Code Register are shown in Table 5, this does not preclude other codes being programmed. The least significant bit of the DCS code is transmitted first and the most significant bit is transmitted last. The CMX882 is able to encode and transmit either of the two DCS modulation modes defined by TIA/EIA-603 and described in Table 4.

To signal the end of the DCS transmission, the host should set the special sub-audio bits in the Audio & Device Address Control register ($C2) to enable the DCS turn off tone for 150ms to 200ms. After this time period has elapsed the host should then disable DCS in the Mode register ($C1). Do not enable CTCSS in the Mode Control ($C1) register when transmitting the DCS turn off tone. To summarize, detection of DCS turn off tone requires the CTCSS decoder to be enabled, whereas generation of the DCS turn off tone requires the CTCSS encoder to be disabled.

1.5.4.4 Transmitting In-band Tones

The In-band tone to be generated is defined in the Tx In-Band Tones register ($C3). The tone level is set in the Programming register (P1.4). The In-band tone must be transmitted without other signals in the voice band, so when either In-band signalling bit is selected, the voice path is automatically disabled. The voice path bit should not be set to '0' at this time, as this produces anomalous results. However, the voice path can be disabled by setting bits 4 and 5 to '00' in the Signal Routing register ($B1).

Table 6 shows valid In-band tones, together with the values for programming the In-band bits of the Tx In-Band Tones register.

Custom In-band tone frequencies are set in the program register ($C8) P1.2-5. See section 1.6.20.2 for programming details.

1.5.4.5 Transmitting FFSK/MSK Signals

The FFSK/MSK encoding operates in accordance with the bit settings in the Modem Control register ($C7). When enabled the MSK modulator begins transmitting data using the settings and values in block 0 of the Programming register (the bit sync and the frame sync patterns), the Modem Control register and the Tx Data register. Therefore, these registers should be programmed to the required value before transmission is enabled.

The CMX882 generates it's own internal data clock and converts the binary data into the appropriately phased frequencies, as shown in Figure 11 and Table 8. The binary data is taken from registers $CA and $CB, most significant bit first. The following data words must be provided over the C-BUS within certain time limits to ensure the selected baud rate is maintained. The time limits will be dependent on the data coding being used, see Table 9.

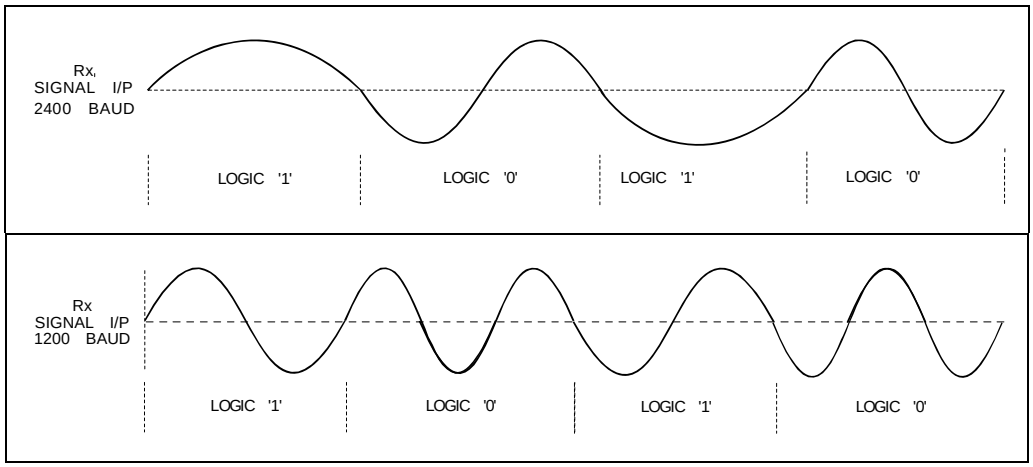


Figure 11 Modulating Waveforms for 1200 and 2400 Baud FFSK/MSK Signals

The table below shows the combinations of frequencies and number of cycles to represent each bit of data, for both baud rates.

Table 8 Data Frequencies for each Baud Rate

Baud Rate	Data	Frequency	Number of Cycles
1200 baud	1	1200Hz	one
	0	1800Hz	one and a half
2400 baud	1	1200Hz	half
	0	2400Hz	one

Note: FFSK may be transmitted in conjunction with a CTCSS or DCS sub-audio component.

1.5.4.6 Transmitting XTCSS Signalling

XTCSS signals can be transmitted by loading the 4 tone pattern and the special CTCSS (XTCSS maintenance) tone into the C-BUS registers and enabling XTCSS. The device will transmit the 4 tones in sequence, raise an interrupt when this is complete and then automatically generate the CTCSS tone, if selected in the Audio & Device Address Control register ($C2). At the end of the message the CTCSS tone is disabled by clearing the XTCSS maintenance tone bit (b9) to '0' in the Audio and Device Address Control register. The XTCSS 4 tone sequence must be transmitted on its own, so if a voice or a data signal is being transmitted, this must be disabled during the XTCSS 4 tone transmission. See section 1.5.6 for more information.

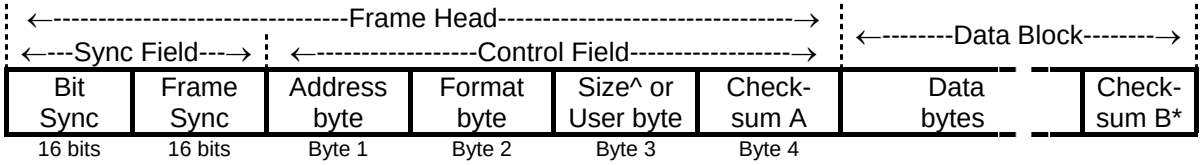
1.5.5 FFSK/MSK Data Packeting

The CMX882 has extensive data packeting features that can be controlled by the Modem Control register ($C7). The CMX882 can packet data in a variety of formats so the user can have the optimum data throughput for various signal to noise ratios. Data is transferred in packets or frames, each frame is made up of a Frame Head followed by any associated User Data. The Frame Head is composed of a 16 bit Bit Sync and 16 bit Frame Sync pattern immediately followed by 4 bytes of data. The 4 bytes of data start with an 8 bit address followed by 1 byte carrying information about the format of the following Data Block, a further byte indicates the size of the packet and the last byte is a checksum to detect if any of the 4 Frame Head bytes has been corrupted.

1.5.5.1 Tx Hang bit

When transmitting FFSK/MSK data with type 0, 2 or 3, the user should ensure that the data is terminated with a hang bit. To do this, the host must set the 'Last Data' bit in the Modem Control Register ($C7) after the last data word has been loaded into the Tx Data register, as described in section 1.6.11. This will append a hang bit onto the end of the current word and will stop modulating after the hang bit has been transmitted. It will also generate an interrupt (if enabled) when the hang bit has left the modulator.

1.5.5.2 Frame format



* Checksum B not applied to all Data Block types

^ Byte 3 is only reserved on sized data blocks.

The Data Block is made up from the User Data. This consists of a variable number of data bytes optionally encoded to ensure secure delivery over a radio channel to the receiver. Checksum B is only applied at the end of sized Data Blocks, the receiver can then detect if any of the User Data has been corrupted. Checksum B is composed of 16 bits for messages ≤16 bytes and 32 bits for longer messages.

1.5.5.3 Frame Head

The Frame Head forms an important part of a frame as it allows the receiver to detect and lock on to MSK signals, provides basic addressing to screen out unwanted messages and indicates the format, coding and length of any following data.

The 4 Control Field bytes have Forward Error Correction (FEC) applied to them in the transmitter, this adds 4 bits to every byte and the receiver can correct errors in the received bytes. The 4 received bytes are then checked for a correct CRC so corrupted Frame Heads can be rejected. If checksum A indicates that the Control Field bytes are correct, the Address (byte 1) is compared with that stored in the Device Address bits of register $C2. If a match occurs, or if the received address is '40' then an interrupt is raised indicating a valid Frame Head has been received. The Frame Head is 80 bits long (16 + 16 + {4x12}).

1.5.5.4 Data Block Coding

The Data Block follows the Frame Head and can be coded with different levels of error correction and detection. The Data Block format is controlled by Frame Head byte 2, see also section 1.6.11. Messages can take the following formats:

Type: Description:

0 Raw data, the CMX882 will transmit 16 bits at a time. In receive the device will search for the programmed 16 bit frame sync pattern and then output all following data 16 bits at a time, the host will have to perform all other data formatting. The data scrambler does not operate in this mode. This mode can be useful when interfacing to a system using a different format to those available in the CMX882.

1 Frame Head only, no User Data will be added. This format can be useful for indicating channel or user status by using byte 3 and the User Bit of the Frame Head.

2 Frame head followed by raw data. User data is appended to the Frame Head in 2 byte units with no formatting or CRC added by the CMX882. No size information is set in the Frame Head and User Data may contain any even number of bytes per Frame.

3 Frame Head followed by FEC coded data only. Each byte of the User Data has 4 bits of FEC coding added. No size information is set in the Frame Head and User Data may contain any even number of bytes per Frame. No CRC is added to the data.

4 Frame Head followed by FEC coded data with an automatic CRC at the end of the User Data. The number of User Data bytes in the Frame must be set in Frame Head byte 3. The CRC is automatically checked in the receiver and the result indicated to the host. Up to 255 bytes of User Data can be sent in each Frame using this format.

5 As per ‘4’ with the addition of all Data Block bytes being interleaved. This spreads the transmitted information over time and helps reduce the effect of errors caused by fading. Interleaving is performed on blocks of 4 bytes, the CMX882 automatically adds and strips out pad bytes to ensure multiples of 4 bytes are sent over the radio channel.

Notes:

- Message types 1, 2 and 3 have no size information requirement and do not reserve Frame Head byte 3. This byte may be freely used by the host to convey information. In message types 4 and 5 this byte must be set to the number of User Bytes in the message attached to that Frame Head ($\leq$255) to allow the receiver to correctly decode and calculate the CRC.
- Type 0 data transfers do not use frame heads. In Tx the host must transfer the bit and frame sync data before sending the message data. In Rx the host must decode all data after the frame sync.
- When using type 0 (raw data) messages it is strongly recommended that the default Frame Sync pattern is not used. This is to reduce the loading on receivers using the formatted data types which would otherwise try to decode the 6 bytes following a type 0 frame sync as a Frame Head.

Table comparing different message types:

Data Block Formatting Type:	Total over-air bits for an 80 byte message	Air time for FFSK message (ms) at 1200b/s	Air time for FFSK message (ms) at 2400b/s	Over air efficiency	Burst length protection at 1200b/s *[for 2400b/s divide both times by 2]*	Probability of detecting errors
2	720	600	300	89%	None	Zero
3	1040	867	433	62%	<0.83ms in any 10ms	Poor
4	1088	907	453	59%	<0.83ms in any 10ms	Excellent
5	1088	907	453	59%	<3.33ms in any 40ms	Excellent

Higher levels of error protection have the penalty of adding extra bits to the over air signal and this reduces the effective bit rate. Less error protection increases the effective bit rate, however in typical radio conditions the penalty is a greater risk of errors leading to repeated messages and a net reduction in effective bit rate compared to using error correction and detection.

1.5.5.5 Data Scrambling / Privacy Coding

It is preferable for MSK over air data to be reasonably random in nature to ensure the receiver can track timing using the bit changes and to smooth the frequency spectrum. To reduce the possibility of User Data causing long strings of 1's or 0's to be transmitted, a 16 bit data scrambler is provided and operates on all bits after the Frame Head.

The default (standard) setting for this scrambler is with a start code (seed) of $FFFF and any receivers with the same seed may decode this data. However, if the transmitter and receiver pre-arrange a different seed then the scrambler will start its sequence in another place and any simple receiver that does not know the transmitted seed will not be able to successfully decode the data. This method gives over 65,000 different starting points and the chance of others decoding data successfully is reduced.

The CMX882 provides the option of two custom 16 bit words that are programmable by the user in Program Register P0.2 to P0.5. Bits 0 and 1 in the Frame Head Format byte indicate which setting (standard, Seed1, Seed2 or none) the flowing Data Block has been scrambled with, see section 1.6.11. Note that a seed of $0000 will effectively turn off the scrambler and provide no protection against long sequences of 1's or 0's. Reception of scrambled data will only be successful when the receiving device has been programmed with the correct (identical) seed to that used by the transmitter.

By using this method the CMX882 provides a privacy code that will protect against casual monitoring, however the data is not encrypted and a sophisticated receiver can decode the data by using moderately simple decoding techniques. If data encryption is required it must be performed by the host. The scrambler function is controlled by bits 0,1 of the Modem Control register ($C7).

1.5.5.6 Data Buffer Timing

Data must be transferred at the rate appropriate to the signal type and data format. The CMX882 buffers signal data in up to two 16-bit registers. The CMX882 will issue interrupts to indicate when data is available or required. The host must respond to these interrupts within the maximum allowable latency for the signal type. Table 9 shows the maximum latencies for transferring signal data to maintain appropriate data throughput.

Table 9 Maximum Data Transfer Latency

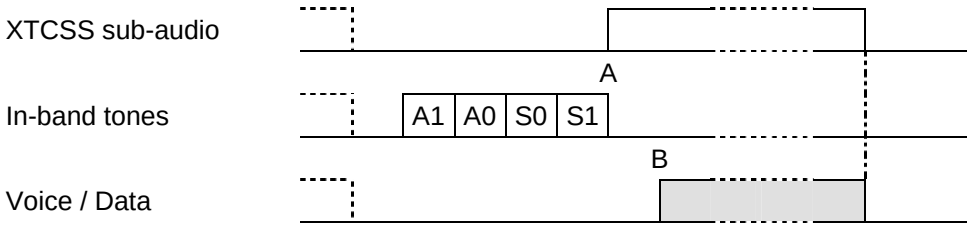
Data encoding type	Max time to read from or write to data buffer 1200b/s	Max time to read from or write to data buffer 2400b/s	Data buffer size
0	13.3ms	6.6ms	2 bytes
1	N/A*	N/A*	4 bytes
2	13.3ms	6.6ms	2 bytes
3	20ms	10ms	2 bytes
4	40ms	20ms	4 bytes
5	40ms	20ms	4 bytes

- Type 1 message is an isolated Frame Head, there is no subsequent data to load (Tx) or read (Rx).

1.5.6 XTCSS Coding

The CMX882 allows addressed calling using a 4 tone In-band tone burst followed by an optional sub-audio 'XTCSS maintenance tone' (at 64.7Hz). In transmit the CMX882 handles the transmission of the 4 tone sequence and the sub-audio tone. In receive the CMX882 will search for valid In-band tone sequences containing the previously programmed address.

The over air signalling of XTCSS is shown below:



Notes:

- To reduce 'cut on' time with XTCSS voice calls, the host can enable the receive audio path at 'B' (as soon as the 4 tone sequence is available), before the sub-audio is detected.
- XTCSS 4 tone sequences must be prefixed and suffixed with a silent 'no-tone' period of at least the length of each tone. The sequencing and timing of this function must be applied by the host µController. See also programming register P1.1.

In-band tones A1 and A0 are the BCD (binary coded decimal) representation of the Device Address bits of $C2 register, the valid XTCSS address range is 01 to 99, A0 is the least significant digit. The XTCSS address '40' is reserved for an all call address - regardless of the XTCSS address being searched for the CMX882 will always indicate when a valid 4 tone set containing address '40' has been received.

In transmit mode, the CMX882 will automatically generate the sub-audio maintenance tone, if the XTCSS maintenance tone is selected in the Audio & Device Address Control register ($C2). CTCSS must not be enabled in the Mode Control register ($C1, CTCSS Enable bit, b11 = 0). The sub-audio maintenance tone (if enabled) will automatically be output after the 4th XTCSS tone has been transmitted. An XTCSS interrupt is generated (if enabled) at point 'A' - see diagram above. The host should then wait one tone period before enabling the audio path (or transmitting data) to ensure sufficient no-tone suffix to the XTCSS 4 tone set. The host should ensure that the XTCSS transmit mode remains selected when the Voice or Data mode is enabled, to continue to transmit the XTCSS special subaudio maintenance tone. The XTCSS, Voice and Data modes must be disabled and the transmit mode turned off at the same time before initiating another transmit mode operation, such as XTCSS EOM.

To receive the XTCSS maintenance tone, CTCSS must be enabled (b11 = 1) in the Mode Control register ($C1; no special sub-audio tone selected in the Audio & Device Address Control register, $C2). When the maintenance tone is detected a CTCSS change is flagged in the Status register and the XTCSS sub-audio tone is identified in the Tone Status register.

In-band tone S0 is selected from the normal tone range of $B - $D to maintain compatibility with HSC type addressing. In-band tone S1 is selected from the normal tone range $0 - $9. The bit patterns for S0 and S1 indicate the type of information to follow according to the following tables:

In-band tone S0		
Dec	Hex	
0-10	0-$A	Reserved, do not use for S0
11	$B	Data or other silent (non-voice) call to follow, see S1a
12	$C	Voice to follow - see S1b
13	$D	Reserved, do not use for S0

In-band tone S1a				
Dec	Hex			
0-3	0-3	User option for S1a		
4	4	MSK data to follow	1200b/s	Formatted Blocks
5	5	MSK data to follow	1200b/s	Raw Data
6	6	MSK data to follow	2400b/s	Formatted Blocks
7	7	MSK data to follow	2400b/s	Raw Data
8	8	End of XTCSS coded message (EOM)		
9-13	9-$D	Reserved - do not use for S1a		

In-band tone S1b		
Dec	Hex	Voice message Compressed
0	0	No
1	1	Yes
2-13	2-$D	Reserved, do not use for S1b

Note: Tone numbers in the above tables refer to the Normal tone column as defined in Table 6.

Examples:

Device address	Over air 4 tones	Meaning
$22	34C0	Address 34, Un-compressed voice to follow
$03	03C1	Address 03, Compressed voice to follow
$2C	4EB0	Address 44, Non voice, user option 0, (E is repeat character)

Note: For all XTCSS coding the CMX882 will add (in Tx) and strip out (in Rx) the repeat tone as required. The host µC need only load or read out the normal tones listed in Table 6.

1.5.7 C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX882's internal registers and the µC over the C-BUS serial interface. Each transaction consists of a single Register Address byte sent from the µC which may be followed by one or more data byte(s) sent from the µC to be written into one of the CMX882's Write Only Registers, or one or more data byte(s) read out from one of the CMX882's Read Only Registers, as illustrated in Figure 12.

Data sent from the µC on the Command Data line is clocked into the CMX882 on the rising edge of the Serial_Clock input. Reply Data sent from the CMX882 to the µC is valid when the Serial_Clock is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an A/C byte is dependent on the value of the A/C byte. The most significant bit of the address or data are sent first. For detailed timings see section 1.8.1.

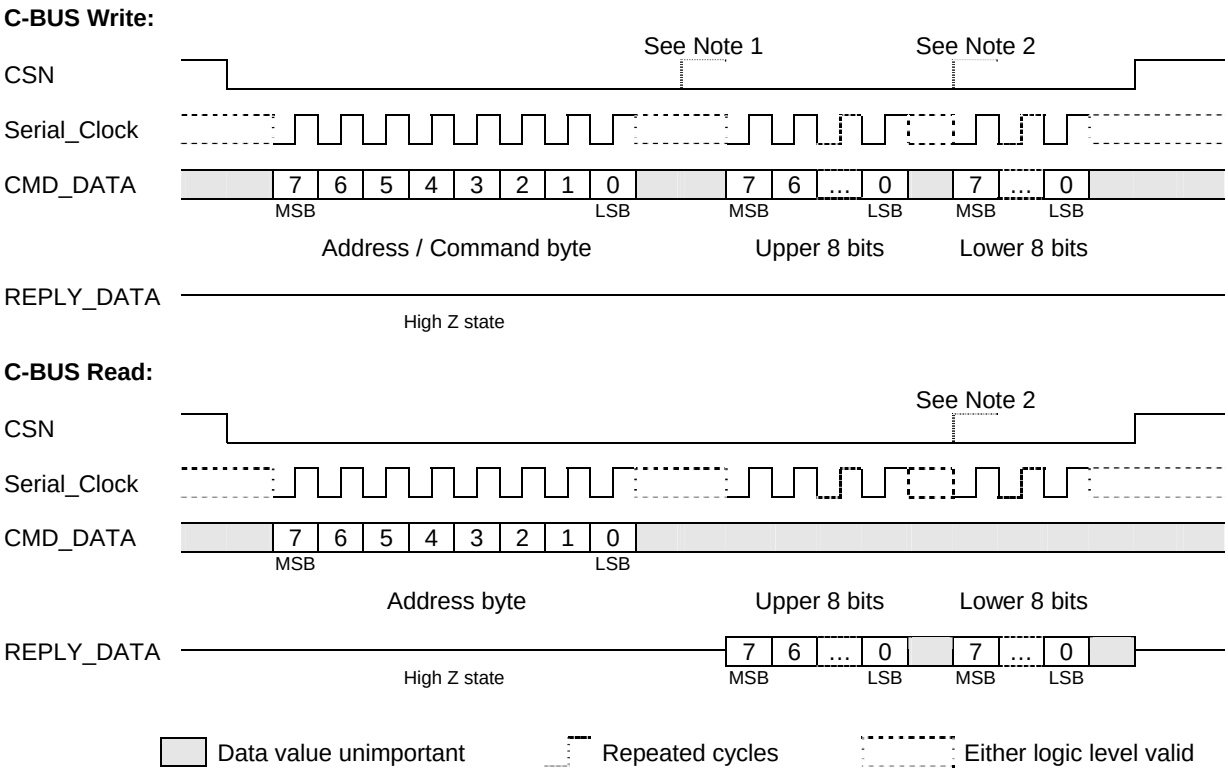


Figure 12 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CMD_DATA and REPLY_DATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The Serial_Clock input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CMD_DATA and REPLY_DATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

1.6 C-BUS Register Description

1.6.1 C-BUS Register Summary

C-BUS Write Only Registers

ADDR. (hex)	REGISTER	Word Size (bits)
$01	C-BUS RESET	0
$B0	ANALOGUE GAIN	16
$B1	SIGNAL ROUTING	16
$B2	AUXILIARY ADC THRESHOLDS	16
$B3	AUXILIARY ADC CONTROL	8
$C0	POWER DOWN CONTROL	16
$C1	MODE CONTROL	16
$C2	AUDIO & DEVICE ADDRESS CONTROL	16
$C3	TX IN-BAND TONES	16
$C7	MODEM CONTROL	16
$C8	PROGRAMMING REGISTER	16
$CA	TX DATA 1	16
$CB	XTCSS & TX DATA 2	16
$CD	AUDIO TONE	16
$CE	INTERRUPT MASK	16
$CF	RESERVED REGISTER ADDRESS	16

The C-BUS address $CF is allocated for production testing and must not be accessed in normal operation.

C-BUS Read Only Registers

ADDR (hex)	REGISTER	Word Size (bits)
$B4	AUX ADC MONITOR DATA	8
$C5	RX DATA 1	16
$C6	STATUS	16
$C9	XTCSS & RX DATA 2	16
$CC	TONE STATUS	16

Interrupt Operation

The CMX882 will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the Status register and the IRQ Mask bit (bit 15) are both set to ‘1’. The IRQ bit is set when the state of the interrupt flag bits in the Status register change from a '0' to '1' and the corresponding mask bit(s) in the Interrupt Mask register is(are) set.

All interrupt flag bits in the Status register except the Programming Flag (bit 0) are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the Status register. The Programming Flag bit is set to '1' only when it is permissible to write a new word to the Programming register.

1.6.2 $01 C-BUS RESET: address only.

The reset command has no data attached to it. It sets the device registers into the states listed below.

Addr.	REG.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$B0	ANALOGUE GAIN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B1	SIGNAL ROUTING	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B2	AUXILIARY ADC THRESHOLDS	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
$B3	AUXILIARY ADC CONTROL									0	0	0	0	0	0	0	0
$B4	AUX ADC MONITOR DATA									X	X	X	X	X	X	X	X
$C0	POWER DOWN CONTROL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C1	MODE CONTROL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C2	AUDIO & DEVICE ADDRESS CONTROL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C3	TX IN-BAND TONES	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C5	RX DATA 1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
$C6	STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C7	MODEM CONTROL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C8	PROGRAMMING REGISTER	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C9	XTCSS & RX DATA 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CA	TX DATA 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CB	XTCSS & TX DATA 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CC	TONE STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CD	AUDIO TONE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CE	INTERRUPT MASK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CF	Reserved Register Address	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Whilst the Programming Register word is cleared to zero by a general C-Bus reset, the Programming Register blocks are not initialised by general C-Bus resets. Initialisation of the Programming Register blocks is controlled by the Power Down Control register (see section 1.6.7).

1.6.3 $B0 ANALOGUE GAIN: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Inv_1	MOD_1 Attenuation			Inv_2	MOD_2 Attenuation			0	Input Gain			Audio Output Attenuation			

Bits 15 and 11 set the phase of the MOD_1 and MOD_2 outputs. When set to '0' the 'true' signal (0° phase shift) will be produced, when set to '1' the signal will be inverted (180° phase shift). This can be useful when interfacing with rf circuitry or when generating an inverted turn off tone for CTCSS. Any change will take place immediately after these bits are changed.

The output paths provide user programmable attenuation stages to independently adjust the output levels of the modulators. Finer level control of the MOD_1 and MOD_2 outputs can be achieved with the FINE OUTPUT GAIN 1 and FINE OUTPUT GAIN 2 registers (P4.2-3).

Bit 14	Bit 13	Bit 12	**MOD_1 Output Attenuation**
0	0	0	>40dB
0	0	1	12dB
0	1	0	10dB
0	1	1	8dB
1	0	0	6dB
1	0	1	4dB
1	1	0	2dB
1	1	1	0dB

Bit 10	Bit 9	Bit 8	**MOD_2 Output Attenuation**
0	0	0	>40dB
0	0	1	12dB
0	1	0	10dB
0	1	1	8dB
1	0	0	6dB
1	0	1	4dB
1	1	0	2dB
1	1	1	0dB

Bit 7 is reserved - set to 0.

Bits 6 to 4 control the input path programmable gain stage - useful when amplifying low power voice signals from the microphone inputs. Finer gain control can be achieved with the 'FINE INPUT GAIN' control register (P4.0). In receive mode it is recommended to set the gain to 0dB.

Bit 6	Bit 5	Bit 4	**Input Gain**
0	0	0	0dB
0	0	1	3.2dB
0	1	0	6.4dB
0	1	1	9.6dB
1	0	0	12.8dB
1	0	1	16.0dB
1	1	0	19.2dB
1	1	1	22.4dB

Bit 3	Bit 2	Bit 1	Bit 0	**Audio Output Attenuation**
0	0	0	0	>60dB
0	0	0	1	44.8dB
0	0	1	0	41.6dB
0	0	1	1	38.4dB
0	1	0	0	35.2dB
0	1	0	1	32.0dB
0	1	1	0	28.8dB
0	1	1	1	25.6dB
1	0	0	0	22.4dB
1	0	0	1	19.2dB
1	0	1	0	16.0dB
1	0	1	1	12.8dB
1	1	0	0	9.6dB
1	1	0	1	6.4dB
1	1	1	0	3.2dB
1	1	1	1	0dB

Bits 3 to 0 control the output path programmable attenuation stage to adjust the volume of the audio output signal. Finer volume control can be achieved with the 'FINE OUTPUT GAIN 1' control register (P4.2).

1.6.4 $B1 SIGNAL ROUTING: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	Tx MOD_1 and MOD_2 Routing		0	0	0	0	0	0	Analogue i/p select		AUDIO o/p select		Ramp Up	Ramp Down

Bits 15 and 14 reserved - set to 0.

Bits 13 and 12 select the routing of the transmit signals allowing 1 or 2 point modulation and interfaces.

Bit 13	Bit 12	**Tx MOD_1 and MOD_2 routing**
0	0	Tx, MOD_1 and MOD_2 outputs set to bias.
0	1	Tx, In band signals to MOD_1, Subaudio signals to MOD_2
1	0	Tx, In band and Subaudio to MOD_1, Subaudio signals to MOD_2
1	1	Tx, In band and Subaudio to both MOD_1 and MOD_2

To route In-band and Subaudio to MOD_1 and Vbias to MOD_2, select b13 = 1 (b12 = 0 or = 1) and set MOD_2 attenuation to >40dB in the Analogue Gain register.

'In-band' in this context refers to any of the signals; Voice, In-band tone etc.

Bits 11 to 6 are reserved - set to 0.

Bit 5	Bit 4	**Analogue Input select**
0	0	No input selected (Input = V_{BIAS})
0	1	Input amplifier 2 (Input_2 i/p)
1	0	Microphone (MIC i/p)
1	1	Discriminator (DISC i/p)

Bit 3	Bit 2	**AUDIO Output select**
0	0	No output selected (Output = V_{BIAS})
0	1	Received Voice signal
1	0	MOD_1 signal (for Tx monitoring)
1	1	Reserved, do not use

When bits 1 or 0 are set to '1' output signals are ramped up (bit 1) or ramped down (bit 0) to reduce transients in the transmitted signal. Time to ramp up / down is set in the 'Ramp Rate Control' section of the Programming register (P4.6).

1.6.5 $B2 AUXILIARY ADC THRESHOLDS: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	High Threshold [Range: 0 to 255]								Low Threshold [Range: 0 to 255]							

If the selected signal level exceeds the High Threshold, the 'Signal High' bit of the Status register will be set to 1. If the Signal level falls below the Low Threshold, the 'Signal Low' bit of the Status register will be set to 1. If the corresponding interrupt bit is enabled, a C-BUS interrupt will be generated. These status bits are cleared when the Status register is read. The behaviour of the CMX882 is not defined if the high threshold is less than the low threshold.

Threshold resolution: V_{DD}(A)/256 per LSB
Threshold accuracy: ±2 LSB
Differential linearity: ±1 LSB [monotonic]

The 'Auxiliary ADC Thresholds' register must not be updated whilst the Auxiliary ADC is enabled.

1.6.6 $B3 AUXILIARY ADC CONTROL: 8-bit write-only

Bit:	7	6	5	4	3	2	1	0
	Aux ADC i/p select		Conversion Interval					

The 'Conversion Interval' (bits 5 to 0) defines the time between measurements whilst the Auxiliary ADC is enabled. This allows the user to trade-off device power consumption with response time.

Auxiliary ADC power = $0.5mW/V_{DD}(A)$/conversion (approximate)
Conversion Interval = $20.8\mu s$ per LSB. (approximate)

The user should set an interval to ensure that no part of a received signal is missed, so that the signal type can be correctly identified. If using the Rx Auto start-up feature the recommended maximum Conversion Interval is 125µs. The 'Auxiliary ADC' register must not be updated whilst the Aux ADC is enabled.

The Aux ADC i/p select (bits 7 to 6) control the input to the Auxiliary ADC. Control is independent of the Analogue i/p select bits and hence the Aux ADC can monitor any one of the 4 inputs independently.

Bit 7	Bit 6	**Auxiliary ADC input from:**
0	0	Signal monitor (Sig_Monitor i/p)
0	1	Input amplifier 2 (Input_2 i/p)
1	0	Microphone (MIC i/p)
1	1	Discriminator (DISC i/p)

1.6.7 $C0 POWER DOWN CONTROL: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8
	Input_2 amp	MIC amp	Disc amp	Input Gain	Output Fine Gain 1	Output Fine Gain 2	O/P Coarse Gain 1	O/P Coarse Gain 2

Bit:	7	6	5	4	3	2	1	0
	Audio Output	BIAS	Signal Processing	Prog Reg Save	Disable Xtal_N	Disable Clock_Out_N	Enable Aux ADC	Rx Auto start-up

Bits 15 to 5 provide the power control of the specified blocks. If a bit is '1', the corresponding block is on, else it is powered down. A C-BUS or Power up reset clears all bits in this register to '0'.

If bit 5 is '0' the internal signal processing blocks are reset and placed into a power-save mode.

If bit 4 is clear to '0', the program registers will be reset to the default state described below whenever the Signal Processing block comes out of power save (b5 0 → 1). To preserve the current settings of the Programming register values bit 4 should be set to a '1'. Setting bit 4 to '1' prevents the Programming register values being reset when the Signal Processing block comes out of power save, such as during Rx Auto start-up. This facility should only be used if all the Programming register values have been initialised or programmed by the host μC prior to the signal processing block being put into power save.

Bits 3 and 2 control the xtal clock circuit. The xtal circuit is powered down by setting bit 3 to '1'. Note: The Clock/Xtal pin may be driven by an external clock source regardless of the setting of these bits. The Clock_Out pin is disabled (held low) by setting bit 2 to '1'. After a Power-up or C-BUS reset bits 2 and 3 are cleared to '0', so that both the xtal circuit and clock output are enabled.

Bit 1 controls the Auxiliary ADC. If set to '1' the Auxiliary ADC will generate interrupts in accordance with the settings of the interrupt mask bits. If bit 1 is '0' the Auxiliary ADC is disabled and powered down.

Bit 0 controls Rx Auto start up. If bit 0 is set to '1' and the Aux ADC input rises above the 'High Threshold' the device will automatically enter receive mode and initiate Rx signal type identification for those signals enabled in the Mode register. The correct Aux ADC input, Rx signal routing and power down bits must be set for automatic receive start up to operate, the mode control bits (b1, b0) should be set to '01' (Receive) in this case. If bit 0 is cleared to '0' the CMX882 will not automatically start-up and it is up to the host to respond to Aux ADC interrupts in this case. Bit 0 must be set to '0' whilst writing through register $C8 - Programming Register.

Initialisation of the Programming Register Blocks

Removal of the signal processing block from reset (b5 0→ 1), with b4 kept low (= 0), will cause all of the programming register words (P0 – P4) to be reset to zero, except the following:

P0.0	Frame Sync LSB	-	-	-	-	0	0	0	0	0	0	1	0	0	0	1	1
P0.1	Frame Sync MSB	-	-	-	-	0	0	0	0	1	1	0	0	1	0	1	1
P0.6	Bit Sync LSB	-	-	-	-	0	0	0	0	0	1	0	1	0	1	0	1
P0.7	Bit Sync MSB	-	-	-	-	0	0	0	0	0	1	0	1	0	1	0	1
P4.7	Transmit Limiter Control	-	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1

This initiates the device with the MSK frame sync pattern of $CB23 and bit sync of alternate 1's and 0's. The transmit limiter value is initialised to the maximum limit.

1.6.8 $C1 MODE CONTROL: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8
	Enable Voice	In band signalling: In-band tone, XTCSS		Generate Audio Tone	Enable CTCSS	Enable DCS	Enable DCS Inverse	0

Bit:	7	6	5	4	3	2	1	0
	0	0	0	Enable 2400b/s	Enable 1200b/s	0	Mode Select	

Bits 1 and 0 control the overall mode of the CMX882 according to the table below:

Bit 1	Bit 0	**Device Mode**
0	0	Idle
0	1	Receive Mode
1	0	Transmit Mode
1	1	Reserved - do not use

During transmit, only one signal type may be enabled for each of the sub-audio and voice bands, see Table 7, with the exception that "enable voice" must either be selected at all times or during transmission of audio tones or during In-band tone transmissions or during XTCSS transmissions. During receive the CMX882 will search for all signals enabled in this register and report those that are successfully decoded. See also Table 2 in section 1.5.3.

In transmit mode the CMX882 begins transmission of a selected signal immediately after it has been enabled. The host µC must ensure all associated data and control bits have been set to their required values before enabling the signal in this register.

Bits 4 and 3 control the modem functions of the CMX882 in accordance with the following table:

Bit 4	Bit 3	**Tx - Transmitted signal**	**Rx - Monitored signal(s)**
0	0	None	None
0	1	MSK 1k2b/s	MSK 1k2b/s
1	0	MSK 2k4b/s	MSK 2k4b/s
1	1	Reserved	MSK 1k2 & 2k4b/s

In transmit mode data transmission will start or finish (regardless of whether all data has been transmitted) immediately after the modem control bits are changed. To transmit a second data message the modem control bits must be set to '0', data bytes for the following message loaded, and the required bits set to '1'.

Bits 2 and 5 to 8 are reserved - set to '0'.

Bits 11 to 9 determine the sub-audio transmission / reception signalling:

Bit 11	Bit 10	Bit 9	**Tx - Transmitted signal:**	**Rx - Monitored signal(s):**
0	0	0	No Sub-Audio Transmitted	No Sub-audio Monitoring
0	0	1	Inverted DCS*	Inverted DCS*
0	1	0	DCS	DCS
0	1	1	Do not use	DCS + inv DCS*
1	0	0	CTCSS	CTCSS
1	0	1	Do not use	CTCSS + inv DCS*
1	1	0	Do not use	CTCSS + DCS
1	1	1	Do not use	CTCSS + DCS + inv DCS*

* See Table 4 DCS Modulation Modes.

Bit 12 enables Audio tone generation (see section 1.6.14). This operates in transmit and receive modes. In transmit mode this bit will only enable the Audio Generator when no other voice band signals are being transmitted i.e. bits 14, 13, 4 and 3 set to '0'.

Bits 14 and 13 select the type of In band tone to transmit or receive. When transmitting In band signals the voice path must be enabled by setting 'Enable Voice' bit 15 to '1'. To de-emphasise received in-band tones, both b15 of this register and b0 of the programming register P1.0 must be set to '1'. Note that the pre-emphasis of In-band signals other than voice is not allowed when the 'Enable Voice' bit 15 is set to '1'.

Bit 14	Bit 13	**Tx - Transmitted signal**	**Rx - Monitored signal**
0	0	No voice band tone transmitted	No voice band tones monitored
0	1	In-band tone	In-band tone
1	0	Reserved	Reserved
1	1	XTCSS	XTCSS

When set to '1', bit 15 enables the voice path. In transmit mode the selected audio input is routed to the modulator outputs. In transmit mode bit 15, if set to '1', will be temporarily disabled (cleared to '0') whenever any of the bits 3, 4, 12, 13 and 14 are set to '1'. In receive mode the voice processing path is enabled to the audio output. In receive mode bit 15, if set to '1', will be temporarily disabled (cleared to '0') whenever bit 12 is set to '1'. It is up to the host µC to control bit 15 when voice band signals are received. Bits 15, 14 and 13 should not be enabled in the same command instruction.

When in receive mode, if Voice is enabled and In-band tone detection is also selected, the voice processing quality (SINAD) is reduced. A 350µs delay must be inserted between enabling Voice and Selcall tone detection.

The Mode Control register ($C1) may be written to at any time (subject to C-BUS timing restrictions). If the enable bit of the currently decoded signal is cleared, the decoder is turned off. If it is subsequently re-enabled, the decoder will enter the appropriate signal acquisition phase.

The CMX882 will only detect signals when their amplitude is above the threshold set for each band (sub-audio and voice), as set in the program registers. Therefore even if valid tones or signals are present the CMX882 will ignore them unless they exceed the detect threshold. Time and level hysteresis is applied to reduce chattering in marginal conditions.

Detection strategies used by the CMX882 whilst in receive mode:
When in receive mode the CMX882 treats the received signal in two bands; Sub-audio (60-260Hz) and voice band (300-3kHz). For the sub-audio the CMX882 can monitor and decode CTCSS and DCS signals in parallel. Because certain FFSK bit patterns can mimic some In-band tones the In-band receiver is temporarily disabled when an FFSK frame sync is detected. If using sized packets (type 1, 4 and 5) the CMX882 will automatically restore In-band tone detection when the received message has ended. If using unsized packets (type 0, 2 and 3) the host must monitor the received data and restore XTCSS / In-band tones (by setting bits 14 and 13 as required) when it has detected the end of data.

Configuring the CMX882 for Automatic Receive Start-Up
Prior to setting the CMX882 into Automatic Receive Start-Up mode, the Mode Control register should be clear (Tx and Rx modes disabled). Set up the Programming Register blocks as required. Write to the Powerdown Control register with the appropriate functions enabled or disabled, including Signal Processing bit clear (b5 = 0), Prog Reg Save bit set (b4 = 1) and the Rx Auto Start-Up bit set (b0 = 1). While the Signal Processing block is in its powersave condition, the Mode Control register should be set up for the appropriate signalling schemes to be processed and Rx mode selected (b1 = 0, b0 = 1). When auto start-up is triggered, the signal processing bit in the Powerdown Control register will automatically be set (= 1) and the selected receiver processing will start.

Configuring and Changing Transmit or Receive Modes
Bits 15-9 and 4,3 select the device function and bits 1,0 select the mode, transmit (TX), receive (RX) or IDLE. When IDLE mode is selected, all the function bits should also be cleared to '0' by the host. If a mode change places the device into IDLE mode, at least 350 µs should elapse before changing the device again into an active mode (RX or TX). It is possible to transition between RX and TX modes without going through the IDLE mode.

All the Programming register words must be configured as required, in accordance with the procedures defined in section 1.6.20, whilst the Mode Control register ($C1) is set in IDLE mode.

In RX mode, concurrent signalling schemes are allowed, as described in section 1.5.3. Receive functions can be switched on or off at any time while in receive mode, by setting or clearing their respective enable bits in the Mode Control register.

In TX mode, only up to one of the in-band signalling schemes, plus "enable voice", and only up to one of the sub-audio signalling schemes should be selected, as described in section 1.5.4, table 7. The combination of XTCSS and voice is allowed, but only while the XTCSS function is transmitting the sub-audio maintenance tone, as described in section 1.5.6.

Special consideration is needed when changing from one in-band TX function to another whilst remaining in TX mode. To effect the change, set the current function to transmit a null signal, adjust settings for the next function as required, wait for at least 350µs, then select the new function and turn off the current function by writing to the Mode Control register with the current function enable bit cleared and the new function enable bit set.

- To select a null TX voice signal function, set Signal Routing register ($B1) bits 5,4 = 0,0.
- To select a null TX in-band tone signal function, clear Tx In-Band Tones register ($C3) = 0.
- Transmissions of XTCSS tones sequences end in null in-band signals, unless voice is later enabled while the sub-audio maintenance tone is on, so no specific action is needed to select a null XTCSS signal.
- To select a null TX MSK signal function, set Modem Control register ($C7) bit 9 = 1, as described in section 1.5.5.
- To start a new MSK data packet it is necessary to toggle between the MSK TX mode and IDLE mode or, if CTCSS or DCS require to be maintained, toggle between the MSK TX and null voice or null in-band tone TX.

CTCSS sub-audio transmission is turned off by putting the device into IDLE mode (Mode Control register = 0) [or by setting the Audio & Device Address register bits 7-0 = 0, to select CTCSS No Tone]. DCS transmission is normally ended by applying the special DCS turn-off tone. To turn off the special sub-audio DCS turn off tone, put the device into IDLE mode [or set the Audio & Device Address register bits 7-0 = 0 and select CTCSS].

Some configurations of the Audio & Device Address register ($C2), Modem Control register ($C7) and the TX Data registers ($CA & $CB) are decoded by the device at the start of the function's operation, so they must be set up before selecting the function in the Mode Control register.

Configuration features	Register & Bits	Action to instigate configuration change
Voice filter, emphasis, compand and scramble	$C2, bits 14-10	Decode triggered by entering Voice mode from IDLE mode or from another function mode.
In-band tone or XTCSS using Pre-/De-Emphasis	$C2, bit 10	Decode triggered by entering the in-band signalling mode from IDLE mode or from another function mode.
Device decode address	$C2, bits 7-0	Decode triggered by selecting CTCSS, XTCSS and/or MSK RX mode or XTCSS TX mode. Decode of transmitted CTCSS tones is continuous in TX mode.
MSK modem tx functions	$C7, bits 10, 7-0	Decode triggered by selecting MSK RX or TX mode.
MSK tx Frame Head data	$CA	
MSK modem rx functions	$C7, bit 10	
XTCSS tx codes	$CB	Decode triggered by entering the XTCSS signalling mode from IDLE mode [or from another function mode].

In the case of MSK transmit functions, the data register(s) must be updated with new data as described in sections 1.5.5 and 1.6.13. Subsequent changes to the other configurations defined above will only take effect when the relevant operation is re-started from IDLE mode or by switching to another mode. Voice compand and scramble bits should not be changed while the voice function is operating.

Changes to other registers and configuration bits are permitted at any time, as appropriate. Normally the device will be configured prior to selecting the transmit or receive mode in the Mode Control register.

1.6.9 $C2 AUDIO & DEVICE ADDRESS CONTROL: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	Scramble	Compand	Voice filter mode			Special Sub-Audio		Device Address							

Bits 7 to 0 define the device address. This setting is used for the CTCSS and XTCSS address in both Tx and Rx modes and as the receive MSK frame head address. The range of valid addresses is: CTCSS tone (1-51 in decimal), MSK address (1-255 in decimal) and XTCSS (1-99 in decimal).

In Tx the device address is used to select the addressing of the enabled XTCSS or CTCSS signalling scheme. If the address is outside the valid range no signalling will occur. The device address must be asserted before selecting XTCSS transmit mode. In CTCSS transmit mode, decoding of the device address is continuous, so changing the device address will cause the transmitted CTCSS tone to change accordingly.

In Rx the device address (along with the all-call address of '40') will be searched for each signalling format enabled in the Mode register. The detected signal type will be reported in the Status register $C6 and the address will be indicated in the appropriate Rx Data register $C5 or $C9, or the Tone Status register $CC. The device address must be asserted before selecting any receive mode that relies on this address.

Bits 9 to 8 select special sub-audio tones in accordance with the following table.

Bit 9	Bit 8	**Freq (Hz)**	**Special Sub-Audio tone**
0	0	-	None
0	1	134.4	DCS turn off tone
1	0	64.7	XTCSS maintenance tone (Tx Only)
1	1	Clone	CTCSS Tone clone mode (Rx only)

- Selecting the 'DCS turn off tone' during DCS transmit will cause the DCS turn off tone to be transmitted; this will override the DCS data being transmitted. Select 'DCS turn off tone' in this register to enable detection of the DCS turn off tone during receive. CTCSS must be enabled in the Mode Control register to receive the 'DCS turn off tone'.
- To transmit the 64.7Hz XTCSS maintenance tone, XTCSS transmit must be selected in the Mode Control register and XTCSS maintenance tone must be selected in this register. Transmission of the maintenance tone overrides any other CTCSS tone being transmitted. The XTCSS maintenance tone decoder is enabled by selecting XTCSS and CTCSS receive modes in the Mode Control register, so it is not necessary to select the XTCSS maintenance tone in this register when receiving.
- If the Tone Clone™ mode is selected this allows the device in Rx to non-predictively detect any CTCSS frequency in the range of valid tones, the received tone number will be reported in the Tone Status register $CC. The narrowest bandwidth should be selected in Programming Register word P2.1.

The voice filter control bits 12 and 11 determine the Voice Band Filter mode applied to the voice signal before it is transmitted or after it has been received. Bit 10 controls the de-emphasis (Rx) or pre-emphasis (Tx) mode of the voice band filtering.

Bit 12	Bit 11	Bit 10	**Voice filter mode**
X	X	0	Disable de/pre-emphasis
X	X	1	Enable de/pre-emphasis
0	0	X	No filtering applied
0	1	X	In transmit mode: HPF (to remove SA) + 12.5kHz channel filtering In receive mode: HPF (to remove SA) + Low pass filter
1	0	X	In transmit mode: HPF (to remove SA) + 25.0kHz channel filtering In receive mode: HPF (to remove SA) + Low pass filter
1	1	X	Reserved – do not use

Bit 13 controls the audio band compandor. When set to '1' audio band signals are compressed in transmit mode and expanded in receive mode. When set to '0' no companding is performed.

Bit 14 controls the audio band scrambler. When set to '1' voice signals are scrambled, by frequency inversion, in transmit and receive modes. When set to '0' no scrambling is performed.

The settings of bits 10 to 14 must be asserted before voice Tx or Rx mode is selected. To change the operating modes controlled by these bits, the Tx or Rx operation must be turned off, then after the appropriate period (see section 1.6.8), apply the changes to this register and turn on the new mode in the Mode Control register.

Bit 15 is reserved, set to '0'.

1.6.10 $C3 Tx In-Band Tones: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tx In-band tone					0	0	0	0	0	0	0	0	0	0	0

Bits 15 to 11 define the tone transmitted when Tx In-band tone is enabled. The frequency is as defined in Table 6, In-band Tones.

Bits 10 to 0 are reserved, set to '0'.

1.6.11 $C7 Modem Control: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	Type 0 format	Last Tx data	0	MSK message format			0	0	User bit	Scramble seed	

This register configures the way the CMX882 handles MSK data in both transmit and receive.

Bits 15 to 11, 8, 4 and 3 are reserved, set to '0'.

Bit 10 sets the raw data mode when set to '1'. When set to '0' the built in data packeting is enabled. The way this bit is set determines how the CMX882 handles new data when in transmit or receive modes:

Bit 10, Receive mode:

- If Bit 10 is '1' the device will look for the programmed Frame Sync. pattern, raise an interrupt (if enabled) and decode the following data 16 bits at a time, making them available in register $C5.
- If Bit 10 is '0' the device will look for a complete Frame Head before raising an interrupt (if enabled) and then decode the following data in accordance with the received message format. The Frame Head Control Field bytes, User Data and any CRC will be presented in registers $C5 and $C9.

Bit 10, Transmit mode:

- If Bit 10 is '1' the device will transmit data 16 bits at a time from register $CA. Bit and frame sync pattern generation and all formatting of the data have to be performed by the host in this case.
- If Bit 10 is '0' the device will transmit the programmed bit and frame sync patterns followed by a Frame Head containing the information supplied in bits 7–0 of this register and the 2 bytes in register $CA. Subsequently the host must supply data when requested to complete the transmission of the data packet as defined in the Frame Head bytes.

The state of bit 10 must not be changed while the device is operating in MSK mode.

Bit 9 is only valid when transmitting data with type 0, 2 or 3 formatting and indicates to the CMX882 that it can cease modulation. The host must set this bit to '1' immediately after the interrupt for 'load more data' occurs. In receive, or when transmitting other message formats, this bit must be set to '0'.

When bit 10 = '0' bits 7-0 control the format and coding used for MSK messages: (See also section 1.5.5.)

Bits 7 to 5 control the data formatting used by the CMX882 in transmit and receive:

Bit 7	Bit 6	Bit 5	Type	**Message format:**
0	0	1	1	Frame Head only, no payload
0	1	0	2	Frame Head + Unsized payload of raw 16 bit words
0	1	1	3	Frame Head + Unsized payload with FEC
1	0	0	4	Frame Head + Sized payload with FEC + CRC
1	0	1	5	Frame Head + Sized payload with FEC + CRC + interleaving
All other patterns			-	Reserved

Bit 2 is a User bit and may be freely used by the host. This bit has no effect on the message format or encoding and will be reported in the Rx Data register for the receiving host to use as appropriate. This bit could be used to indicate a special message, e.g. one containing handset or channel set-up information.

Bits 1-0 select the data scrambler seed used when transmitting User Data. The receiving CMX882 will automatically de-scramble the received User Data using the setting indicated in the received Frame Head. The receiving host can read the scrambler setting (0-3) used by the transmitter via register $C9 and may use this when returning messages. See also section 1.5.5.5.

Bit 1	Bit 0	**MSK data scrambling setting:**
0	0	Standard scrambling (seed = $FFFF)
0	1	Scramble Seed1 (see P0.2-3)
1	0	Scramble Seed2 (see P0.4-5)
1	1	No scrambling (seed = $0000)

1.6.12 $C8 PROGRAMMING REGISTER: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	First Word	Block Number	Block / Data		Programming Data											

See section 1.6.20 for a description of this register.

1.6.13 $CA and $CB TX DATA & XTCSS Codes: 2 x 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$CA	Tx MSK Data Byte 0 (Frame Head: Address byte)								Tx MSK Data Byte 1 (Frame Head: Size / Information byte)							
$CB*	Tx Data Byte 2*								Tx Data Byte 3*							
	XTCSS Tone 3 (S1)				XTCSS Tone 2 (S0)				0	0	0	0	0	0	0	0

*Register $CB is only used for Type 4 and 5 data formats and Frame Heads, the Tx buffer is effectively 4 bytes long in these cases.

These 2 words hold next 2 bytes (Byte 0 and 1) or 4 bytes (Bytes 0, 1, 2 and 3) of MSK data to be transmitted. Outgoing data is continuous, if new data is not provided before the current data has been transmitted the current data will be re-transmitted, until new data is provided. Transmission of current data will be completed before transmission of newly loaded data begins. See section 1.5.5.6.

$CB holds the codes to be used when transmitting an XTCSS type tone set. Each 4 bits define the In-band tone used, see Table 6, In-band Tones. S0 and S1 are the information section of the 4 tone set. This register must be set to the required value before XTCSS transmission is enabled. For more details see section 1.5.6. Note: the XTCSS address used is defined in the Audio and Device Address Control register.

Although $CB holds both Tx data and Tx XTCSS tone information, these functions can not be used simultaneously so no conflict will occur.

When transmitting formatted MSK data packets the host must first load the correct Address and Size / Information bytes for the following packet into register $CA. The CMX882 will automatically add the Control byte (based on the settings in register $C7) and calculate the Frame Head Checksum A byte. The CMX882 will read the Size and Message formatting information and automatically format all following data; adding error correction bytes, adding pad bytes, interleaving, scrambling and calculating and appending Checksum B as required. The only task the host need perform during the transmission of a Frame is to download new data when it is required.

Note: These 2 words must be written separately. i.e. Two 16 bit C-BUS transactions.

1.6.14 $CD AUDIO TONE: 16-bit write only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	Audio Tone											

When the required bits of the Mode Control register ($C1) are set an audio tone will be generated with the frequency set by bits (11-0) of this register in accordance with the formula below. If bits 11-0 are programmed with '0' no tone (i.e. Vbias) will be generated when the Audio Tone is enabled.

frequency = Audio Tone (i.e. 1Hz per LSB)

The Audio Tone frequency must only be set to generate frequencies from 300Hz to 3000Hz.

The host must suppress other voice band signalling and set the correct audio routing before generating an audio tone and re-enable signalling and audio routing on completion of the audio tone. The timing of intervals between these actions is also controlled by the host μC.

This register may be written to whilst the audio tone is being generated, any change in frequency will take place after the end of the C-BUS write to this register. This allows complex sequences (e.g. ring or alert tunes) to be generated for the local speaker (Tx or Rx via the AUDIO pin) or transmitted signal (Tx via the MOD1/2 pins).

1.6.15 $CE INTERRUPT MASK: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8
	IRQ MASK	0	Rx In-band detect MASK	XTCSS MASK	Rx CTCSS detect MASK	Rx DCS detect MASK	Aux ADC High MASK	Aux ADC Low MASK

Bit:	7	6	5	4	3	2	1	0
	FFSK end MASK	Data transfer MASK	0	Rx 2400b/s detect MASK	Rx 1200b/s detect MASK	0	0	Prog Flag MASK

Bit	Value	Function
15	1	Enable selected interrupts
	0	Disable all interrupts (IRQN pin not activated)
14		Reserved – Set to 0
13	1	Enable interrupt when a change to a In-band tone is detected as indicated by a '0' to '1' change of bit 13 of the Status register
	0	Disabled
12	1	Enable interrupt when a valid XTCSS 4 tone set is detected or has finished being transmitted as indicated by a '0' to '1' change on bit 12 of the Status register
	0	Disabled
11	1	Enable interrupt when a change to a programmed CTCSS tone is detected as indicated by a '0' to '1' change of bit 11 of the Status register
	0	Disabled
10	1	Enable interrupt on a change in the detect status of the DCS decoder as indicated by a '0' to '1' change of bit 10 of the Status register
	0	Disabled
9, 8	1	Enable interrupt when the corresponding Aux ADC status bit changes
	0	Disabled
7	1	Enable interrupt when FFSK data transmission has ended
	0	Disabled
6	1	Enable interrupt when an FFSK data transfer is required
	0	Disabled
5		Reserved - Set to 0
4	1	Enable interrupt when valid 2400b/s data is detected
	0	Disabled
3	1	Enable interrupt when valid 1200b/s data is detected
	0	Disabled
2, 1		Reserved - Set to 0
0	1	Enable interrupt when Prog Flag bit of the Status register changes from '0' to '1' (see Programming register $C8)
	0	Disabled

The following 5 registers (including 2 receive data registers) are read only

1.6.16 $B4 AUX ADC MONITOR DATA: 8-bit read-only

Bit:	7	6	5	4	3	2	1	0
	Signal Monitor Data							

This data holds the result of the last measurement performed by the auxiliary ADC. The signal processor must be on to read Aux ADC data, so Power Down Control register b5 must be set to '1'. This is independent of whether Tx or Rx modes are selected.

1.6.17 $C6 STATUS: 16-bit read-only

Bit:	15	14	13	12	11	10	9	8
	IRQ	0	In-band tone state change	XTCSS 4 tone set complete	CTCSS state change	DCS state change	Aux ADC Monitor High	Aux ADC Monitor Low

Bit:	7	6	5	4	3	2	1	0
	End of FFSK data	FFSK data transfer required	Block CRC error	Rx 2400b/s	Rx 1200b/s	0	0	Programming Flag

This word holds the current status of the CMX882: the value read out is only valid when bit 5 of the Power Down Control register ($C0) is set to '1'. Changes in the Status register will cause the IRQ bit (bit 15) to be set to '1' if the corresponding interrupt mask bit is enabled. An interrupt request is issued on the IRQN pin when the IRQ bit is '1' and the IRQ MASK bit (bit 15 of register $CE) is set to '1'.

Bits 1 to 15 of the Status register are cleared to '0' after the Status register is read. Bit 0 is only cleared by writing to the Programming Register.

Bits 14 and 2 to 1 are reserved.

Bits 13, 11 and 10 indicate that a In-band tone, CTCSS or DCS event caused the interrupt, the host should then read the Tones Status register ($CC) for further information. In transmit these bits will be set to '0'. Detection of the DCS turn off tone and removal of the DCS turn off tone are both flagged as DCS events in the Status register, not as CTCSS events. The assertion or removal of the 'XTCSS Maintenance Tone' (64.7Hz) is flagged as a CTCSS event.

In receive bit 12 indicates that a valid XTCSS 4 tone set with the correct addressing (see $C2) has been detected, the 4 received tones are indicated in $C9. In Tx mode bit 12 will be set to '1' at the end of the 4th XTCSS tone transmitted.

Aux ADC High (bit 9) and Aux ADC Low (bit 8) reflect the recent history of the Aux ADC level, with respect to the high and low thresholds. The most recent Aux ADC reading can be read from $B4.

Aux ADC Monitor High	Aux ADC Monitor Low	**Aux ADC history since last reading:**
0	0	Neither threshold crossed
0	1	Signal gone below low threshold
1	0	Signal gone above high threshold
1	1	Signal gone below low threshold and above high threshold

In Rx mode bit 7 will be set at the same time as bit 6 after receiving the last part of a sized FFSK Frame or Type 1 (frame head only) message, bit 5 (CRC) will also be updated at this time. When the host detects bit 7 is set it may power down the CMX882 or set the CMX882 to transmit or receive new information as appropriate.

In Tx mode bit 7 will be set when the last bit of FFSK data has been transmitted. Note; when using type 0, 2 or 3 data formats (see section 1.5.5.4) this bit will only be set if bit 9 of the Modem Control register

($C7) is set at the appropriate time. After allowing a short time delay associated with the external components and radio circuitry, the host may power down the CMX882 and transmitter or set the CMX882 to transmit or receive new information as appropriate.

Bit 6 indicates that new transmit data is required (in Tx mode) or received data is ready to be read (in Rx mode). For continuous transmission or reception of information, a data transfer should be completed within the time appropriate for that data (see Table 9).

Bit 5 will be set after receiving the CRC portion of a sized Data Block (types 4 and 5) and will be set to '0' when the locally calculated CRC indicates the received data has no errors.

Bits 4 and 3 indicate the received data rate after a valid data sequence has been received. If data Type 0 formatting is enabled these bits will be set on detection of a valid frame sync pattern. If Type 0 formatting is disabled then these bits will only be set when a Frame Head is detected with a correct CRC.

Rx 2400b/s	Rx1200b/s	**Bit rate of detected valid data:**
0	0	No data
0	1	1200b/s
1	0	2400b/s
1	1	Reserved

Programming Flag, bit 0: The Programming Register ($C8) should only be written to when bit 0 is set to '1' (with both Mode select bits set low – See register $C8). Writing to the Programming Register ($C8) clears bit 0 to '0'. Bit 0 is restored to '1' when the programming action is complete, normally within 250µs**,** when it is then safe to write to the Programming Register.

1.6.18 $C5 and $C9 RX DATA: 2 x 16-bit read-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$C5	Rx Data Byte 0 (Frame Head: Address byte)								Rx Data Byte 1 (Frame Head: Format byte)							
$C9	Rx Data Byte 2* (Frame Head: Size / Information byte)								Rx Data Byte 3* (Frame Head: CRC byte)							
	XTCSS Tone 3 (S1)				XTCSS Tone 2 (S0)				XTCSS received address							

*$C9 is used when receiving Type 4 and 5 formats and Frame Heads, the Rx buffer is effectively 4 bytes long in these cases.

These 2 words hold the most recent 2 bytes (Byte 0 and 1) or 4 bytes (Bytes 0, 1, 2 and 3) of MSK data decoded. Received data is continuous, if the data is not read before the next data is received the current data will be over-written.

$C9 holds the information decoded after receiving an XTCSS type tone set. Bits 7 to 0 represent the received address in hex based on the XTCSS tones A1 and A0. This register will only be updated if the received address matches the one programmed in the Audio and Device Address Control register or is the all call address of '40'. Bits 15 to 12 and 11 to 8 defines the received S1 and S0 tones, see Table 6 and section 1.5.6.

Although $C9 holds both Rx data and Rx XTCSS tone information, only one type of signal will be present in the received signal at any one time so no conflict will occur.

After receiving a Frame Head the host can read the Frame Head Size / Information and Frame Head Checksum A bytes for the following packet from $C5 and the Address byte and the Control byte from $C9. The CMX882 will read the Size and Message formatting information and if the message is of type 3, 4 or 5 (see section 1.5.5.4) it will set the automatic decoding of the following data; descrambling, de-interleaving, decoding error correction bytes, stripping out pad bytes, calculating and checking Checksum B as required. The only task the host need perform during the reception of formatted Frames is to read out data when it is ready.

Note: These 2 words must be read separately. i.e. Two 16 bit C-BUS transactions.

1.6.19 $CC TONES STATUS: 16-bit read-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Detected Selcall tone frequency					Sub-Audio Status			0	0	Detected CTCSS code					

This word holds the current status of the CMX882 sub-audio and In-band tone sections. This word should be read by the host after an interrupt caused by a DCS, CTCSS or In-band tone event.

The value in bits 5 to 0, Detected CTCSS code, identifies the detected sub-audio tone by its position in Table 3 CTCSS Tones. If bits 5 to 0 = '000000' there is no CTCSS tone currently being detected. If bits 5 to 0 = '110111' (= 55 in decimal) this indicates that an Invalid Tone has been detected. An Invalid Tone is any tone in the subaudio band which is not the selected subaudio tone nor the all-call tone, or is a tone not listed in Table 3. A change in the state of bits 5-0 to Invalid Tone from the no tone condition will not cause Status register ($C6), b11 to be set to '1'. Any other change in the state of bits 5-0 will cause the Status register ($C6), b11 to be set to '1'.

A detected In-band frequency is indicated by the value in bits 15 to 11, 'Detected In-band tone frequency', identifies the frequency by its position in Table 6, In-band Tones. If bits 15 to 11 = '00000' there is no In-band tone currently being detected. A change in the state of bits 15 to 11 will cause bit 13 of the Status register ($C6), 'In-band State Change', to be set to '1', unless the change is between Unrecognised Tone and No Tone.

Bits 10 to 8 indicate the DCS and special sub-audio tone status. The Status register ($C6) will indicate the type of signal detected. If DCS or special CTCSS tones are detected they will be indicated in bits 10 to 8 according to the table below and bits 7 to 0 will be set to '00000000'. If a normal CTCSS tone is detected bits 10 to 8 will be set to '000' and bits 7 to 0 will indicate the decoded tone. A change in the state of bits 10 to 8 will cause the relevant bit (10 or 11) of the Status register to be set to '1'.

Bit 10	Bit 9	Bit 8	**Sub-Audio status**	
0	0	0	No DCS or special CTCSS detected	
0	0	1	Reserved	
0	1	0	DCS sequence detected	Only enabled with DCS
0	1	1	inverted DCS sequence detected	Only enabled with DCS
1	0	0	Reserved	
1	0	1	134.4Hz DCS turn off tone detected	Only enabled with DCS
1	1	0	64.7Hz XTCSS sub-audio tone detected	Only enabled with XTCSS
1	1	1	Reserved	

When the relevant detection mode is not enabled, the associated bits will be set to '0'. In Tx mode this register will be set to '0'.

During DCS receive, the device can flag an interrupt when the DCS code fails to be recognised. This may be due to code dropout. The turn off tone may be flagged shortly after, if the transmission is ending. Alternatively the DCS link may be restored and DCS detection will be flagged again.

1.6.20 $C8 PROGRAMMING REGISTER: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	First Word	Block Num.	Block Num. or Data		Programming Data											

This register is used for programming various gains, levels, offset compensations, tones and codes. The programmed values are initialised in accordance with the settings described in section 1.6.7 (Power Down Control), when the signal processing block is taken out of reset and the Prog Reg Save bit is clear (= 0).

The Signal Processing function and the XTAL clock circuit must both be enabled in order to write to the Programming Register, so Power Down Control register bit 5 must be set to '1' and bit 3 must be set to '0'. All other interrupt sources should be disabled while loading the programming register blocks.

The Programming Register should only be written to when the Programming Flag bit (bit 0) of the Status register is set to '1' and the Rx and Tx modes are disabled (bits 0 and 1 of the Mode Control register both '0'). The Programming Flag is cleared when the Programming Register is written to. When the corresponding programming action has been completed (normally within 250μs) the CMX882 will set the flag back to '1' to indicate that it is now safe to write the next programming value. The Programming Register must not be written to while the Programming Flag bit is '0'. Programming is done by writing a sequence of 16-bit words to the Programming Register, in the order shown in the following tables. Writing data to the Programming Register must be performed in the order shown for each of the blocks, however the order in which the blocks are written is not critical. If later words in a block do not require updating the user may stop programming that block when the last change has been performed. e.g. If only 'Fine output gain 1' needs to be changed the host will need to write to P4.0, P4.1 and P4.2 only.

The user must not exceed the defined word counts for each block. The word P4.8 is allocated for production testing and must not be accessed in normal operation.

The high order bits of each word define which block the word belongs to, and if it is the first word of that block:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11 – Bit 0
1	X	X	X	1st data for each block
0	X	X	X	2nd and following data
X	1	0	0	Write to block 0 (12 bit words)
X	1	0	1	Write to block 1 (12 bit words)
X	1	1	0	Write to block 2 (12 bit words)
X	1	1	1	Reserved - do not use
X	0	Write to		block 4 (14 bit words)

Block 0 – Modem Configuration:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0.0	1	1	0	0	0				MSK Frame Sync LSB							
P0.1	0	1	0	0	0				MSK Frame Sync MSB							
P0.2	0	1	0	0	0				Scramble Seed 1 LSB							
P0.3	0	1	0	0	0				Scramble Seed 1 MSB							
P0.4	0	1	0	0	0				Scramble Seed 2 LSB							
P0.5	0	1	0	0	0				Scramble Seed 2 MSB							
P0.6	0	1	0	0	0				MSK Bit Sync LSB							
P0.7	0	1	0	0	0				MSK Bit Sync MSB							

Block 1 – XTCSS and In-band tone Setup:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.0	1	1	0	1	Audio band Tx level											Emph
P1.1	0	1	0	1	XTCSS tone length		Audio band detect threshold						In-band tone detect bandwidth			
P1.2	0	1	0	1	0	Programmable In-band Tone 0										
P1.3	0	1	0	1	0	Programmable In-band Tone 1										
P1.4	0	1	0	1	0	Programmable In-band Tone 2										
P1.5	0	1	0	1	0	Programmable In-band Tone 3										

Block 2 – CTCSS and DCS Setup:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.0	1	1	1	0	CTCSS and DCS Tx level											
P2.1	0	1	1	0	DCS 24	0	CTCSS and DCS detect threshold						CTCSS detect bandwidth			
P2.2	0	1	1	0	DCS Code bits 11 – 0											
P2.3	0	1	1	0	DCS Code bits 23/22 – 12											
P2.4	0	1	1	0	Sub-audio drop out time				0							

Block 3 – Reserved. Do not use.

Block 4 – Gain and Offset Setup:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.0	1	0	Fine Input Gain													
P4.1	0	0	Reserved - set to '0'													
P4.2	0	0	Fine Output Gain 1													
P4.3	0	0	Fine Output Gain 2													
P4.4	0	0	Output 1 Offset Control													
P4.5	0	0	Output 2 Offset Control													
P4.6	0	0	Ramp Rate Control													
P4.7	0	0	Limiter Setting (all 1's = Vbias +/- 0.5 Vdd)													
P4.8	0	0	Special Programming Register (Production Test Only)													

1.6.20.1 PROGRAMMING REGISTER Block 0 – Modem Configuration:

$C8 (P0.0-1) MSK Frame Sync

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0.0	1	1	0	0	0				MSK Frame Sync LSB							
P0.1	0	1	0	0	0				MSK Frame Sync MSB							

Bits 7 to 0 set the Frame Sync pattern used in Tx and Rx MSK data. Bit 7 of the MSB is compared to the earliest received data. After a power on or C-BUS reset they are set to $CB23.

$C8 (P0.2-5) Scramble Seed 1 and 2

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0.2	0	1	0	0	0				Scramble Seed 1 LSB							
P0.3	0	1	0	0	0				Scramble Seed 1 MSB							
P0.4	0	1	0	0	0				Scramble Seed 2 LSB							
P0.5	0	1	0	0	0				Scramble Seed 2 MSB							

These bits set the scramble seed used on all data bits following a Frame Head. If $0000 is programmed as the seed then no scrambling will occur when selected. If either programmable scramble seeds are selected, both the transmit and receive devices must use the same seed pattern for data to be transferred correctly.

$C8 (P0.6-7) MSK Bit Sync

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0.6	0	1	0	0	0				MSK Bit Sync LSB							
P0.7	0	1	0	0	0				MSK Bit Sync MSB							

This bit pattern is used when transmitting the bit sync portion of a Frame Head. After a power on or C-BUS reset they are set to $5555 (‘0101…0101’), if Powerdown Control bit 4 is clear when signal processing is enabled (See section 1.6.7).

1.6.20.2 PROGRAMMING REGISTER Block 1 – XTCSS and In-band tone Setup:

$C8 (P1.0) Voice band tones Tx Level

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.0	1	1	0	1	Voice band tones Tx level											Emph

Bits 11 (MSB) to 1 (LSB) set the transmitted In-band tone, Audio Tone and MSK signal level (pk-pk) with a resolution of $V_{DD}(A)/2048$ per LSB (1.465mV per LSB at $V_{DD}(A)$=3V). Valid range for this value is 0 to 1536.

Bit 0 controls Rx In-band tone de-emphasis. When set to '0' the signal going to the In-band tone detector is not de-emphasised. When voice processing is enabled in the Mode register, de/pre-emphasis is enabled in the Audio & Device Address register and this bit (b0) is set to '1', signals going to the In-band tone detector are de-emphasised in accordance with Figure 6.

$C8 (P1.1) In-band tone Detect Bandwidth and Audio Band Detect Threshold

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.1	0	1	0	1	XTCSS tone length		Audio band detect threshold						In-band tone detect bandwidth			

XTCSS tone length (bits 11, 10): '00' = 40ms, '01' = 60ms, '10' = 80ms and '11' = 100ms.

- In transmit mode, these set the transmit tone length for each of the 4 tones in an XTCSS sequence.
- In receive mode these bits define the minimum silent prefix and suffix qualification periods for successful reception and they also define the nominal tone decode length. The tone will be decoded if the tone length is up to 1.5 times the programmed tone length, but will not decode if the tone length is greater than twice the programmed length.

The 'detect threshold' bits (bits 9 to 4) set the minimum In-band tone and/or MSK signal level that will be detected. The levels are set according to the formula:

$$\text{Minimum Level} = \text{Detect Threshold} \times 3.63\text{mV rms at } V_{DD}(A) = 3V$$

The In-band tone detected bandwidth is set in accordance with the following table:

					BANDWIDTH	
	Bit 3	Bit 2	Bit 1	Bit 0	Will Decode	Will Not Decode
	1	0	0	0	±1.1%	±2.4%
Recommended for EEA ⇒	**1**	**0**	**0**	**1**	**±1.3%**	**±2.7%**
	1	0	1	0	±1.6%	±2.9%
	1	0	1	1	±1.8%	±3.2%

$C8 (P1.2-5) Programmable In-band Tones

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.2-5	0	1	0	1	0	Programmable In-band Tone										
						N (see below)							R (see below)			

These words set the programmable In-band tones used in transmit and receive. The frequency is set in bits 10-0 for each word according to the formula:

N = Integer part of (0.042666 x frequency)

R = (0.042666 x frequency - N) x 6000 / frequency (round to nearest integer)

Example: For 1010Hz, N = 43, R = 1. The programmed tones should only be set to frequencies between 400Hz to 3000Hz. It is possible to programme frequencies outside these limits but the programmed transmitter signal levels and accuracy and receiver thresholds and decode bandwidths may not be applicable – see section 1.8.1, AC parameters of the In-Band Tone Detector and of the In-Band Tone Encoder.

1.6.20.3 PROGRAMMING REGISTER Block 2 – CTCSS and DCS Setup:

$C8 (P2.0) CTCSS and DCS TX LEVEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.0	1	1	1	0	CTCSS and DCS Level											

Bits 11 (MSB) to 0 (LSB) set the transmitted CTCSS or DCS sub-audio signal level (pk-pk) with a resolution of $V_{DD}(A)/16384$ per LSB (0.183mV per LSB at $V_{DD}(A)$=3V, giving a range 0 to 749.8mV pk-pk).

$C8 (P2.1) CTCSS TONE BW AND LEVEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.1	0	1	1	0	DCS 24	0	CTCSS and DCS detect threshold						CTCSS detect bandwidth			

Bit 11, DCS 24, sets the length of DCS code transmitted or searched for. When this bit is set to '1' 24 bit codes are transmitted and decoded. When this bit is set to '0' 23 bit codes are used.

The 'detect threshold' bits (bits 9 to 4) set the minimum CTCSS or DCS signal level that will be detected. The levels are set according to the formula:

$$\text{Minimum Level} = \text{Detect Threshold} \times 2\text{mV rms at } V_{DD}(A) = 3V$$

The CTCSS detected tone bandwidth is set in accordance with the following table:

	Bit 3	Bit 2	Bit 1	Bit 0	BANDWIDTH Will Decode	BANDWIDTH Will Not Decode
Recommended for use with split tones and Tone Cloning™	0	1	1	0	±0.5%	±1.8%
	0	1	1	1	±0.8%	±2.1%
Recommended for CTCSS ⇒	**1**	**0**	**0**	**0**	**±1.1%**	**±2.4%**
	1	0	0	1	±1.3%	±2.7%
	1	0	1	0	±1.6%	±2.9%
	1	0	1	1	±1.8%	±3.2%

$C8 (P2.2-3) DCS CODE (LOWER) and DCS CODE (UPPER)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.2	0	1	1	0	DCS Data (bits 11-0)											
P2.3	0	1	1	0	DCS Data (bits 23/22-12)											

These words set the DCS code to be transmitted or searched for. The least significant bit (bit 0) of the DCS code is transmitted or compared first and the most significant bit is transmitted or compared last. Note that DCS Data bit 23 is only used when bit 11 (DCS 24) of P2.1 is set to '1'.

$C8 (P2.4) SUBAUDIO DROP OUT TIME

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.4	0	1	1	0	Subaudio Drop Out Time				0							

The Subaudio Drop Out Time defines the time that the sub-audio signal detection can drop out before loss of sub-audio is asserted. The period is set according to the formula:

$$\text{Time} = \text{Subaudio Drop Out Time} \times 8.0\text{ms} \qquad \text{[range 0 to 120ms]}$$

The setting of this register defines the maximum drop out time that the device can tolerate. The setting of this register also determines the de-response time, which is typically 90ms longer than the programmed drop out time.

1.6.20.4 PROGRAMMING REGISTER Block 3 – Reserved

1.6.20.5 PROGRAMMING REGISTER Block 4 – Gain and Offset Setup

$C8 (P4.0) FINE INPUT GAIN

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.0	1	0	Fine Input Gain (unsigned integer)													

Gain = 20 × log([32768-IG]/32768)dB IG is the unsigned integer value in the 'Fine Input Gain' field

Fine input gain adjustment should be kept within the range 0 to -3.5dB.

$C8 (P4.1) Reserved

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.1	0	0	Reserved - set to '0'													

This register is reserved and should be set to '0'.

$C8 (P4.2-3) FINE OUTPUT GAIN 1 and FINE OUTPUT GAIN 2

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.2	0	0	Fine Output Gain 1 (unsigned integer)													
P4.3	0	0	Fine Output Gain 2 (unsigned integer)													

Gain = 20 × log([32768-OG]/32768)dB OG is the unsigned integer value in the 'Fine Output Gain' field

Fine output gain adjustment should be kept within the range 0dB to -3.5dB.

$C8 (P4.4-5) OUTPUT 1 OFFSET and OUTPUT 2 OFFSET

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.4	0	0	2's complement offset for MOD_1, resolution = V_{DD}(A)/65536 per LSB													
P4.5	0	0	2's complement offset for MOD_2, resolution = V_{DD}(A)/65536 per LSB													

The programmed value is subtracted from the output signal Can be used to compensate for inherent offsets in the output path via MOD_1 (Output 1 Offset) and MOD_2 (Output 2 Offset). It is recommended that the offset correction is kept within the range +/-50mV.

$C8 (P4.6) RAMP RATE CONTROL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.6	0	0	Ramp Rate Up Control (RRU)							Ramp Rate Down control (RRD)						

The ramp-up and ramp-down rates can be independently programmed. The ramp rates apply to all the analogue output ports. They only affect those ports being turned on (ramp-up) or turned off (ramp down). The ramp rates should be programmed before ramping any outputs.

Time to ramp-up to full gain = (1 + RRU) × 1.333ms
Time to ramp down to zero gain = (1 + RRD) × 1.333ms

Ramp up starts from when transmit mode starts (Mode Control Register bit 1 set = '1'). Ramp down starts from when transmit mode is turned off (Mode Control Register bit 1 cleared = '0').

$C8 (P4.7) TRANSMIT LIMITER CONTROL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.7	0	0	Limiter Setting, resolution = V_{DD}(A)/16384 per LSB													

This unsigned number sets the clipping point (maximum deviation from the centre value) for the MOD_1 and MOD_2 pins. The maximum setting ($1FFF) is +/- V_{DD}(A)/2 i.e. output limited from 0 to V_{DD}(A).

The limiter is set to maximum following a C-BUS Reset or a Power Up Reset. The limiter is applied to the composite inband and subaudio signal, not just the voice signal. The levels of internally generated signals must be limited by setting appropriate transmit levels.

$C8 (P4.8) Special Programming Register – do not access.

1.7 Application Notes

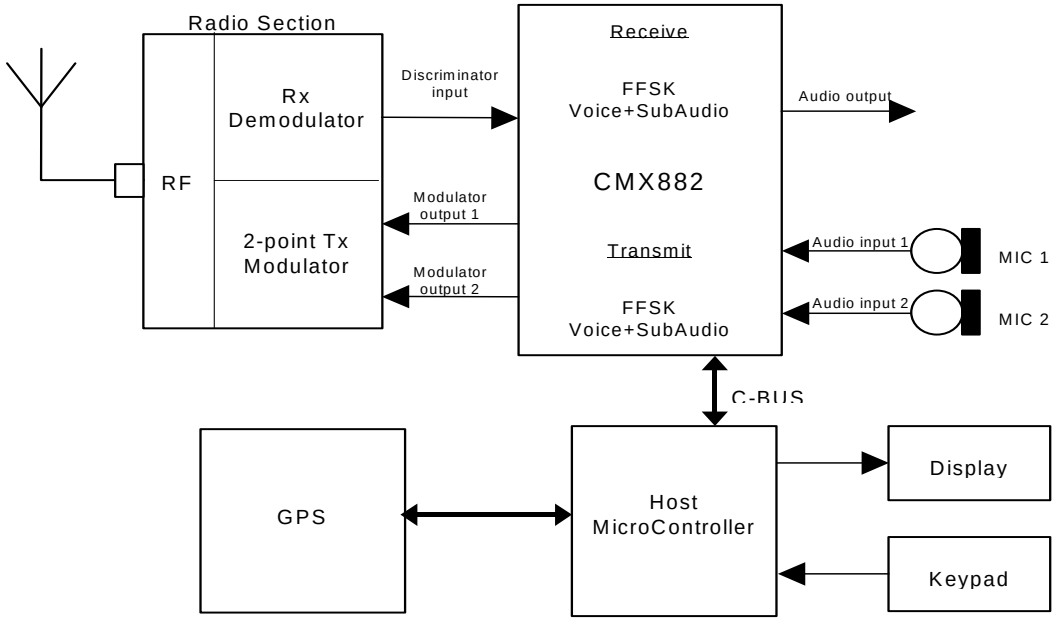


Figure 13 Possible FRS + GPS Configuration

1.7.1 CRC and FEC encoding information

For messages with FEC coding the following matrix is used to calculate and decode bytes:

Data bits								FEC bits			
7	6	5	4	3	2	1	0	3	2	1	0
1	1	1	0	1	1	0	0	1	0	0	0
1	1	0	1	0	0	1	1	0	1	0	0
1	0	1	1	1	0	1	0	0	0	1	0
0	1	1	1	0	1	0	1	0	0	0	1

8 bit CRC is used in all frame heads with the following generator polynomial (GP):

$x^8 + x^7 + x^4 + x^3 + x^1 + x^0$

16 bit CRC is used at the end of sized data messages of up to 16 bytes with the following GP:

$x^{16} + x^{12} + x^5 + x^0$

32 bit CRC is used at the end of sized data messages of over 16 bytes with the following GP:

$x^{32} + x^{31} + x^{30} + x^{28} + x^{27} + x^{25} + x^{24} + x^{22} + x^{21} + x^{20} + x^{16} + x^{10} + x^9 + x^6 + x^0$

1.7.2 Data Interleaving

The built in FFSK packeting includes the option of interleaving the data in each block (Type 5). This, together with Forward Error Correction (FEC), reduces the effects of one of the commonest sources of data errors which is burst noise. Interleaving does not add any bits to the message, the packet is assembled in 'rows' and then transmitting in 'columns'.

Data (8 bits)								FEC (4 bits)			
0	1	2	3	4	5	6	7	8	9	10	11
12	13	14	15	16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31	32	33	34	35
36	37	38	39	40	41	42	43	44	45	46	47

In the above example the packet is assembled as 4 rows with 12 bits of information per row. When this packet is transmitted interleaved the bits are sent over the communication channel in the following order:

0, 12, 24, 36, 1, 13, 25, 37, 2, 14, ... , 33, 45, 10, 22, 34, 46, 11, 23, 35, 47.

In the receiving modem the packet is re-assembled (de-interleaved) before error correction. The 882's built in packet receive modem is able to recognise (by using the frame head bytes) when the data has been interleaved by the transmitter and will decode the data using the correct method.

1.7.3 Scrambler Seed Transfer

The CMX882 data scrambler provides some security for information transfer by allowing the use of different seed patterns. This requires that the transmitting and receiving devices have identical scrambler seeds. Should two radios wish to transfer data using the scrambler the seed must be transferred between them before data transfer takes place. This is best done 'off air' by prior arrangement. Obviously sending the seed over air by voice or by using FFSK (with either no scrambling or the standard scrambler) will enable an eavesdropper to grab the seed as it is transferred and then decode any following messages using that seed.

The following method allows the transfer of a seed between two unrelated radios (from A to B) without the actual 16 bit seed pattern appearing over the air:

Radio	Calculates	Sends over air
A	Seed + X	Seed + X
B	Rx + Y	Seed + X + Y
A	Rx - X	Seed + Y
B	Rx - Y	

Example (4 bit), X=3, Y=9	
Calculates	Sends over air
8 + 3	11
11 + 9	4
4 - 3	1
1 - 9 = **8**	-

The values used for the Seed, X and Y can be any number up to 65535 and all 3 numbers should be different for each seed transfer.

This and other simple methods allow an eavesdropper to use basic mathematical techniques (11-4+1 in the above example) to use the over air information to derive the original seed (they must however have detected all three over air messages to do this). To reduce this possibility the host can employ more sophisticated techniques for seed transfer (e.g. functions using large prime numbers) as this will greatly increase the mathematical complexity required to find the original seed. However, such methods are beyond the scope of this document. Also, they may not be permitted in certain territories and are probably not appropriate for the level of security provided by the inbuilt scrambler.

The data scrambler uses a 16 bit pseudo random number generator with the following feed back taps:

$x^{16} + x^{14} + x^{1} + x^{0}$

1.8 Performance Specification

1.8.1 Electrical Performance

The performance data are target figures, that may change subject to the outcome of device evaluation.

Absolute Maximum Ratings
Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: V_{DD}(D)- V_{SS}(D)	–0.3	7.0	V
V_{DD}(A)- V_{SS}(A)	–0.3	7.0	V
Voltage on any pin to V_{SS}(D)	–0.3	V_{DD}(D) + 0.3	V
Voltage on any pin to V_{SS}(A)	–0.3	V_{DD}(A) + 0.3	V
Current into or out of V_{DD}(A), V_{SS}(A), V_{DD}(D) and V_{SS}(D)	–30	+30	mA
Current into or out of any other pin	–20	+20	mA
Voltage differential between power supplies:			
V_{DD}(D) and V_{DD}(A)	0	0.3	V
V_{SS}(D) and V_{SS}(A)	0	50	mV

D6 Package (SSOP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C		1490	mW
... Derating		14.9	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

E1 Package (TSSOP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C		1110	mW
... Derating		11.1	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Operating Limits
Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply (V_{DD} - V_{SS})		2.7	5.5	V
Operating Temperature		–40	+85	°C
Clock/Xtal Frequency	11	18.3	18.6	MHz

Notes: 11 Nominal clock frequency is 18.432MHz.

Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 18.432MHz ±0.01% (100ppm).
V_{DD} = 2.7V to 5.5V; Tamb = −40°C to +85°C.
Signal levels are defined for Vdd = 3V.
Signal levels track with supply voltage, so scale accordingly
Reference Signal Level = 308mV rms at 1kHz with V_{DD} = 3V.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB.
Output stage attenuation = 0dB.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current					
I_{DD}(D) (V_{DD} = 3.0V)	21		4.5	8.0	mA
I_{DD}(A) (V_{DD} = 3.0V)	21		1.0	2.0	mA
I_{DD}(D) (All Power-saved) (V_{DD} = 3.0V)	21		2.0	10	µA
I_{DD}(A) (All Power-saved) (V_{DD} = 3.0V)	21		2.0	10	µA
C-BUS Interface					
Input Logic '1'		70%			V_{DD}
Input Logic '0'				30%	V_{DD}
Input Leakage Current (Logic '1' or '0')	21	−1.0		1.0	µA
Input Capacitance		-		7.5	pF
Output Logic '1' (I_{OH} = 120µA)		90%			V_{DD}
Output Logic '0' (I_{OL} = 360µA)				10%	V_{DD}
"Off" State Leakage Current	21			10	µA
IRQN (Vout = V_{DD}(D))	21	−1.0		1.0	µA
REPLY_DATA (output HiZ)	21	−1.0		1.0	µA
CLOCK_OUT					
Output Logic '1' (I_{OH} = 120µA)		90%			V_{DD}
(I_{OH} = 1mA)		80%			V_{DD}
Output Logic '0' (I_{OL} = 360µA)				10%	V_{DD}
(I_{OL} = -1.5mA)				15%	V_{DD}
CLOCK/XTAL	22				
Input Logic '1'		70%			V_{DD}
Input Logic '0'				30%	V_{DD}
Input current (Vin = V_{DD})				40	µA
Input current (Vin = V_{SS})		−40			µA
V_{BIAS}	23				
Output voltage offset wrt V_{DD}/2 (I_{OL} < 1µA)		-2%		+2%	V_{DD}
Output impedance			22		kΩ

Notes:
21 Tamb = 25°C, not including any current drawn from the device pins by external circuitry.
22 Characteristics when driving the CLOCK/XTAL pin with an external clock source.
23 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 3.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
CLOCK/XTAL Input						
'High' pulse width		31	21			ns
'Low' pulse width		31	21			ns
Input impedance (at 18.432MHz)						
Powered-up	Resistance			150		kΩ
	Capacitance			20		pF
Powered-down	Resistance			300		kΩ
	Capacitance			20		pF
Clock frequency				18.432		MHz
Clock stability/accuracy					±100	ppm
Clock start up (from power-save)				400		ms
CLOCK_OUT Output						
CLOCK/XTAL input to CLOCK_OUT timing:						
(in high to out high)		32		15		ns
(in low to out low)		32		15		ns
'High' pulse width		33	22	27.13	33	ns
'Low' pulse width		33	22	27.13	33	ns
V_{BIAS}						
Start up time (from power-save)				30		ms
Microphone, Input_2 and Disc Inputs (MIC, INPUT_2, DISC)						
Input impedance		34		1		MΩ
Input signal range		35	10		90	$\%V_{DD}$
Feedback load resistance (pins 12, 14 & 16)			80			kΩ
Amplifier open loop voltage gain (I/P = 1mV rms at 100Hz)				60		dB
Unity gain bandwidth				1.0		MHz
Programmable Input Gain Stage		36				
Gain (at 0dB)			−0.5	0	0.5	dB
Cumulative Gain Error (wrt attenuation at 0dB)			−1.0		1.0	dB

Notes:

31 Timing for an external input to the CLOCK/XTAL pin.

32 CLOCK/XTAL input driven by external source.

33 18.432MHz XTAL fitted.

34 With no external components connected

35 After multiplying by gain of input circuit, with external components connected.

36 Gain applied to signal at output of buffer amplifier, pin 12, 14 or 16

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1 and 2 and Audio Output (MOD_1, MOD_2, AUDIO)					
Power-up to output stable	37		50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)	39	−1.0	0	1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−0.6		0.6	dB
Output Impedance Enabled	38		600		Ω
Output Impedance Disabled	38		500		kΩ
Output current range (V_{DD} = 3.0V)		-125		125	µA
Output voltage range	40	0.5		V_{DD}–0.5	V
Load resistance		20			kΩ
Audio Attenuator					
Attenuation (at 0dB)	39	−1.0	0	1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−1.0		1.0	dB
Output Impedance Enabled	38		600		Ω
Output Impedance Disabled	38		500		kΩ
Output current range (V_{DD} = 3.0V)		-125		125	µA
Output voltage range	40	0.5		V_{DD}–0.5	V
Load resistance		20			kΩ

Notes:

37 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in power-save mode.

38 Small signal impedance, at V_{DD} = 3.0V and Tamb = 25°C.

39 Wrt the signal at the feedback pin of the selected input port.

40 With output driving a 20kΩ load to $V_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary ADC (Signal Monitor)					
8 Bit ADC Mode					
Resolution			8		Bits
Input Range		10%		90%	V_{DD}
Conversion time	41		20.8		µs
Input impedance					
Resistance			10		MΩ
Capacitance			5		pF
Zero error (input offset to give ADC output = 0)		−20		+20	mV
Integral Non-linearity	42			2	LSB
	43			4	LSB
Differential Non-linearity	42			1	LSB
	43			3	LSB
Source output impedance	44			24	kΩ
Level Threshold Detect Mode					
Threshold Resolution			8		Bits
Upper threshold range (VTH)	45	VTL		V_{DD}(A)	V
Lower threshold range (VTL)	45	V_{SS}(A)		VTH	V
Signal Monitor change to IRQ	46			120	µs
Signal Monitor change to Receiver-Turn-On	47			60	µs
Audio Compandor					
Attack time	49		4.0		ms
Decay time	50		13		ms
0dB point	48		100		mVrms
Compression / Expansion ratio			2:1		

Notes:

41 With clock frequency of 18.432MHz.

42 $V_{DD}(A) \geq 3.0V$

43 $V_{DD}(A) < 3.0V$

44 Denotes output impedance of the driver of the Signal Monitor input, to ensure < 1 bit additional error under nominal conditions.

45 Upper threshold > Lower threshold

46 Time from Signal Monitor input rising above Upper Threshold or falling below Lower Threshold, to IRQN being asserted.

47 Time from Signal Monitor input rising above Upper Threshold to receiver path powering up, settling and starting automatic signal type identification.

48 $V_{DD}(A) = 3.0V$

49 The attack time of the transmitter's compressor is defined as the time taken for the output signal to settle to 1.5 times its (eventual) steady state value, following an abrupt 12dB increase in the input signal amplitude. The attack time of the receiver's expander is defined as the time taken for the output signal to settle to 0.57 times its (eventual) steady state value, following an abrupt 6dB increase in the input signal amplitude.

50 The decay time of the compressor is defined as the time taken for the output signal to settle to 0.75 times its (eventual) steady state value, following an abrupt 12dB decrease in the input signal amplitude. The decay time of the expander is defined as the time taken for the output signal to settle to 1.5 times its (eventual) steady state value, following an abrupt 6dB decrease in the input signal amplitude.

AC Parameters (cont.)		Notes	Min.	Typ.	Max.	Unit
Receiver Signal Type Identification						
Probability of correctly identifying signal type	(SNR = 12dB)			>>99.9		%
CTCSS Detector						
Sensitivity	(Pure Tone)	51		-26		dB
Response Time	(Composite Signal)	52		140	250	ms
De-response Time	(Composite Signal)	52, 55		210		ms
Dropout immunity		55		160		ms
Frequency Range			60		260	Hz
IN-BAND TONE Detector						
Sensitivity	(Pure Tone)	53		-26		dB
Response Time	(Good Signal)			35		ms
De-response Time	(Good Signal)				52	ms
Dropout immunity					20	ms
Frequency Range	(In-band tone)	56	400		3000	Hz
DCS Decoder						
Sensitivity		51	58			mVp-p
Bit-Rate Sync Time				2		edges
FFSK/MSK Decoder						
Signal Input Dynamic Range		54	100		800	mVrms
Bit Error Rate	(SNR = 20dB)	54		<1		10^{-8}
Receiver Synchronisation	(SNR = 12dB)					
Probability of bit 16 being correct				>99.9		%

Notes:

51 Sub-Audio Detection Level threshold set to 16mV.

52 Composite signal = 308mV rms at 1kHz + 75mV rms Noise + 31mV rms Sub-Audio signal. Noise bandwidth = 5kHz Band Limited Gaussian.

53 In-band Tone Detection Level threshold set to 16mV.

54 $V_{DD}(A)$ = 3.0V, for a "101010101 ... 01" pattern measured at the input amplifier feedback pin (12). Signal level scales with $V_{DD}(A)$. See Figure 15 for variation of BER with SNR.

55 With sub-audio dropout time (P2.4) set to ≥ 120ms. The typical dropout immunity is approximately 40ms more than the programmed dropout immunity. The typical de-response time is approximately 90ms longer than the programmed dropout immunity. See section 1.6.20.3, P2.4.

56 The device can decode in-band tones below the 400Hz lower limit but not necessarily within the selected bandwidth or with the selected threshold resolution. This can result in some CTCSS tones above approximately 160Hz being flagged in the Tone Status register as unrecognised in-band tones.
Some tones in the range 250Hz to 400Hz cannot be defined by the 'in-band' custom tones programming facility, but can be detected by selecting a valid close tone and using a suitably wide bandwidth setting.

AC Parameters (cont.)		Notes	Min.	Typ.	Max.	Unit
CTCSS Encoder						
Frequency Range			60.0		260	Hz
Tone Frequency Accuracy					±0.3	%
Tone Amplitude Tolerance		61	-1.0		+1.0	dB
Total Harmonic Distortion		62		2.0	4.0	%
In-band tone Encoder						
Frequency Range		64	400		3000	Hz
Tone Frequency Accuracy					±0.3	%
Tone Amplitude Tolerance		63	-1.0		+1.0	dB
Total Harmonic Distortion		62		2.0	4.0	%
DCS Encoder						
Bit Rate				134.4		bits/s
Amplitude Tolerance		61	-1.0		+1.0	dB
FFSK/MSK Encoder						
Output signal level				775		mVrms
Output level variation			-1.0		+1.0	dB
Output distortion					5	%
3rd harmonic distortion					3	%
Logic 1 freq	1200baud and 2400baud		1198	1200	1202	Hz
Logic 0 freq	1200baud		1798	1800	1802	Hz
	2400baud		2398	2400	2402	Hz
Isochronous distortion (0 to 1 and 1 to 0)					40	μs

Notes:

61 V_{DD}(A) = 3.0V and TX Sub-Audio Level set to 88mV p-p (31mV rms).

62 Measured at MOD_1 or MOD_2 output.

63 V_{DD}(A) = 3.0V and Tx Audio Level set to 871mV p-p (308mV rms).

64 'In-band' tones between 400Hz and approximately 250Hz can be programmed, but the range is not contiguous and the transmitted tones may not be within the tone accuracy limits.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Analogue Channel Audio Filtering					
Pass-band (nominal bandwidth):					
Received voice	71	300		3000	Hz
12.5kHz channel transmitted voice	72	300		2550	Hz
25kHz channel transmitted voice	73	300		3000	Hz
Pass-band Gain (at 1.0kHz)			0		dB
Pass-band Ripple (wrt gain at 1.0kHz)		-2		+0.5	dB
Stop-band Attenuation		33.0			dB
Residual Hum and Noise	76		-50		dB
Pre-emphasis	74		6		dB/oct
De-emphasis	75		−6		dB/oct
Audio Scrambler					
Inversion frequency			3300		Hz
Pass band		300		3000	Hz
Audio Expandor					
Input signal range	77			0.5	Vrms

Notes:

71 The receiver voice filter complies with the characteristic shown in Figure 5. The high pass filtering removes sub-audio components from the audio signal.

72 The 12.5kHz channel filter complies with the characteristic shown in Figure 9.

73 The 25kHz channel filter complies with the characteristic shown in Figure 8.

74 The pre-emphasis filter complies with the characteristic shown in Figure 10.

75 The de-emphasis filter complies with the characteristic shown in Figure 6.

76 Measured in a 30kHz bandwidth.

77 $V_{DD}(A) = 3.0V$

C-BUS Timing

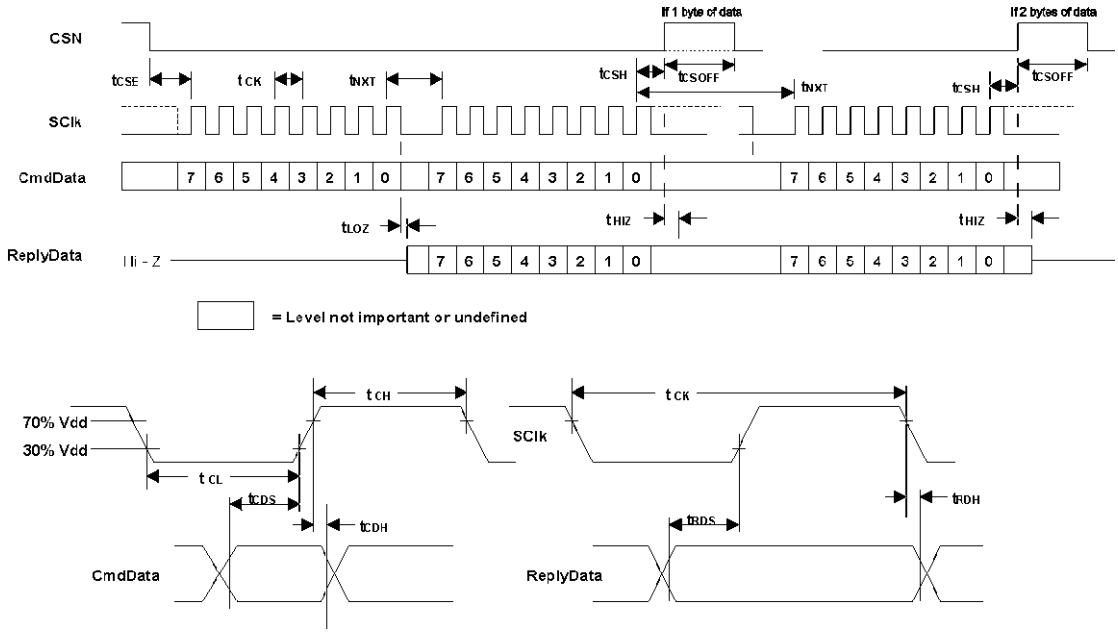


Figure 14 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SClk high time		100			ns
t_{CSH}	Last SClk high to CSN high time		100			ns
t_{LOZ}	SClk low to ReplyData Output Enable Time		0.0			ns
t_{HIZ}	CSN high to ReplyData high impedance				1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0			µs
t_{NXT}	Inter-byte time		200			ns
t_{CK}	SClk cycle time		200			ns
t_{CH}	SClk high time		100			ns
t_{CL}	SClk low time		100			ns
t_{CDS}	Command Data setup time		75			ns
t_{CDH}	Command Data hold time		25			ns
t_{RDS}	Reply Data setup time		50			ns
t_{RDH}	Reply Data hold time		0			ns

Notes:
1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SERIAL_CLOCK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SERIAL_CLOCK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX882 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

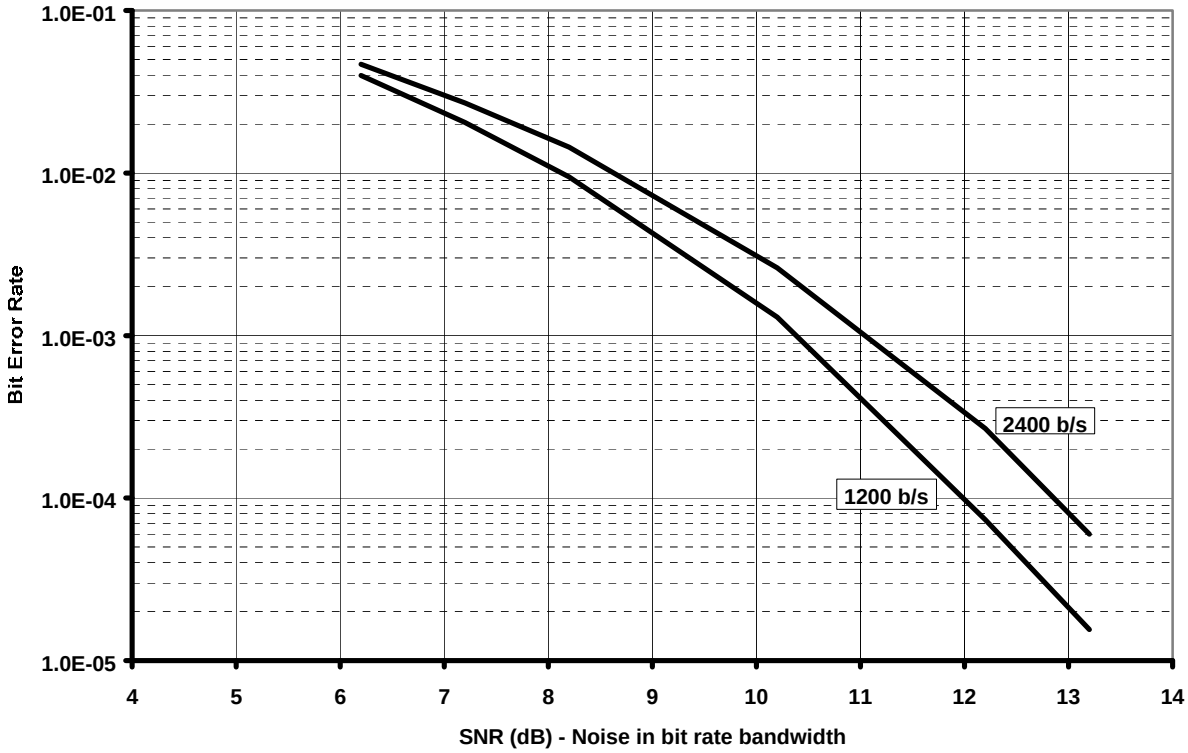
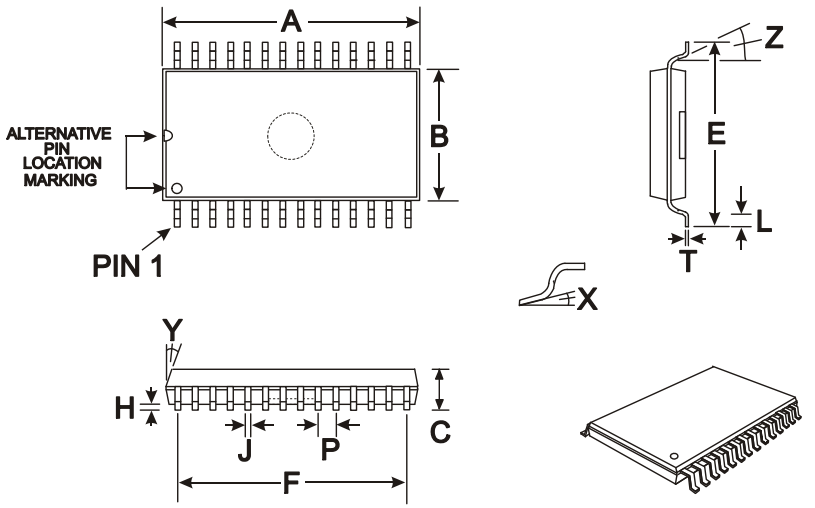


Figure 15 Typical FFSK/MSK Bit Error Rate Graph

1.8.2 Packaging



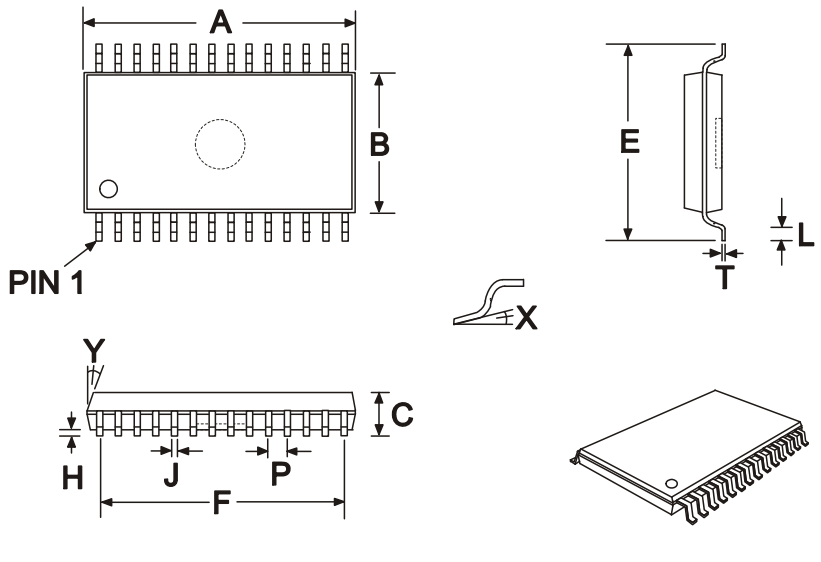
	DIM.	MIN.	TYP.	MAX.
*	A	9.90		10.50
*	B	5.00		5.60
	C	1.67		2.00
	E	7.40		8.20
	F		8.45	
	H	0.05		0.21
	J	0.22		0.38
	L	0.55		0.95
	P		0.65	
	T	0.09		0.25
	X	0°		8°
	Y	7°		9°
	Z	4°		12°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 16 Mechanical Outline of 28-pin SSOP (D6): *Order as part no. CMX882D6*



	DIM.	MIN.	TYP.	MAX.
*	A	9.60		9.80
*	B	4.30		4.50
	C	--------		1.20
	E	6.20		6.60
	F		8.45	
	H	0.05		0.15
	J	0.17		0.30
	L	0.45		0.75
	P		0.65	
	T	0.08		0.20
	X	0°		8°
	Y		12°	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Figure 17 Mechanical Outline of 28-pin TSSOP (E1): *Order as part no. CMX882E1*

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