Photoflash Capacitor Chargers with Output Voltage Monitor and Integrated IGBT Drive

FEATURES

- **Integrated IGBT Driver**
- **Voltage Output Monitor**
- **Uses Small Transformers: 5.8mm × 5.8mm × 3mm**
- **Operates from Two AA Batteries, Single Cell Li-Ion or Any Supply from 1.8V up to 10V**
- No Output Voltage Divider Needed
- No External Schottky Diode Required
- Charges Any Size Photoflash Capacitor
- Available in 10-Lead (3mm × 3mm) DFN

Fast Charge Time

VERSION	INPUT CURRENT (mA)	CHARGE TIME (sec)
LT3485-3	750	2.5
LT3485-0	500	3.7
LT3485-2	350	5.5
LT3485-1	225	4.0*

V_{IN} = V_{BAT} = 3.6V
100µF capacitor, 320V. *50µF capacitor

APPLICATIONS

- Digital Camera and Cell Phone Flash Charger

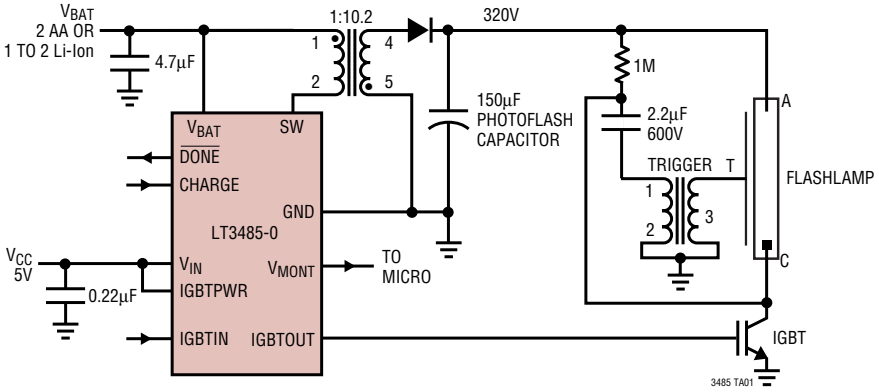
DESCRIPTION

The LT®3485 family of photoflash chargers are highly integrated ICs containing complete charger and IGBT drive functions. The patented control technique of the LT3485-x allows it to use extremely small transformers. Output voltage detection requires no external circuitry. The turns ratio of the transformer controls the final charge voltage. While charging, the output voltage on the capacitor may be monitored by a microcontroller from the monitor pin. Each device contains an on-chip high voltage NPN power switch, which can withstand negative voltages on the switch pin without an external Schottky diode. The device features a V_{BAT} pin, which allows the use of two AA cells to charge the capacitor. The internal circuitry operates from the V_{IN} pin. The LT3485-0 has a primary current limit of 1.4A, whereas the LT3485-3, LT3485-2, and LT3485-1 have current limits of 2A, 1A and 0.7A respectively. These different current limits result in tightly controlled input currents.

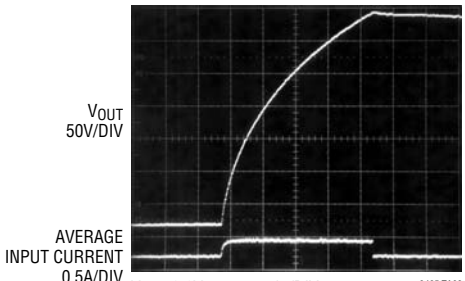
The CHARGE pin gives full control of the part to the user. Driving CHARGE low puts the part in shutdown. The $\overline{DONE}$ pin indicates when the part has completed charging. The LT3485 series of parts are housed in a leadless (3mm × 3mm) DFN package.

TYPICAL APPLICATION

LT3485-0 Photoflash Charger Uses High Efficiency 3mm Tall Transformers
DANGER HIGH VOLTAGE – OPERATION BY HIGH VOLTAGE TRAINED PERSONNEL ONLY



LT3485-0 Charging Waveform

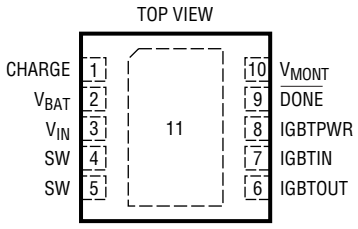


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage 10V
V_{BAT} Voltage 10V
SW Voltage ..... –1V to 50V
SW Pin Negative Current ..... –0.5A
CHARGE Voltage 10V
IGBTIN Voltage 10V
IGBTOUT Voltage 10V
$\overline{DONE}$ Voltage 10V
IGBTPWR Voltage 10V
V_{MONT} Voltage 10V
Current into $\overline{DONE}$ Pin 0.2mA/–1mA
Maximum Junction Temperature ..... 125°C
Operating Temperature Range (Note 2) ... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

PACKAGE/ORDER INFORMATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C θ_{JA} = 43°C/W
EXPOSED PAD (11) IS GND, MUST BE SOLDERED TO PCB

ORDER PART NUMBER	DD PART MARKING
LT3485EDD-0	LBRH
LT3485EDD-1	LBVN
LT3485EDD-2	LBVP
LT3485EDD-3	LBTK

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{BAT} = V_{CHARGE} = 3V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current	Not Switching V_{CHARGE} = 0V			5 0	8 1	mA µA
V_{IN} Voltage Range		●	2.5		10	V
V_{BAT} Voltage Range		●	1.7		10	V
Switch Current Limit	LT3485-3 LT3485-0 LT3485-2 LT3485-1		1.6 1.1 0.75 0.45	1.7 1.2 0.85 0.55	1.8 1.3 0.95 0.65	A A A A
Switch V_{CESAT}	LT3485-3, I_{SW} = 1.5A LT3485-0, I_{SW} = 1A LT3485-2, I_{SW} = 700mA LT3485-1, I_{SW} = 400mA			310 210 170 100	400 300 225 175	mV mV mV mV
V_{OUT} Comparator Trip Voltage	Measured as $V_{SW} – V_{IN}$	●	31	31.5	32	V
V_{OUT} Comparator Overdrive	300ns Pulse Width			200	400	mV
DCM Comparator Trip Voltage	Measured as $V_{SW} – V_{IN}$	●	10	45	120	mV
CHARGE Pin Current	V_{CHARGE} = 3V V_{CHARGE} = 0V			65 0	100 0.1	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{BAT} = V_{CHARGE} = 3V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch Leakage Current	V_{IN} = V_{SW} = 5V, in Shutdown	●		0.01	1	µA
CHARGE Input Voltage High		●	1			V
CHARGE Input Voltage Low		●			0.3	V
Minimum Charge Pin Low Time	High→Low→High			20		µs
$\overline{DONE}$ Output Signal High	100kΩ from V_{IN} to $\overline{DONE}$			3		V
$\overline{DONE}$ Output Signal Low	33µA into $\overline{DONE}$ Pin			140	200	mV
$\overline{DONE}$ Leakage Current	$V_{\overline{DONE}}$ = 3V, $\overline{DONE}$ NPN Off			20	100	nA
IGBT Input Voltage High		●	1.5			V
IGBT Input Voltage Low		●			0.3	V
IGBT Output Rise Time	C_{OUT} = 4000pF, IGBTPWR = 5V, 10%→90%			450		ns
IGBT Output Fall Time	C_{OUT} = 4000pF, IGBTPWR = 5V, 90%→10%			340		ns
V_{OUT} Monitor Accuracy	SW – V_{BAT} = 20V SW – V_{BAT} = 30V		610 920	625 940	640 960	mV mV
Monitor Output Current				200		µA

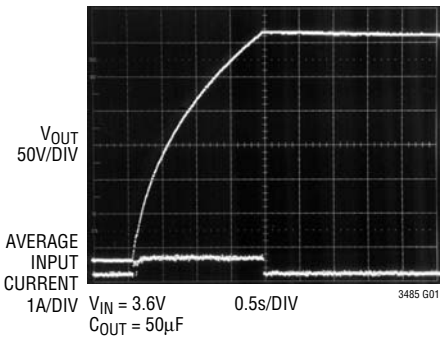
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3485E-X is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

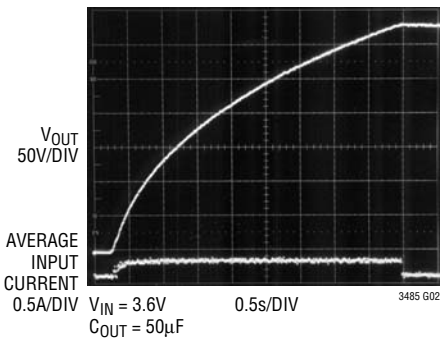
TYPICAL PERFORMANCE CHARACTERISTICS

LT3485-0 curves use the circuit of Figure 8, LT3485-1 curves use the circuit of Figure 9, LT3485-2 use the circuit of Figure 10 and LT3485-3 use the circuit of Figure 11 unless otherwise noted.

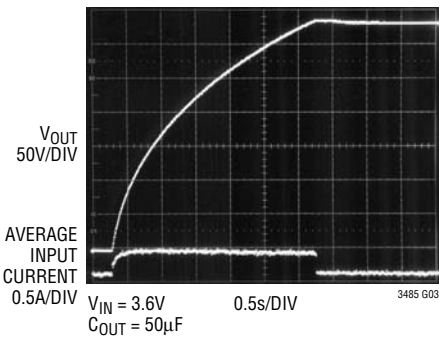
LT3485-0 Charging Waveform



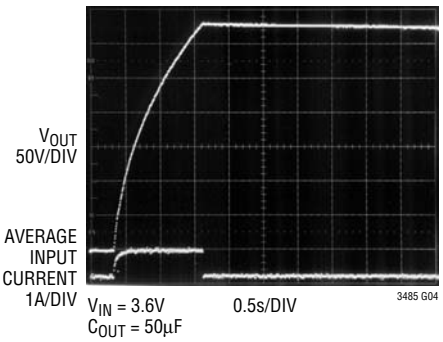
LT3485-1 Charging Waveform



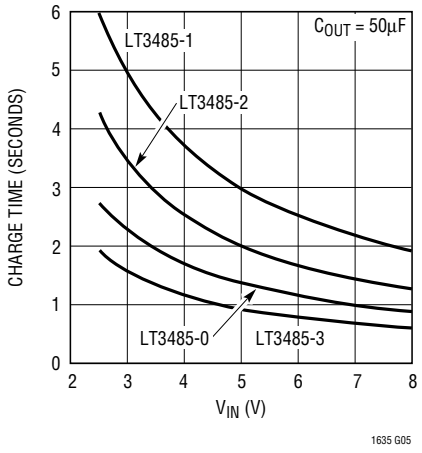
LT3485-2 Charging Waveform



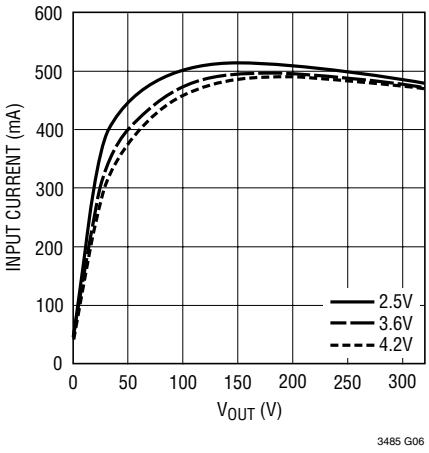
LT3485-3 Charging Waveform



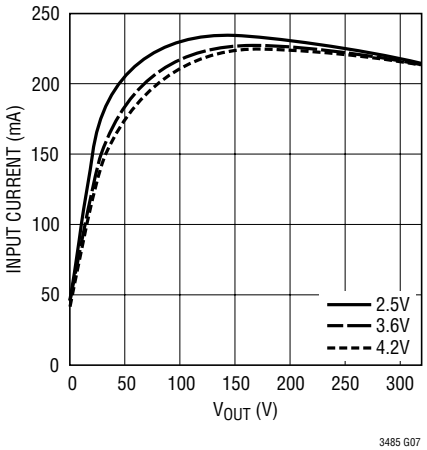
Charge Time



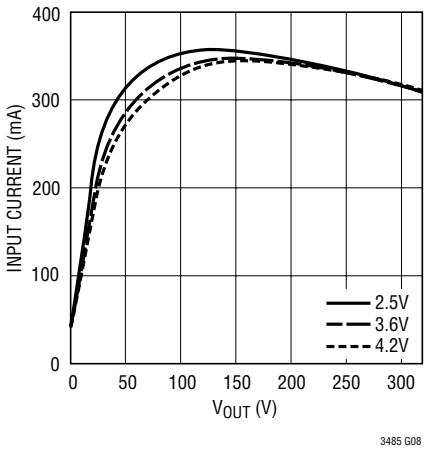
LT3485-0 Input Current



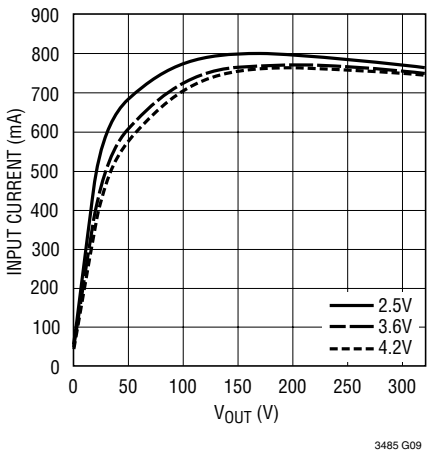
LT3485-1 Input Current



LT3485-2 Input Current



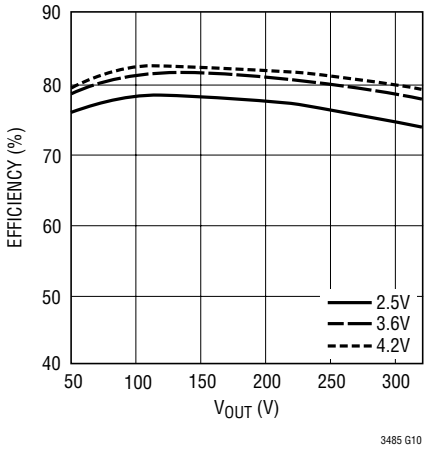
LT3485-3 Input Current



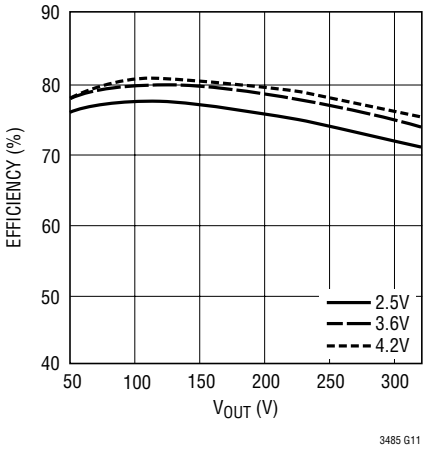
TYPICAL PERFORMANCE CHARACTERISTICS

LT3485-0 curves use the circuit of Figure 8, LT3485-1 curves use the circuit of Figure 9, LT3485-2 use the circuit of Figure 10 and LT3485-3 use the circuit of Figure 11 unless otherwise noted.

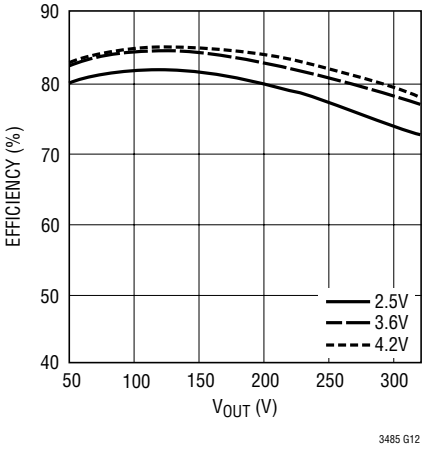
LT3485-0 Efficiency



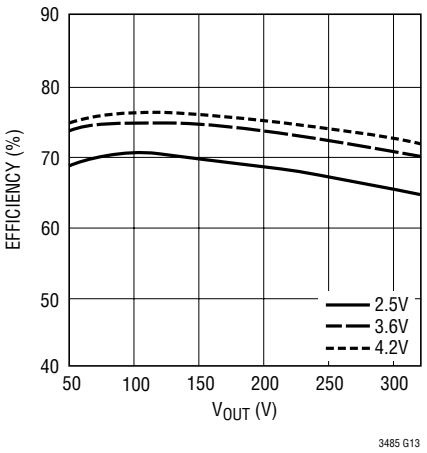
LT3485-1 Efficiency



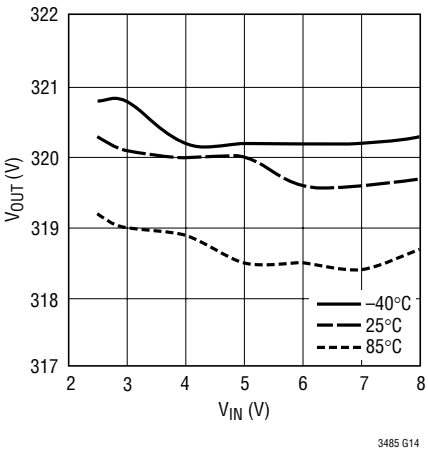
LT3485-2 Efficiency



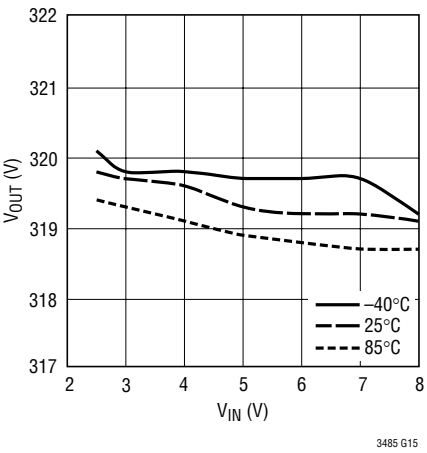
LT3485-3 Efficiency



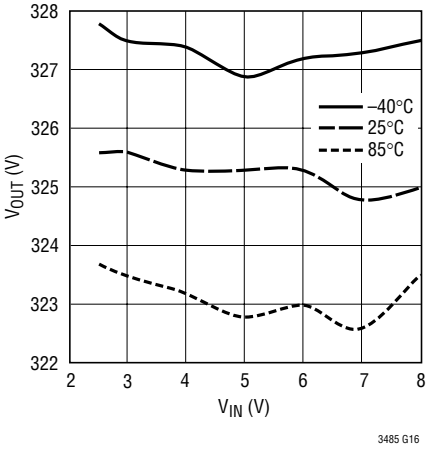
LT3485-0 Output Voltage



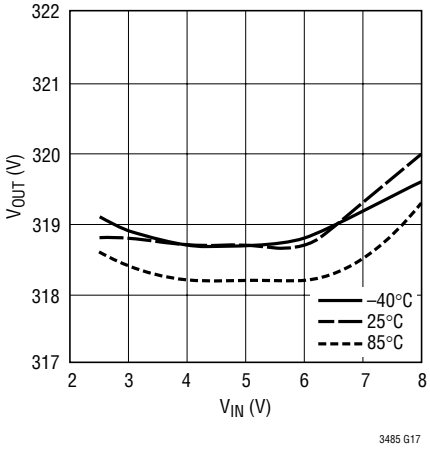
LT3485-1 Output Voltage



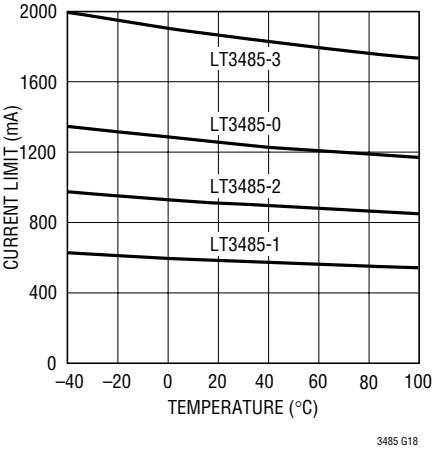
LT3485-2 Output Voltage



LT3485-3 Output Voltage



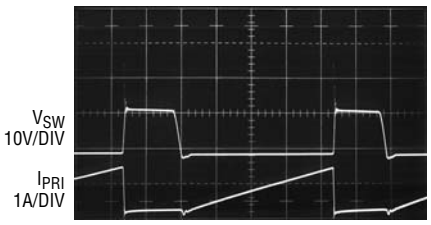
LT3485 Switch Current Limits



TYPICAL PERFORMANCE CHARACTERISTICS

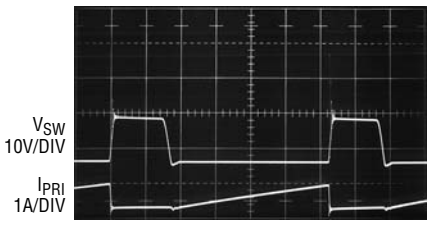
LT3485-0 curves use the circuit of Figure 8, LT3485-1 curves use the circuit of Figure 9, LT3485-2 use the circuit of Figure 10 and LT3485-3 use the circuit of Figure 11 unless otherwise noted.

LT3485-0 Switching Waveform



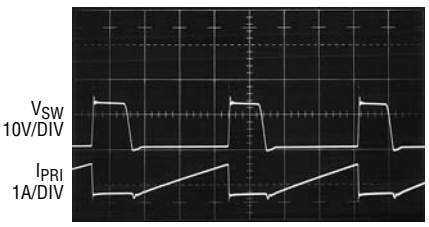
V_{IN} = 3.6V 1µs/DIV
V_{OUT} = 100V

LT3485-1 Switching Waveform



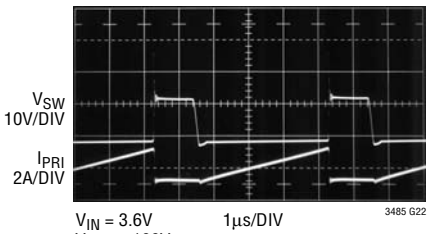
V_{IN} = 3.6V 1µs/DIV
V_{OUT} = 100V

LT3485-2 Switching Waveform



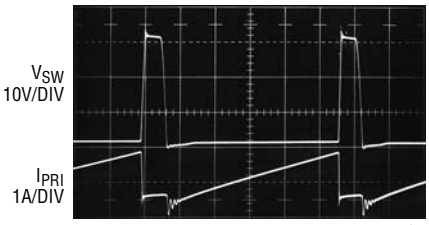
V_{IN} = 3.6V 1µs/DIV
V_{OUT} = 100V

LT3485-3 Switching Waveform



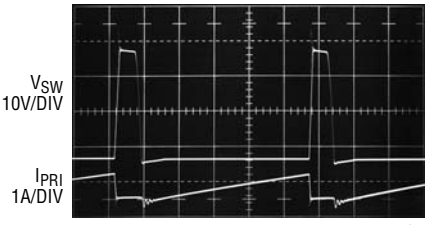
V_{IN} = 3.6V 1µs/DIV
V_{OUT} = 100V

LT3485-0 Switching Waveform



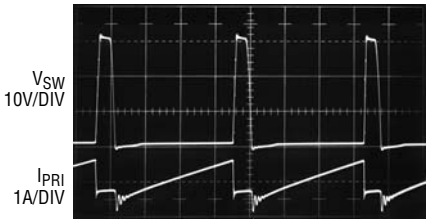
V_{IN} = 3.6V 1µs/DIV
V_{OUT} = 300V

LT3485-1 Switching Waveform



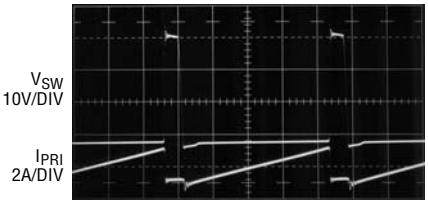
V_{IN} = 3.6V 1µs/DIV
V_{OUT} = 300V

LT3485-2 Switching Waveform



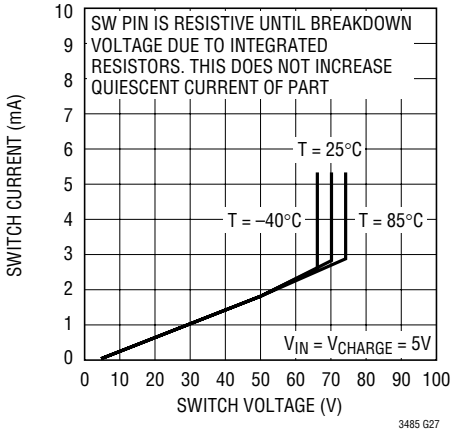
V_{IN} = 3.6V 1µs/DIV
V_{OUT} = 300V

LT3485-3 Switching Waveform



V_{IN} = 3.6V 1µs/DIV
V_{OUT} = 300V

LT3485-0/LT3485-1/LT3485-2/ LT3485-3 Switch Breakdown Voltage



PIN FUNCTIONS

CHARGE (Pin 1): Charge Pin. A low (<0.3V) to high (>1V) transition on this pin puts the part into power delivery mode. Once the target voltage is reached, the part will stop charging the output. Toggle this pin to start charging again. Bringing the pin low (<0.3V) will terminate the power delivery and put the part in shutdown.

V_{BAT} (Pin 2): Battery Supply Pin. Must be locally bypassed with a good quality ceramic capacitor. Battery supply must be 1.7V or higher.

V_{IN} (Pin 3): Input Supply Pin. Must be locally bypassed with a good quality ceramic capacitor. Input supply must be 2.5V or higher.

SW (Pins 4, 5): Switch Pin. This is the collector of the internal NPN power switch. Minimize the metal trace area connected to this pin to minimize EMI. Tie one side of the primary of the transformer to this pin. The target output voltage is set by the turns ratio of the transformer.

Choose Turns Ratio N by the following equation:

$$N = \frac{V_{OUT} + 2}{31.5}$$

where V_{OUT} is the desired output voltage.

IGBTOUT (Pin 6): Output Drive for IGBT Gate. Connect this pin to the gate of the IGBT.

IGBTIN (Pin 7): Logic Input Pin for IGBT Drive. When this pin is driven higher than 1.5V, the IGBT output pin goes high. When the pin is below 0.3V, the output is low.

IGBTPWR (Pin 8): Input Supply Pin. Must be locally bypassed with a good quality ceramic capacitor. Input supply must be 0.1V higher than the turn-on voltage for the IGBT.

$\overline{\text{DONE}}$ (Pin 9): Open NPN Collector Indication Pin. When target output voltage is reached, NPN turns on. This pin needs a pull-up resistor or current source.

V_{MONT} (Pin 10): Supplies a voltage proportional to the output voltage where 1V is the end of charge voltage. Only valid while the part is charging.

Exposed Pad (Pin 11): Ground. Tie directly to local ground plane.

FUNCTIONAL BLOCK DIAGRAM

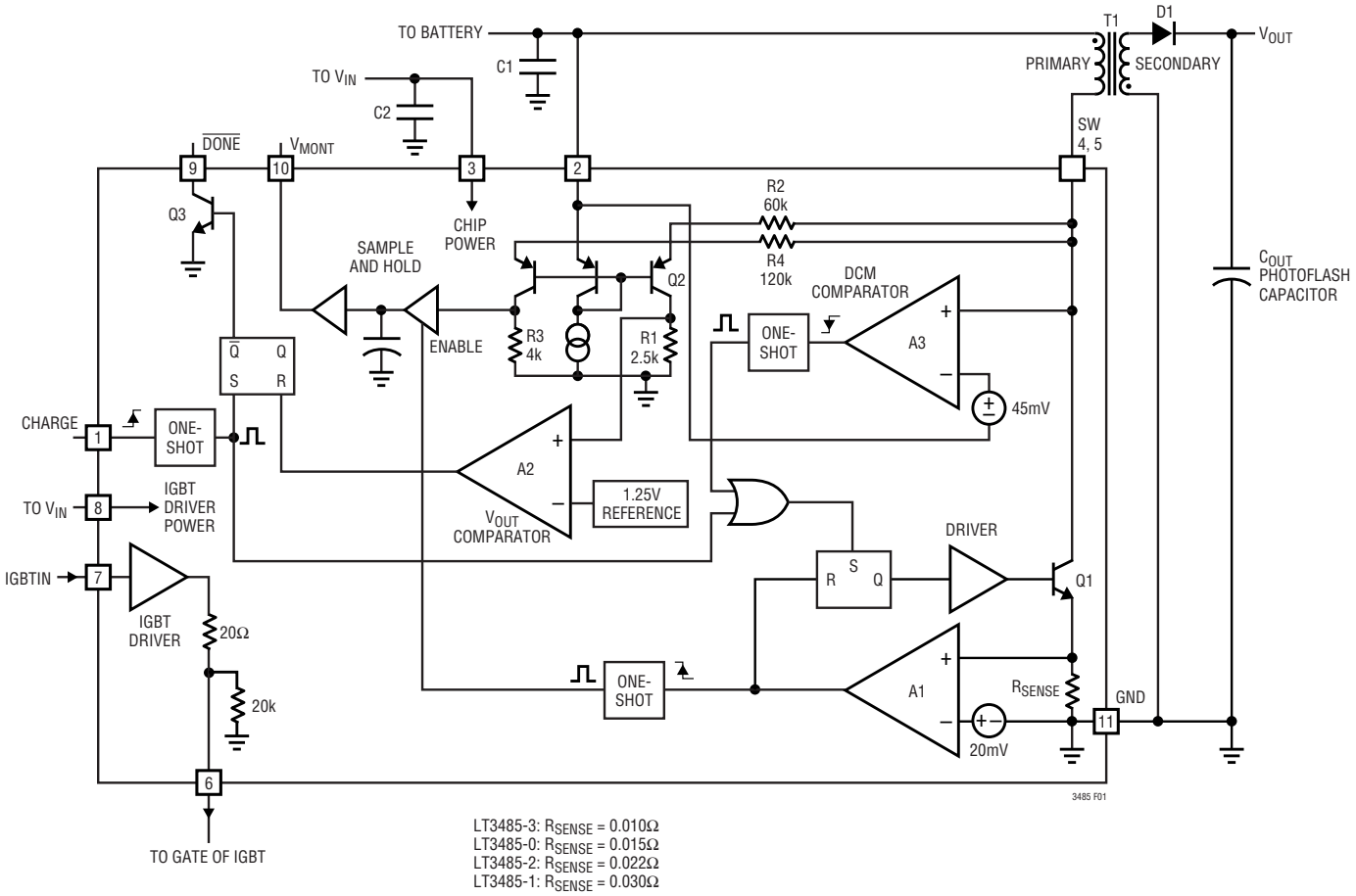


Figure 1

OPERATION

The LT3485-0/LT3485-1/LT3485-2/LT3485-3 are designed to charge photoflash capacitors quickly and efficiently. The operation of the part can be best understood by referring to Figure 1. When the CHARGE pin is first driven high, a one shot sets both SR latches in the correct state. The power NPN device, Q1, turns on and current begins ramping up in the primary of transformer T1. Comparator A1 monitors the switch current and when the peak current reaches 2A (LT3485-3), 1.4A (LT3485-0), 1A (LT3485-2) or 0.7A (LT3485-1), Q1 is turned off. Since T1 is utilized as a flyback transformer, the flyback pulse on the SW pin will cause the output of A3 to be high. The voltage on the SW pin needs to be at least 45mV higher than V_{BAT} for this to happen.

During this phase, current is delivered to the photoflash capacitor via the secondary and diode D1. As the secondary current decreases to zero, the SW pin voltage will begin to collapse. When the SW pin voltage drops to 45mV above V_{BAT} or lower, the output of A3 (DCM Comparator) will go low. This fires a one shot which turns Q1 back on. This cycle will continue to deliver power to the output.

Output voltage detection is accomplished via R2, R1, Q2, and comparator A2 (V_{OUT} Comparator). Resistors R1 and R2 are sized so that when the SW voltage is 31.5V above V_{BAT}, the output of A2 goes high which resets the master latch. This disables Q1 and halts power delivery. NPN transistor Q3 is turned on pulling the $\overline{DONE}$ pin low, indicating that the part has finished charging. Power delivery can only be restarted by toggling the CHARGE pin.

The CHARGE pin gives full control of the part to the user. The charging can be halted at any time by bringing the CHARGE pin low. Only when the final output voltage is reached will the $\overline{DONE}$ pin go low. Figure 2 shows these various modes in action. When CHARGE is first brought high, charging commences. When CHARGE is brought low during charging, the part goes into shutdown and V_{OUT} no longer rises. When CHARGE is brought high again, charging resumes. When the target V_{OUT} voltage is reached, the $\overline{DONE}$ pin goes low and charging stops. Finally the CHARGE pin is brought low again so the part enters shutdown and the $\overline{DONE}$ pin goes high.

Both V_{BAT} and V_{IN} have undervoltage lockout (UVLO). When one of these pins goes below its UVLO voltage, the $\overline{DONE}$ pin goes low. With an insufficient bypass capacitor on V_{BAT} or V_{IN}, the ripple on the pin is likely to activate UVLO and terminate the charge. The applications circuits in the data sheet suggest values adequate for most applications.

The LT3485 V_{MONT} pin functions as an output to a microcontroller to communicate the progress of the charge. The V_{MONT} pin starts to function at about 0.2V, which corresponds to 64V with a turns ratio of 10.2. When the V_{MONT} pin is at 1V, the $\overline{DONE}$ pin goes low and the charging terminates. The pin's output is only valid when the part is charging.

The LT3485 also integrates an IGBT drive. The IGBTPWR pin supplies the power. The IGBT output goes high when IGBTIN goes high and conversely goes low when IGBTIN goes low. While IGBTIN is low, the IGBT drive draws no quiescent current from IGBTPWR.

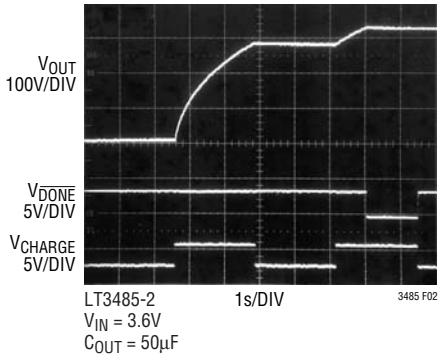


Figure 2. Halting the Charging Cycle with the CHARGE Pin

APPLICATIONS INFORMATION

Choosing the Right Device (LT3485-0/LT3485-1/LT3485-2/LT3485-3)

The only difference between the four versions of the LT3485 is the peak current level. For the fastest possible charge time, use the LT3485-3. The LT3485-1 has the lowest peak current capability, and is designed for applications that need a more limited drain on the batteries. Due to the lower peak current, the LT3485-1 can use a physically smaller transformer. The LT3485-0 and LT3485-2 have a current limit in between that of the LT3485-3 and the LT3485-1.

Transformer Design

The flyback transformer is a key element for any LT3485-0/LT3485-1/LT3485-2/LT3485-3 design. It must be designed carefully and checked that it does not cause excessive current or voltage on any pin of the part. The main parameters that need to be designed are shown in Table 1.

The first transformer parameter that needs to be set is the turns ratio N. The LT3485-0/LT3485-1/LT3485-2/LT3485-3 accomplish output voltage detection by monitoring the flyback waveform on the SW pin. When the SW voltage reaches 31.5V higher than the V_{BAT} voltage, the part will halt power delivery. Thus, the choice of N sets the target output voltage as it changes the amplitude of the reflected voltage from the output to the SW pin. Choose N according to the following equation:

$$N = \frac{V_{OUT} + 2}{31.5}$$

where V_{OUT} is the desired output voltage. The number 2 in the numerator is used to include the effect of the voltage drop across the output diode(s).

Thus for a 320V output, N should be 322/31.5 or 10.2. For a 300V output, choose N equal to 302/31.5 or 9.6.

The next parameter that needs to be set is the primary inductance, L_{PRI}. Choose L_{PRI} according to the following formula:

$$L_{PRI} \geq \frac{V_{OUT} \bullet 200 \bullet 10^{-9}}{N \bullet I_{PK}}$$

where V_{OUT} is the desired output voltage. N is the transformer turns ratio. I_{PK} is 1.4 (LT3485-0), 0.7 (LT3485-1), 1 (LT3485-2) and 2 (LT3485-3).

L_{PRI} needs to be equal or larger than this value to ensure that the LT3485-0/LT3485-1/LT3485-2/LT3485-3 has adequate time to respond to the flyback waveform.

All other parameters need to meet or exceed the recommended limits as shown in Table 1. A particularly important parameter is the leakage inductance, L_{LEAK}. When the power switch of the LT3485-0/LT3485-1/LT3485-2/LT3485-3 turns off, the leakage inductance on the primary of the transformer causes a voltage spike to occur on the SW pin. **The height of this spike must not exceed 40V**, even though the absolute maximum rating of the SW Pin is 50V. The 50V absolute maximum rating is a DC blocking voltage specification, which assumes that the current in the power NPN is zero. Figure 3 shows the SW voltage waveform for the circuit of Figure 8 (LT3485-0).

Table 1. Recommended Transformer Parameters

PARAMETER	NAME	TYPICAL RANGE LT3485-0	TYPICAL RANGE LT3485-1	TYPICAL RANGE LT3485-2	TYPICAL RANGE LT3485-3	UNITS
L_{PRI}	Primary Inductance	>5	>10	>7	>3.5	µH
L_{LEAK}	Primary Leakage Inductance	100 to 300	200 to 500	200 to 500	100 to 300	nH
N	Secondary: Primary Turns Ratio	8 to 12	8 to 12	8 to 12	8 to 12	
V_{ISO}	Secondary to Primary Isolation Voltage	>500	>500	>500	>500	V
I_{SAT}	Primary Saturation Current	>1.6	>0.8	>1.0	>2	A
R_{PRI}	Primary Winding Resistance	<300	<500	<400	<200	mΩ
R_{SEC}	Secondary Winding Resistance	<40	<80	<60	<30	Ω

APPLICATIONS INFORMATION

Note that the absolute maximum rating of the SW pin is not exceeded. Make sure to check the SW voltage waveform with V_{OUT} near the target output voltage, as this is the worst case condition for SW voltage. Figure 4 shows the various limits on the SW voltage during switch turn off.

It is important not to minimize the leakage inductance to a very low level. Although this would result in a very low leakage spike on the SW pin, the parasitic capacitance of the transformer would become large. This will adversely affect the charge time of the photoflash circuit.

Linear Technology has worked with several leading magnetic component manufacturers to produce pre-designed flyback transformers for use with the LT3485-0/LT3485-1/LT3485-2/LT3485-3. Table 2 shows the details of several of these transformers.

Capacitor Selection

For the input bypass capacitors, high quality X5R or X7R types should be used. Make sure the voltage capability of the part is adequate.

Output Diode Selection

The rectifying diode(s) should be low capacitance type with sufficient reverse voltage and forward current ratings. The peak reverse voltage that the diode(s) will see is approximately:

$$V_{PK-R} = V_{OUT} + (N \bullet V_{IN})$$

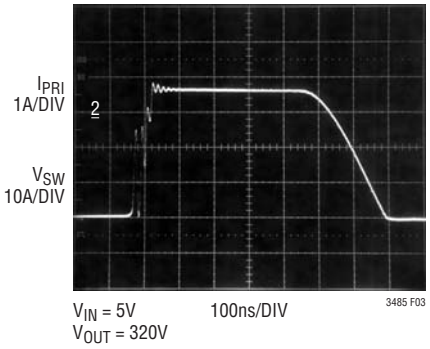


Figure 3. LT3485 SW Voltage Waveform

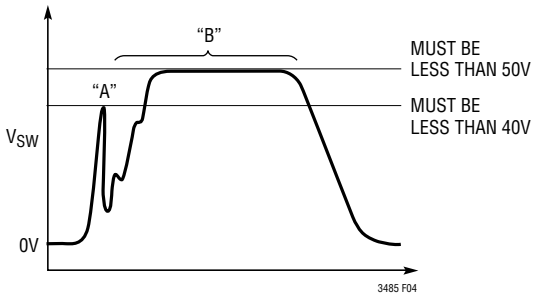


Figure 4. New Transformer Design Check (Not to Scale)

Table 2. Pre-Designed Transformers – Typical Specifications Unless Otherwise Noted

FOR USE WITH	TRANSFORMER NAME	SIZE (W × L × H) mm	L_{PRI} (µH)	LPRI-LEAKAGE (nH)	N	R_{PRI} (mΩ)	R_{SEC} (Ω)	VENDOR
LT3485-0/LT3485-2 LT3485-1	SBL-5.6-1 SBL-5.6S-1	5.6 × 8.5 × 4.0 5.6 × 8.5 × 3.0	10 24	200 Max 400 Max	10.2 10.2	103 305	26 55	Kijima Musen Hong Kong Office 852-2489-8266 (ph) kijimahk@netvigator.com (email)
LT3485-0 LT3485-1 LT3485-2 LT3485-3	LDT565630T-001 LDT565630T-002 LDT565630T-003 LDT565630T-041	5.8 × 5.8 × 3.0 5.8 × 5.8 × 3.0 5.8 × 5.8 × 3.0 5.8 × 5.8 × 3.0	6 14.5 10.5 4.7	200 Max 500 Max 550 Max 150 Max	10.4 10.2 10.2 10.4	100 Max 240 Max 210 Max 90 Max	10 Max 16.5 Max 14 Max 6.4 Max	TDK Chicago Sales Office (847) 803-6100 (ph) www.components.tdk.com
LT3485-0/LT3485-1 LT3485-1 LT3485-3	T-15-089 T-15-083 T-17-109A	6.4 × 7.7 × 4.0 8.0 × 8.9 × 2.0 6.5 × 7.9 × 4.0	12 20 5.9	400 Max 500 Max 300 Max	10.2 10.2 10.2	211 Max 675 Max 78 Max	27 Max 35 Max 18.61 Max	Tokyo Coil Engineering Japan Office 0426-56-6262 (ph) www.tokyo-coil.co.jp

APPLICATIONS INFORMATION

The peak current of the diode is simply:

$$I_{PK\text{-}SEC} = \frac{2}{N} \text{ (LT3485-3)}$$

$$I_{PK\text{-}SEC} = \frac{1.4}{N} \text{ (LT3485-0)}$$

$$I_{PK\text{-}SEC} = \frac{1}{N} \text{ (LT3485-2)}$$

$$I_{PK\text{-}SEC} = \frac{0.7}{N} \text{ (LT3485-1)}$$

For the circuit of Figure 8 with V_{BAT} of 5V, $V_{PK\text{-}R}$ is 371V and $I_{PK\text{-}SEC}$ is 137mA. The GSD2004S dual silicon diode is recommended for most LT3485-0/LT3485-1/LT3485-2/LT3485-3 applications. Another option is to use the BAV23S dual silicon diodes. Table 3 shows the various diodes and relevant specifications. Use the appropriate number of diodes to achieve the necessary reverse breakdown voltage.

IGBT Drive

The IGBT is a high current switch for the 100A+ current through the photoflash lamp. To create a redeye effect or to adjust the light output, the lamp current needs to be stopped, or quenched, with an IGBT before discharging the photoflash capacitor fully. The IGBT device also controls the 4kV trigger pulse required to ionize the xenon gas in the photoflash lamp. Figure 5 is a schematic of a fully functional photoflash application with the LT3485 serving as the IGBT drive. An IGBT drive charges the gate capacitance to start the flash. The IGBT drive does not need to pull-up the gate fast because of the inherently slow nature of the IGBT. A rise time of 2µs is sufficient to charge the gate of the IGBT and create a trigger pulse. With slower rise times, the trigger circuitry will not have a fast enough edge to create the required 4kV pulse. The fall time of the IGBT drive is critical to the safe operation of the IGBT. The IGBT gate is a network of resistors and capacitors, as shown in Figure 6. When the gate terminal is pulled low,

Table 3. Recommended Output Diodes

PART	MAX REVERSE VOLTAGE (V)	MAX FORWARD CONTINUOUS CURRENT (mA)	CAPACITANCE (pF)	VENDOR
GSD2004S (Dual Diode)	2x300	225	5	Vishay (402) 563-6866 www.vishay.com
BAV23S (Dual Diode)	2x250	225	5	Philips Semiconductor (800) 234-7381 www.philips.com
MMBD3004S (Dual Diode)	2x350	225	5	Diodes Inc (816) 251-8800 www.diodes.com

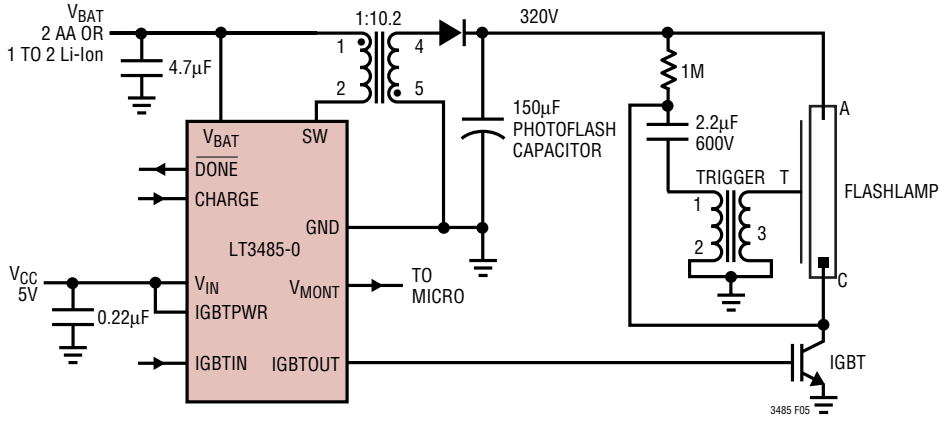


Figure 5. Complete Xenon Circuit

APPLICATIONS INFORMATION

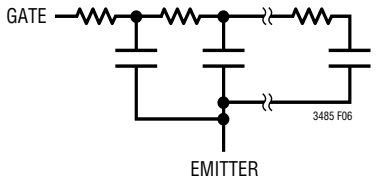


Figure 6. IGBT Gate

the capacitance closest to the terminal goes low but the capacitance further from the terminal remains high. This causes a small portion of the device to handle the full 100A of current, which quickly destroys the device. The pull down circuitry needs to pull down slower than the internal RC time constant in the gate of the IGBT. This is easily accomplished with a resistor in series with the IGBT drive, which is integrated into the LT3485.

The LT3485's integrated drive circuit is independent of the charging function. The IGBT section draws its power from the IGBTPWR pin. The rise and fall times are measured using a 4000pF output capacitor. The typical 10% to 90% rise time is 270ns. The drive pulls high to IGBTPWR. The typical 90% to 10% fall time is 180ns. The drive pulls down to 300mV. The IGBT driver pulls a peak of 150mA when driving an IGBT and 2mA of quiescent current. In the low state, the IGBT's quiescent current is less than 0.1μA.

Table 4 is a list of recommended IGBT devices for strobe applications. These three devices are all packaged in 8-lead TSSOP packages.

V_{OUT} Monitor

The voltage output monitor is a new feature to monitor the progress of capacitor charging with a microcontroller. The monitor uses the flyback waveform to output a voltage proportional to the output of the flyback converter. The output monitor voltage range for the pin is 0V to 1V. The 1V output corresponds with the charge cycle terminating and the $\overline{\text{DONE}}$ pin going low. The voltage output monitor is only functional when the circuit is charging ($\overline{\text{DONE}}$ and CHARGE are high.)

Table 4. Recommended IGBTs

PART	DRIVE VOLTAGE (V)	BREAKDOWN VOLTAGE (V)	COLLECTOR CURRENT (PULSED) (A)	VENDOR
CY25BAH-8F CY25BAJ-8F	2.5 4	400 400	150 150	Renesas (408) 382-7500 www.renesas.com
GT8G133	4	400	150	Toshiba Semiconductor (949) 623-2900 www.semicon.toshiba.co.jp/eng/

APPLICATIONS INFORMATION

Board Layout

The high voltage operation of the LT3485-0/LT3485-1/ LT3485-2/LT3485-3 demands careful attention to board layout. You will not get advertised performance with careless layout. Figure 7 shows the recommended component placement. Keep the area for the high voltage end of the secondary as small as possible. Also note the larger than minimum spacing for all high voltage nodes in order to meet breakdown voltage requirements for the circuit board. *It is imperative to keep the electrical path formed by C1, the primary of T1, and the LT3485-0/LT3485-1/ LT3485-2/LT3485-3 as short as possible.* If this path is haphazardly made long, it will effectively increase the leakage inductance of T1, which may result in an overvoltage condition on the SW pin.

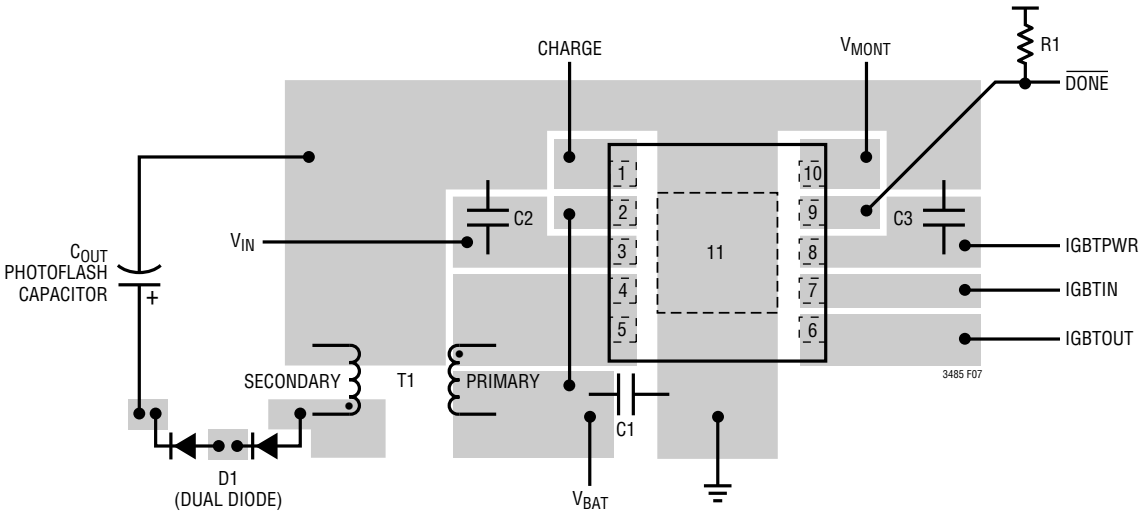
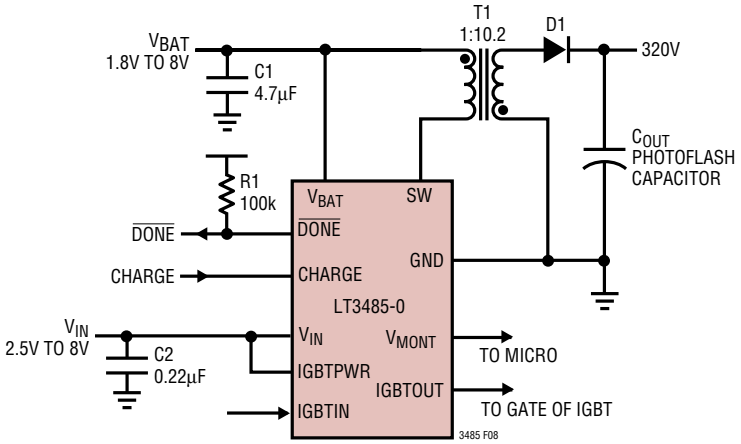


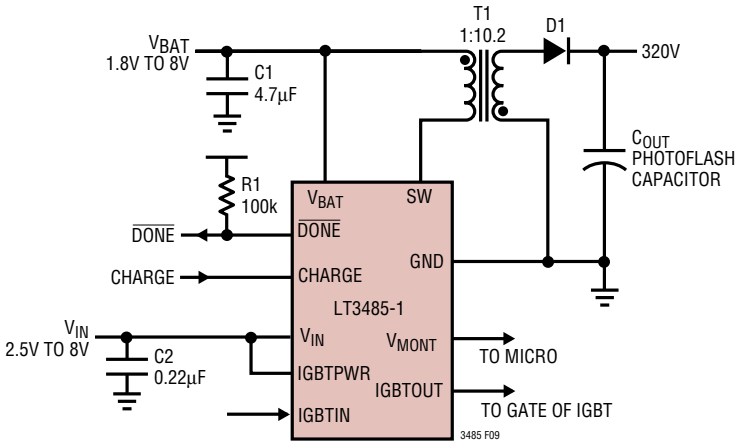
Figure 7. Suggested Layout: Keep Electrical Path Formed by C1, Transformer Primary and LT3485-0/LT3485-1/LT3485-2/LT3485-3 Short

TYPICAL APPLICATIONS



C1: 4.7µF, X5R OR X7R, 10V
C2: 0.22µF, X5R or X7R, 10V
T1: KIJIMA MUSEN PART# SBL-5.6-1, L_{PRI} = 10µH, N = 10.2
D1: DIODES INC MMBD3004S DUAL DIODE CONNECTED IN SERIES
R1: PULL UP RESISTOR NEEDED IF DONE PIN USED

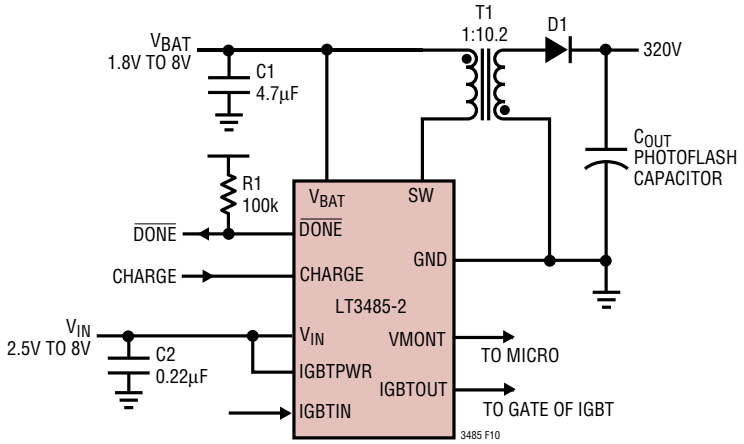
Figure 8. LT3485-0 Photoflash Charger Uses High Efficiency 4mm Tall Transformer



C1: 4.7µF, X5R OR X7R, 10V
C2: 0.22µF, X5R or X7R, 10V
T1: KIJIMA MUSEN PART# SBL-5.6S-1, L_{PRI} = 24µH, N = 10.2
D1: DIODES INC MMBD3004S DUAL DIODE CONNECTED IN SERIES
R1: PULL UP RESISTOR NEEDED IF DONE PIN USED

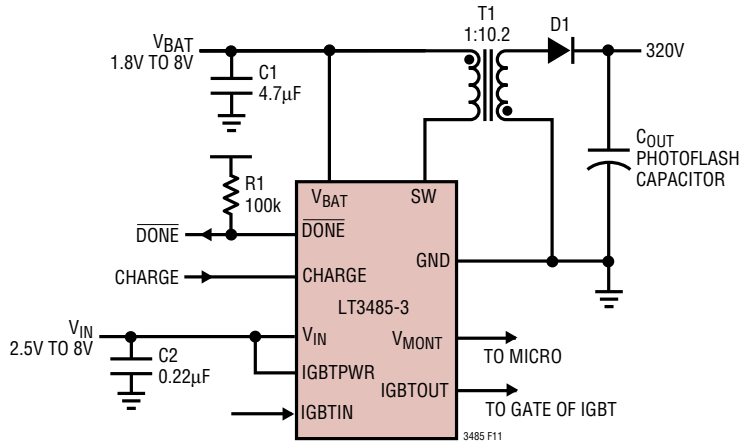
Figure 9. LT3485-1 Photoflash Charger Uses High Efficiency 3mm Tall Transformer

TYPICAL APPLICATIONS



C1: 4.7µF, X5R OR X7R, 10V
C2: 0.22µF, X5R or X7R, 10V
T1: KIJIMA MUSEN PART# SBL-5.6-1, L_{PRI} = 10µH, N = 10.2
D1: DIODES INC MMBD3004S DUAL DIODE CONNECTED IN SERIES
R1: PULL UP RESISTOR NEEDED IF DONE PIN USED

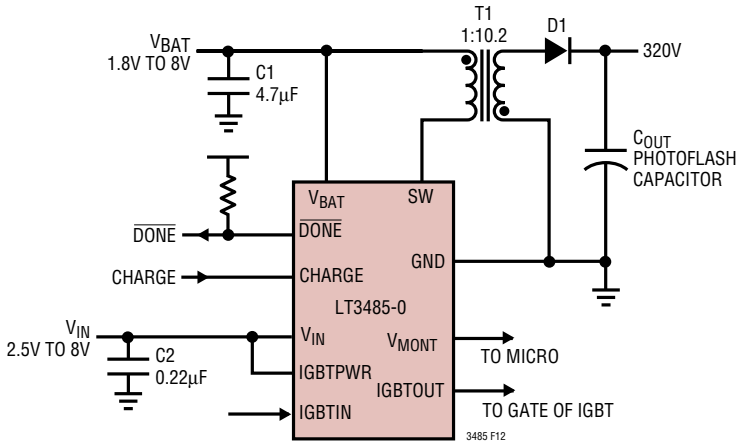
Figure 10. LT3485-2 Photoflash Charger Uses High Efficiency 4mm Tall Transformer



C1: 4.7µF, X5R OR X7R, 10V
C2: 0.22µF, X5R or X7R, 10V
T1: TDK LDT565630T-041, L_{PRI} = 4.7µH, N = 10.4
D1: DIODES INC MMBD3004S DUAL DIODE CONNECTED IN SERIES
R1: PULL UP RESISTOR NEEDED IF DONE PIN USED

Figure 11. LT3485-3 Photoflash Charger Uses High Efficiency 3mm Tall Transformer

TYPICAL APPLICATIONS



C1: 4.7µF, X5R OR X7R, 10V
C2: 0.22µF, X5R or X7R, 10V
T1: TDK LDT565630T-001, L_{PRI} = 6µH, N = 10.4
D1: DIODES INC MMBD3004S DUAL DIODE CONNECTED IN SERIES
R1: PULL UP RESISTOR NEEDED IF DONE PIN USED

Figure 12. LT3485-0 Photoflash Circuit Uses Tiny 3mm Tall Transformer

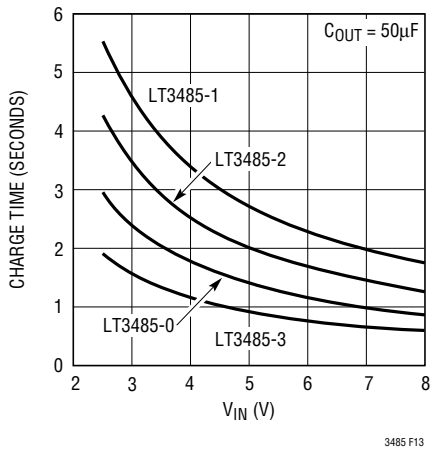
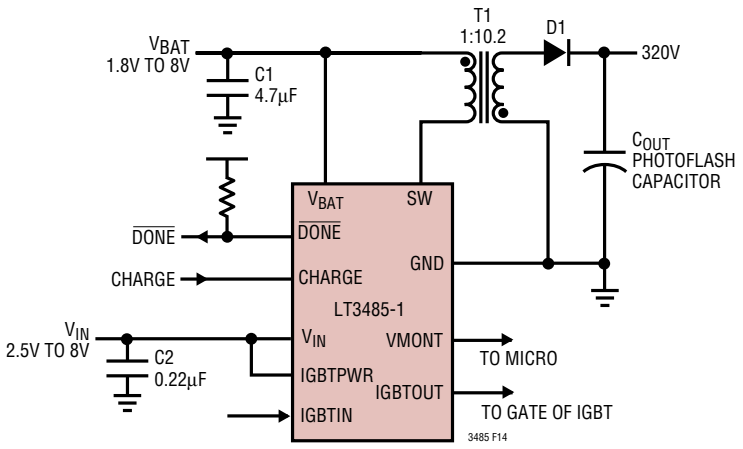


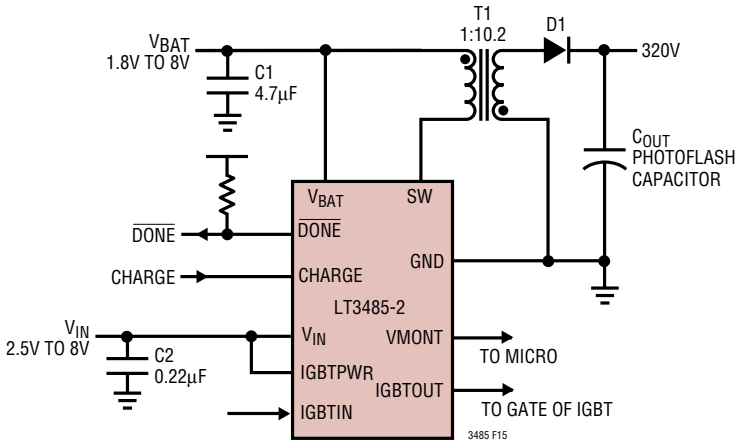
Figure 13. Charge Time with TDK Transformers (Figures 11, 12, 13, 14 and 15)

TYPICAL APPLICATIONS



C1: 4.7µF, X5R OR X7R, 10V
C2: 0.22µF, X5R or X7R, 10V
T1: TDK LDT565630T-002, L_{PRI} = 14.5µH, N = 10.2
D1: DIODES INC MMBD3004S DUAL DIODE CONNECTED IN SERIES
R1: PULL UP RESISTOR NEEDED IF DONE PIN USED

Figure 14. LT3485-1 Photoflash Circuit Uses Tiny 3mm Tall Transformer

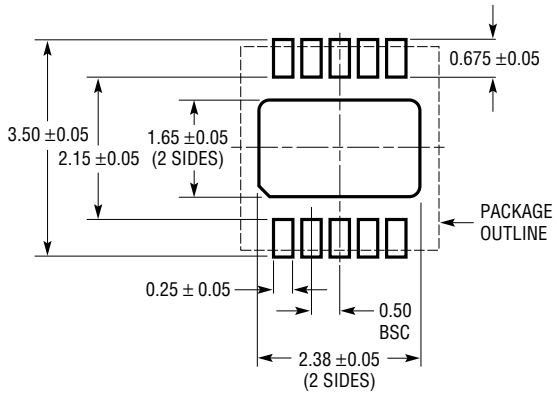


C1: 4.7µF, X5R OR X7R, 10V
C2: 0.22µF, X5R or X7R, 10V
T1: TDK LDT565630T-003, L_{PRI} = 10µH, N = 10.2
D1: DIODES INC MMBD3004S DUAL DIODE CONNECTED IN SERIES
R1: PULL UP RESISTOR NEEDED IF DONE PIN USED

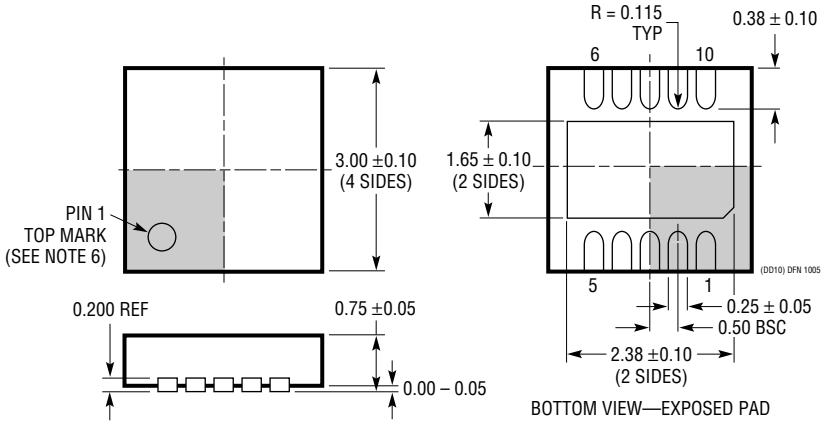
Figure 15. LT3485-2 Photoflash Circuit Uses Tiny 3mm Tall Transformer

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3407	Dual 600mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} <1µA, MS10E
LT3420/LT3420-1	1.4A/1A, Photoflash Capacitor Chargers with Automatic Top-Off	Charges 220µF to 320V in 3.7 seconds from 5V, V_{IN}: 2.2V to 16V, I_Q = 90µA, I_{SD} < 1µA, MS10
LTC3425	5A I_{SW}, 8MHz, Multi-Phase Synchronous Step-Up DC/DC Converter	95% Efficiency, V_{IN}: 0.5V to 4.5V, $V_{OUT(MIN)}$ = 5.25V, I_Q = 12µA, I_{SD} < 1µA, QFN-32
LTC3440	600mA/1A (I_{OUT}), Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V to 5.5V, I_Q = 25µA, I_{SD} < 1µA, MS-10 DFN-12
LT3468/LT3468-1/ LT3468-2	Photoflash Capacitors in ThinSOT™	Charges 110µF to 320V in 4.6 Seconds from 3.6V, V_{IN}: 2.5V to 16V, I_Q = 5mA, I_{SD} < 1µA, ThinSOT
LT3472	Dual ±34V, 1.2MHz Boost (350mA)/Inverting (400mA) DC/DC Converter for CCD Bias	Integrated Schottkys, V_{IN}: 2.2V to 16V, $V_{OUT(MAX)}$ = ±34V, I_Q = 2.5mA, I_{SD} < 1µA, DFN
LT3463/LT3463A	Dual Boost (250mA)/Inverting (250mA/400mA) DC/DC Converter for CCD Bias	Integrated Schottkys, V_{IN}: 2.3V to 15V, $V_{OUT(MAX)}$ = ±40V, I_Q = 40µA, I_{SD} < 1µA, DFN
LT3484-0/LT3484-1/ LT3484-2	Photoflash Capacitor Chargers	Charges 110µF to 320V in 4.6 Seconds from 3.6V, V_{IN}: 2.5V to 16V, V_{BAT}: 1.8V to 16V, I_Q = 5mA, I_{SD} < 1µA, 2mm × 3mm DFN

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