

### Description

The Si4688 single-chip digital receiver is one member of a family of 100% CMOS digital radio broadcast receiver ICs from Silicon Labs. The Si468x family offers a complete and cost-effective digital radio solution integrating the RF tuner, baseband, and audio processing on a single die. The high level of integration provides significant customer benefits compared to traditional digital radio solutions, including a reduction in system implementation complexity, validation and testing, and improved reliability and manufacturability.

The Si4688 is compatible with the iBiquity Digital and NRSC-5 standards for FM In-Band-On-Channel (IBOC) digital radio broadcasting, integrating digital channel demodulation and decoding functions, along with audio decoding and IBOC analog-digital blend. The Si4688 supports IBOC multicasting, as well as the full-range of HD Radio data services, such as PSD, Artist Experience, iTunes® Tagging, Bookmark and real-time Traffic, with the appropriate external decoders.

The Si4688 also offers VHF Band III (168–240 MHz) reception capability and is fully compliant with ETSI EN 300 401 and ETSI TS 102 563. The Si4688 delivers DAB and DAB+ via an integrated source decoder that supports both MPEG Audio Layer 2 (DAB) and HE-AAC V2 (DAB+). The Si4688 supports data services such as Dynamic Labels, Intellitext, Electronic Program Guide (EPG), Slideshow, and Journaline® with the appropriate external decoders.

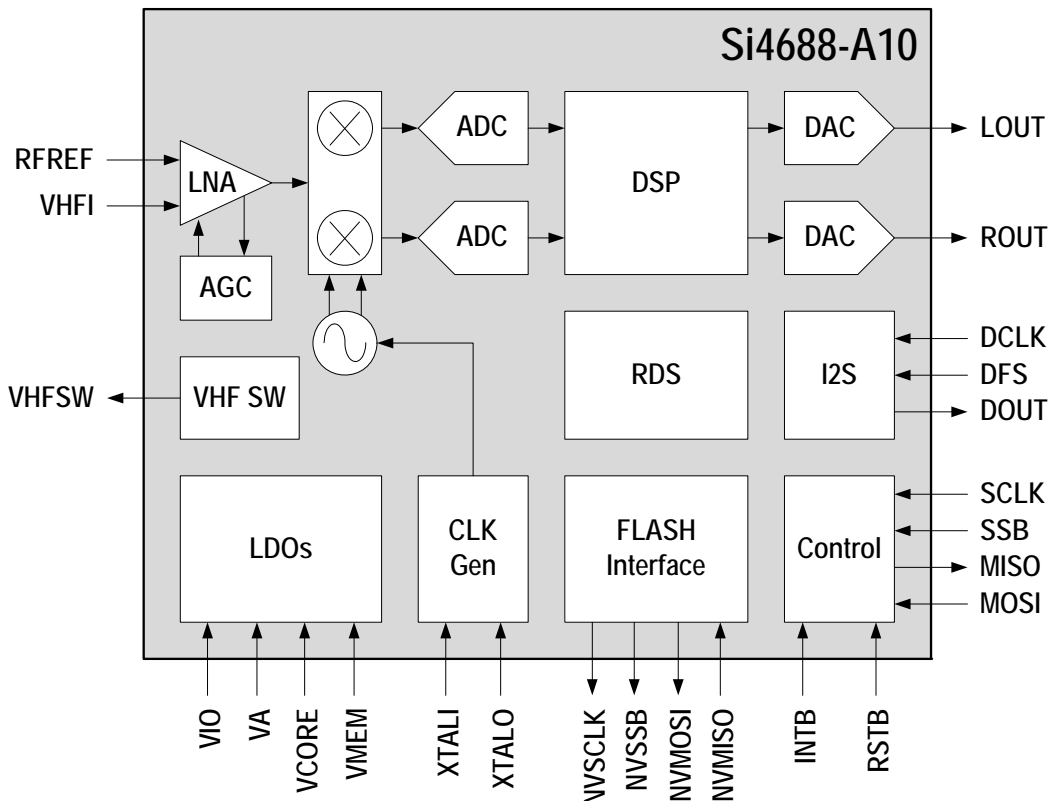
[For more information, visit the Si468x Digital Radio Receivers web page.](#)

### Features

- Worldwide FM band support (76–108 MHz)
- Advanced RDS/RBDS decoder
- FM HD Radio™ support with on-chip IBOC blend
- DAB, DAB+ Band III support (168–240 MHz)
- Supports WorldDMB Receiver Profiles 1 and 2
- Integrated OFDM channel demodulator
- Integrated de-interleaving SRAM
- I<sup>2</sup>S digital audio out with ASRC
- Integrated 97 dB stereo audio DAC
- Concurrent I<sup>2</sup>S/L-R stereo audio out
- Full range of signal quality metrics
- Fully-integrated VCO / PLL / synthesizer
- SPI and I<sup>2</sup>C host control interfaces
- WLCSP 62-ball, 3.2x3.77x0.59 mm
- QFN 48-pin, 7x7x0.85 mm

### Applications

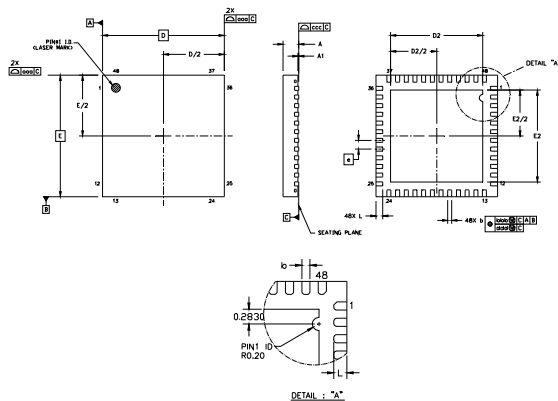
- Mobile phones and tablets
- Clock and tabletop radios
- Stereo boomboxes
- Mini/micro systems
- Docking stations
- Personal navigation devices



### Selected Electrical Specifications

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Ambient Temperature	$T_A$		-40	25	85	°C
Analog Supply Voltage	$V_A$		1.71	1.8	2.0	V
Interface Supply Voltage	$V_{IO}$		1.62	1.8	3.6	V
Core Digital Supply Voltage	$V_{CORE}$		1.62	1.8	2.0	V
Memory Supply Voltage	$V_{MEM}$		1.62	1.8	2.0	V
<b>Analog FM</b>						
Input Frequency	$F_{rf}$		76	—	108	MHz
Seek Time			—	—	60	ms/ch
Input IP3			—	96	—	dB $\mu$ V
Sensitivity		SINAD = 26 dB		0.7		$\mu$ V
<b>FM HD</b>						
Input Frequency	$F_{rf}$		87.5	—	108	MHz
Seek Time			—	—	120	ms/ch
<b>DAB/DAB+</b>						
Input Frequency	$F_{rf}$		168	—	240	MHz
Enable Acquisition Time			—	—	940	ms

**Si4688-A10-GM (QFN)**

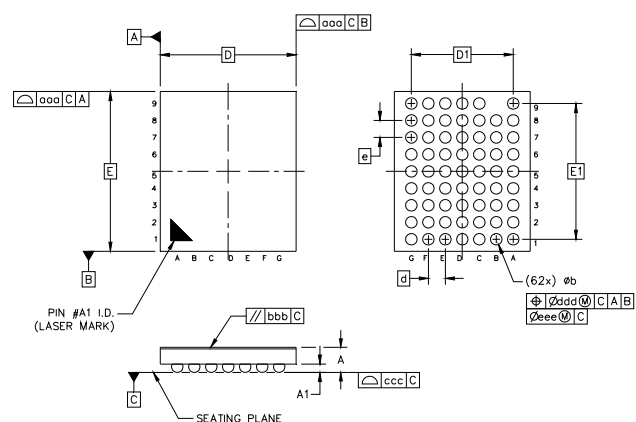


Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		7.00 BSC	
D2	5.20	5.30	5.40
e		0.50 BSC	
E		7.00 BSC	
E2	5.20	5.30	5.40
L	0.30	0.40	0.50
aaa		0.15	
bbb		0.10	
ddd		0.05	
eee		0.08	

**Notes:**

- All dimensions are shown in millimeters (mm) unless otherwise noted.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing conforms to JEDEC Outline MO-220, Variation VKKD-4.
- Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

**Si4688-A10-GD (WLCSP)**



Dimension	Min	Nom	Max
A	0.55	0.59	0.63
A1	0.18	0.20	0.22
b	0.22	0.27	0.32
D		3.20 BSC.	
E		3.77 BSC.	
d		0.40 BSC.	
e		0.40 BSC.	
D1		2.40 BSC.	
E1		3.20 BSC.	
aaa		0.10	
bbb		0.10	
ccc		0.03	
ddd		0.15	
eee		0.05	

**Notes:**

- All dimensions shown are in millimeters (mm) unless otherwise noted.
- Dimensioning and Tolerancing per ANSI Y14.5M-1994.
- Primary datum "C" and seating plane are defined by the spherical crowns of the solder balls.
- Dimension "b" is measured at the maximum solder bump diameter, parallel to primary datum "C".
- Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



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