

SN54ALS113A, SN74ALS113A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

SDAS200 – D2661, APRIL 1982 – REVISED MAY 1986

- Fully Buffered to Offer Maximum isolation from External Disturbance
- Package Options Include Plastic Small Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS113A	40 MHz ($C_L=15$ pF)	6 mW

description

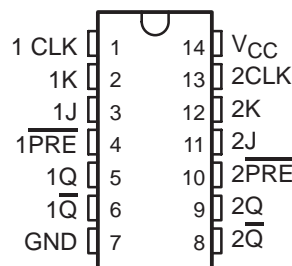
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset input sets the outputs regardless of the levels of the other inputs. When Preset \overline{PRE} is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54ALS113A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS113A is characterized for operation from 0°C to 70°C .

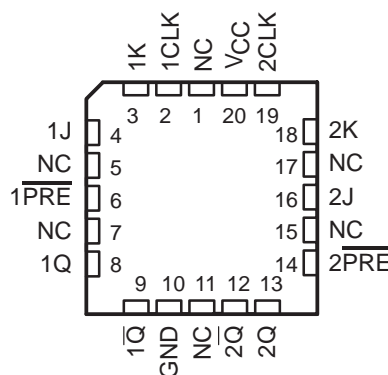
FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLK	J	K	Q	\overline{Q}
L	X	X	X	H	L
H	\downarrow	L	L	Q_0	\overline{Q}_0
H	\downarrow	H	L	H	L
H	\downarrow	L	H	L	H
H	\downarrow	H	H	TOGGLE	
H	H	X	X	Q_0	\overline{Q}_0

SN54ALS113A . . . J PACKAGE
SN74ALS113A . . . D OR N PACKAGE
(TOP VIEW)

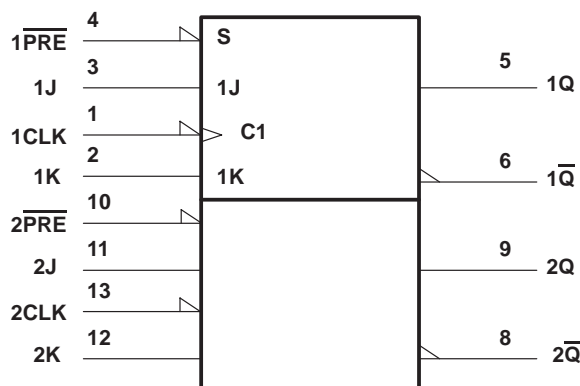


SN54ALS113A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



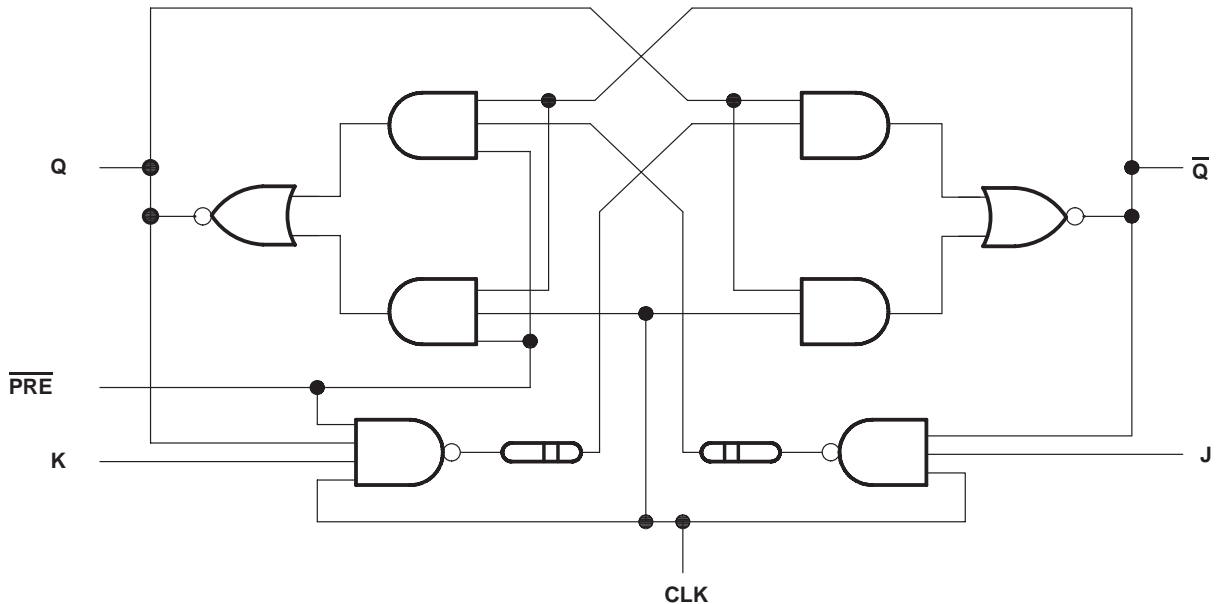
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS113A	-55°C to 125°C
SN74ALS113A	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS113A			SN74ALS113A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			4			8	mA
f_{clock}	Clock frequency	0		25	0		30	mHz
t_w	Pulse duration	PRE low		20		10		ns
		CLK high		20		16.5		
		CLK low		20		16.5		
t_{su}	Setup time before CLK↓	Data		25		22		ns
		PRE inactive		20		20		
t_h	Hold time, data after CLK↓		0			0		ns
T_A	Operating free-air temperature		-55	125		0	70	°C

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electrical characteristic over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS113A		SN74ALS113A		UNIT		
		MIN	TYP†	MAX	MIN		TYP†	MAX
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.5		-1.5	V	
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} -2		V _{CC} -2			V	
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 4 mA		0.25	0.4		0.25 0.4	V	
	V _{CC} = 4.5 V, I _{OL} = 8 mA					0.35 0.5		
I _I	J, K, or CLK PRE	V _{CC} = 5.5 V, V _I = 7 V		0.1		0.1	mA	
				0.2		0.2		
I _{IH}	J, K, or CLK PRE	V _{CC} = 5.5 V, V _I = 2.7 V		20		20	μA	
				40		40		
I _{IL}	J, K, or CLK PRE	V _{CC} = 5.5 V, V _I = 0.4 V		-0.2		-0.2	mA	
				-0.4		-0.4		
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V	-30		-112	-30		-112	mA
I _{CC}	V _{CC} = 5.5 V, See Note 1		2.5	4.5		2.5 4.5	mA	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

NOTE 1: I_{CC} is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX				UNIT
			SN54ALS113A		SN74ALS113A		
			MIN	MAX	MIN	MAX	
f _{max}			25		30	MHz	
t _{PLH}	PRE	Q or Q̄	3	23	3	14	ns
t _{PHL}			4	26	4	18	
t _{PLH}	CLK	Q or Q̄	3	22	3	15	ns
t _{PHL}			5	23	5	19	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



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