High-Speed CMOS 512/1K/2K/4K x 9 Parallel Clocked FIFO

QS72211
QS72221
QS72231
QS72241

FEATURES

- 512 x 9 (QS72211)
- 1K x 9 (QS72221)
- 2K x 9 (QS72231)
- 4K x 9 (QS72241)
- Ultra-high speed 12-ns (83 MHz) read/write cycle times
- Synchronous/asynchronous read and write
- Industry-standard pinouts
- Four flag signals
  - Empty flag
  - Full flag
  - Programmable Almost-Empty flag defaults to EMPTY+7
  - Programmable Almost-Full flag defaults to FULL–7
- Output Enable ($\overline{OE}$) pin
- Available in 32-pin PLCC

DESCRIPTION

The QS72211/221/231/241 are high-speed 512/1K/2K/4K x 9 parallel, clocked FIFOs, respectively. These FIFOs have 9-bit input and output ports. The input port is controlled by a free running clock (WCLK) and two write enable pins ($\overline{WEN1}$, WEN2). The output port is controlled by another clock pin (RCLK) and two read enable pins ($\overline{REN1}$, $\overline{REN2}$). An output enable pin ($\overline{OE}$) is provided on the read port for HIGH-Z control of the output. These FIFOs also have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$), which prevent the FIFO from being written into when full or being read from when empty. There are two additional programmable flags, Almost-Empty flag ($\overline{PAE}$) and Almost-Full flag ($\overline{PAF}$) for improved system control. The programmable flags default to EMPTY+7 and FULL-7 for $\overline{PAE}$ and $\overline{PAF}$, respectively. The programmable flag offset loading is controlled by asserting the load pin ($\overline{LD}$). These FIFOs are easily cascadable to any depth and expandable to any width without any speed penalty and are useful for data communications, digital filtering, processor communication, and video line-doubling applications.

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

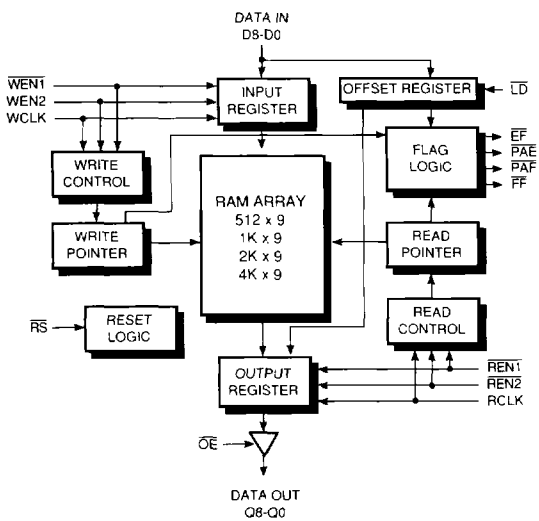


FIGURE 2. QS722X1 PINOUT, 32-PIN PLCC (All pins top view)

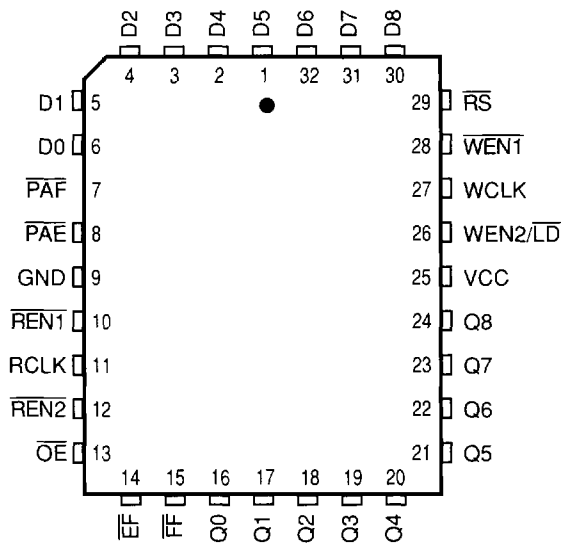


TABLE 1. PIN DESCRIPTIONS

Name	I/O	Function	Description
D8-D0	I	Data Inputs	Nine inputs for the memory array or offset registers.
$\overline{PAE}$	O	Programmable Almost-Empty Flag	When the signal goes LOW, it indicates the array is almost empty, based on the offset value in the almost-empty offset registers. The default value is EMPTY+7. $\overline{PAE}$ transition is synchronous with RCLK.
$\overline{PAF}$	O	Programmable Almost-Full Flag	When the signal goes LOW, it indicates the array is almost full, based on the offset value in the almost-full offset registers. The default value is FULL–7. $\overline{PAF}$ transition is synchronous with WCLK.
RCLK	I	Read Clock	Data are read from the FIFO when $\overline{REN1}$ and $\overline{REN2}$ are LOW on the rising edge of RCLK. The $\overline{EF}$ and $\overline{PAE}$ transitions are synchronized to the RCLK.
$\overline{REN1}$ $\overline{REN2}$	I	Read Enable	When $\overline{REN1}$ and $\overline{REN2}$ are LOW on the rising edge of RCLK, data will be read from the FIFO.
$\overline{OE}$	I	Output Enable	The outputs are in an active state when $\overline{OE}$ is LOW. If $\overline{OE}$ is HIGH, the outputs will be in the high-impedance state.
$\overline{EF}$	O	Empty Flag	The $\overline{EF}$ is LOW when the array is empty and further data reads are inhibited. The $\overline{EF}$ is synchronized to RCLK. When $\overline{EF}$ is HIGH, the FIFO is not empty, and the data can be read from the FIFO.
$\overline{FF}$	O	Full Flag	The $\overline{FF}$ is LOW when the array is full and further data writes are inhibited. The $\overline{FF}$ is synchronized to WCLK. When $\overline{FF}$ is HIGH, data can be written into the FIFO until the FIFO is full.
Q8-Q0	O	Data Outputs	Data are read from the FIFO memory on these outputs.
WEN2/ $\overline{LD}$	I	Write Enable 2/ Register Load	If WEN2/$\overline{LD}$ is LOW during the reset operation, this signal will subsequently function as an $\overline{LD}$ pin to control offset register load and read operations. If WEN2/$\overline{LD}$ is HIGH during the reset operation, this signal will function as WEN2, a second active HIGH write enable pin.
WCLK	I	Write Clock	Data are written into the FIFO on the rising edge of WCLK if $\overline{WEN1}$ and WEN2 are asserted. The $\overline{FF}$ and $\overline{PAF}$ transitions are synchronized to the WCLK.
$\overline{WEN1}$	I	Write Enable 1	When $\overline{WEN1}$ is LOW and WEN2 is HIGH on the rising edge of WCLK, data will be written into the FIFO.
$\overline{RS}$	I	Reset	When $\overline{RS}$ is LOW the read and write pointers are set to the first location and all offset registers are reset to the default value. The output register is also initialized to zero. After the device is powered up, a reset is required before a write operation can take place.
Vcc			+5V Power Supply
GND			Ground at 0V

FUNCTIONAL DESCRIPTION

Reset ($\overline{RS}$)
A reset is initiated by bringing $\overline{RS}$ LOW. A reset is required after power-up before a write operation can take place.
During reset, the following occurs:
1) The internal read and write pointers are set to the first physical location.
2) The output register is initialized to zero.
3) The offset registers are initialized to their default values.
4) The Empty flag ($\overline{EF}$) and Programmable Almost-Empty flag ($\overline{PAE}$) will reset to LOW.
5) The Full flag ($\overline{FF}$) and Programmable Almost-Full flag ($\overline{PAF}$) will reset to HIGH.
6) WEN2/$\overline{LD}$ signal is configured during reset.

Read Enables ($\overline{REN1}$), ($\overline{REN2}$)
New data are read from the FIFO when $\overline{REN1}$ and $\overline{REN2}$ are both LOW during the rising edge of RCLK. If either read enable is HIGH, then the outputs will retain the previous data. When the FIFO is empty, then the read enable signals are ignored.

Read Clock (RCLK)
When the read enable pins are both LOW, new data can be read from the FIFO on the LOW-to-HIGH transition of the read clock (RCLK). The Empty flag ($\overline{EF}$) and Programmable Almost-Empty flag ($\overline{PAE}$) are synchronized to the rising edge of the read clock (RCLK).

Output Enable ($\overline{OE}$)
When output enable ($\overline{OE}$) is LOW, the parallel output buffers receive data from the output register independent of other input signals. The output data bus will go to a high-impedance state when the output enable ($\overline{OE}$) goes HIGH. The flag outputs are not affected by output enable ($\overline{OE}$).

Data-In (D8-D0)
Nine-bit-wide data bus input for writing the FIFO array.

Write Enable 1 ($\overline{WEN1}$)
When the FIFO is configured with the ability to program the offset registers then $\overline{WEN1}$ is the only write enable signal. In this mode, when $\overline{WEN1}$ is LOW on the rising edge of the write clock, then data are written into the FIFO at the next sequential location. In this mode, when $\overline{WEN1}$ and $\overline{LD}$ are LOW on the rising edge of the write clock (WCLK), then data are written into a programmable offset register.

When the FIFO is configured to have two write enable pins, then data is written into the FIFO at the next sequential location when $\overline{WEN1}$ is LOW and WEN2 is HIGH on the rising edge of the write clock (WCLK). When the FIFO is full, the $\overline{WEN1}$ signal is ignored except for loading offsets.

Write Clock (WCLK)
A write occurs on the LOW-to-HIGH transition of the write clock (WCLK) when writing is enabled. All setup and hold times are with respect to this transition. The Full flag ($\overline{FF}$) and Programmable Almost-Full flag ($\overline{PAF}$) are synchronized to the rising edge of the write clock (WCLK). The write and read clocks can be tied together and driven by one external clock input, or they can be supplied by separate asynchronous clock inputs.

Write Enable 2 (WEN2)/Load ($\overline{LD}$)
This signal can function as a second write enable (WEN2) or as an offset register load/read control pin ($\overline{LD}$). If WEN2 /$\overline{LD}$ is HIGH during reset, then this signal functions as WEN2. If WEN2/$\overline{LD}$ is LOW during reset, then this signal functions as $\overline{LD}$. When this pin is configured as a second write enable pin (WEN2), then a write occurs when $\overline{WEN1}$ is LOW and WEN2 is HIGH on the rising edge of the write clock (WCLK).

When the FIFO is full then the WEN2 signal is ignored except for loading registers. Having a second write enable pin allows for depth expansion. To allow programming of the offset registers WEN2/$\overline{LD}$ must be configured as an $\overline{LD}$ pin. There are four 9-bit offset registers, two registers for controlling the Programmable Almost-Empty flag ($\overline{PAE}$) and two registers for controlling the Programmable Almost-Full flag ($\overline{PAF}$).

When $\overline{LD}$ and $\overline{WEN1}$ are LOW, data are written to the least-significant bits, LSB almost-empty register on the first LOW-to-HIGH transition of the write clock. Data are written into the most significant bits, MSB, almost-empty register on the next LOW-to-HIGH transition of the write clock, and into the LSB almost-full register on the next transition and into the MSB almost-full register on the next transition. If more WCLK transitions occurred, the sequence would wrap around through the same sequence. When programming of the offset registers is interrupted, then the next register in sequence will be accessed when programming is resumed. In a similar fashion, the offset registers are read when both read enables $\overline{REN1}$, $\overline{REN2}$ and $\overline{LD}$ are LOW on the LOW-to-HIGH transition of the read clock (RCLK). The offset register

sequence is the same as stated for programming the registers. Simultaneous write and read operations to the offset registers are not allowed.

Output Data (Q8-Q0)
Memory array data and programmable offsets are read from these nine outputs.

Empty Flag ($\overline{EF}$)
When the read and write pointer are at the same location in the FIFO array, signifying that the FIFO is empty, the Empty flag ($\overline{EF}$) goes LOW. The Empty flag is synchronized to the rising edge of the read clock (RCLK).

Full Flag ($\overline{FF}$)
When the Full flag ($\overline{FF}$) goes LOW, then further write operations are inhibited. The Full flag is synchronized to the rising edge of the write clock (WCLK).

Programmable Almost-Empty Flag ($\overline{PAE}$)
The Programmable Almost-Empty flag ($\overline{PAE}$) is LOW after a reset pulse and will go HIGH when the write pointer is N+1 locations ahead of the read pointer where N is the value in the empty offset register. The default value for N is 7. The Programmable Almost-Empty flag ($\overline{PAE}$) is synchronized to the rising edge of the read clock (RCLK).

Programmable Almost-Full Flag ($\overline{PAF}$)
The Programmable Almost-Full flag ($\overline{PAF}$) goes LOW on the subsequent LOW-to-HIGH transition of the write clock (WCLK) when the write pointer becomes (FULL–N) locations ahead of the read pointer, where N is the value in the full offset register. The default value for N is 7.

TABLE 2. WRITE OFFSET REGISTER

Operation	$\overline{WEN1}$	WCLK	$\overline{LD}$
No Operation	1	↑	1
Write in FIFO	0	↑	1
No Operation	1	↑	0
Empty Offset LSB	0	↑	0
Empty Offset MSB	0	↑	0
Full Offset LSB	0	↑	0
Full Offset MSB	0	↑	0

Note:
The same sequence applies for reading the offset registers.

TABLE 3. LOCATION OF DATA IN OFFSET REGISTERS

QS72211 512 x 9 BIT Synchronous FIFO Registers									
Data Inputs	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Empty LSB Offset	X	•	•	•	•	•	•	•	L
Empty MSB Offset	X	X	X	X	X	X	X	X	M
Full LSB Offset	X	•	•	•	•	•	•	•	L
Full MSB Offset	X	X	X	X	X	X	X	X	M

QS72221 1K x 9 BIT Synchronous FIFO Registers									
Data Inputs	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Empty LSB Offset	X	•	•	•	•	•	•	•	L
Empty MSB Offset	X	X	X	X	X	X	X	M	•
Full LSB Offset	X	•	•	•	•	•	•	•	L
Full MSB Offset	X	X	X	X	X	X	X	M	•

QS72231 2K x 9 BIT Synchronous FIFO Registers									
Data Inputs	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Empty LSB Offset	X	•	•	•	•	•	•	•	L
Empty MSB Offset	X	X	X	X	X	X	M	•	•
Full LSB Offset	X	•	•	•	•	•	•	•	L
Full MSB Offset	X	X	X	X	X	X	M	•	•

QS72241 4K x 9 BIT Synchronous FIFO Registers									
Data Inputs	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Empty LSB Offset	X	•	•	•	•	•	•	•	L
Empty MSB Offset	X	X	X	X	X	M	•	•	•
Full LSB Offset	X	•	•	•	•	•	•	•	L
Full MSB Offset	X	X	X	X	X	M	•	•	•

Notes:
1. L signifies LSB of data in offset registers.
2. M signifies MSB of data in offset registers.
3. X signifies do not care bit in offset registers.
4. The default value for both registers is 0007H.

TABLE 4. STATUS OF FIFO FLAGS

QS72211	QS72221	$\overline{EF}$	$\overline{PAE}$	$\overline{PAF}$	$\overline{FF}$
0	0	L	L	H	H
1 to l	1 to l	H	L	H	H
(l + 1) to (512 – (J + 1))	(l + 1) to (1024 – (J + 1))	H	H	H	H
(512 – J) to 511	(1024 – J) to 1023	H	H	L	H
512	1024	H	H	L	L

QS72231	QS72241	$\overline{EF}$	$\overline{PAE}$	$\overline{PAF}$	$\overline{FF}$
0	0	L	L	H	H
1 to l	1 to l	H	L	H	H
(l + 1) to (2048 – (J + 1))	(l + 1) to (4096 – (J + 1))	H	H	H	H
(2048 – J) to 2047	(4096 – J) to 4095	H	H	L	H
2048	4096	H	H	L	L

Note:
l is the value in the empty offset register, and J is the value in the full offset register. The default value for l and J is 7.

TABLE 5. POWER SUPPLY CHARACTERISTICS

Parameter	Description	Test Conditions	722X1-12	722X1-15	722X1-20	Units
I_{CC}[1]	Operating Current	Vcc = Max, I_{OUT} = 0 mA	150	125	100	mA
I_{SB}[2]	Standby Current	Vcc = Max, I_{OUT} = 0 mA	5	5	5	mA

Parameter	Description	Test Conditions	722X1-25	722X1-35	722X1-50	Units
I_{CC}[1]	Operating Current	Vcc = Max, I_{OUT} = 0 mA	80	45	40	mA
I_{SB}[2]	Standby Current	Vcc = Max, I_{OUT} = 0 mA	5	5	5	mA

Notes:
1. Input signals switch from 0V to 3V with a rise/fall time of less than 3ns, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
2. All input signals are connected to Vcc. All outputs are unloaded. Read and write clocks switch at maximum frequency (f_{MAX}).

TABLE 6. ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to 7.0V
AC Input Voltage (Pulse Width 20 ns)	5.0V
DC Output Current Max. Sink Current/Pin	50 mA
T_{STG} Storage Temperature	–55°C to +125°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

TABLE 7. CAPACITANCE

T_A = 25°C, f = 1.0 MHz

Name	Description[1]	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	—	10	pF
C_{OUT}	Output Capacitance[2]	V_{OUT} = 0V	—	10	pF

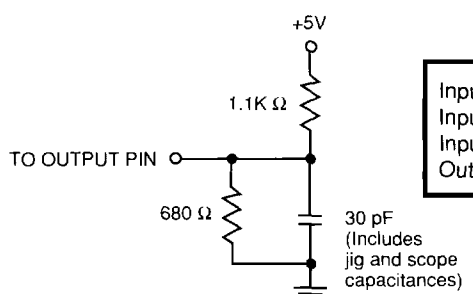
Notes:
1. Capacitance is guaranteed but not tested.
2. *Outputs are deselected,* $\overline{OE}$ *is HIGH.*

TABLE 8. DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA	2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA	—	0.4	V
I_{OZ}	Output Leakage	V_{CC} = Max, V_{IN} = GND to V_{CC} $\overline{OE}$ V_{IH}	–10	+10	µA
I_{IL}	Input Leakage	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	–1	+1	µA

FIGURE 3. AC TEST CONDITIONS



Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

TABLE 9. AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

		Speed (ns) -12		-15		-20		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
fs	Clock Cycle Frequency	—	83	—	66.7	—	50	MHz
tA	Data Access Time	2	9	2	10	2	12	ns
tCLK	Clock Cycle Time	12	—	15	—	20	—	ns
tCLKH	Clock HIGH Time	5	—	6	—	8	—	ns
tCLKL	Clock LOW Time	5	—	6	—	8	—	ns
tDS	Data Setup Time	3	—	4	—	5	—	ns
tDH	Data Hold Time	1	—	1	—	1	—	ns
tENS	Enable Setup Time	3	—	4	—	5	—	ns
tENH	Enable Hold Time	1	—	1	—	1	—	ns
tRS	Reset Pulse Width[1]	12	—	15	—	20	—	ns
tRSS	Reset Setup Time	12	—	15	—	20	—	ns
tRSF	Reset to Flag and Output Valid	—	12	—	15	—	20	ns
tOE	Output Enable to Output Valid	3	7	3	8	3	10	ns
tOLZ	Output Enable to Output LOW[2]	0	—	0	—	0	—	ns
tOHZ	Output Enable to Output HIGH[2]	3	7	3	8	3	10	ns
tWFF	Write Clock to Full Flag	—	9	—	10	—	12	ns
tREF	Read Clock to Empty Flag	—	9	—	10	—	12	ns
tPAF	Write Clock to Programmable Almost-Full Flag	—	9	—	10	—	12	ns
tPAE	Read Clock to Programmable Almost-Empty Flag	—	9	—	10	—	12	ns
tSKEW1	Skew Time between Read Clock and Write Clock for Empty Flag and Full Flag	5	—	6	—	8	—	ns
tSKEW2	Skew Time between Read Clock and Write Clock for Almost-Empty and Almost-Full Flag	22	—	28	—	35	—	ns

Notes: 1. Pulse widths less than minimum values are not allowed.
2. Values are generated by design, not currently tested.

TABLE 9. AC ELECTRICAL CHARACTERISTICS

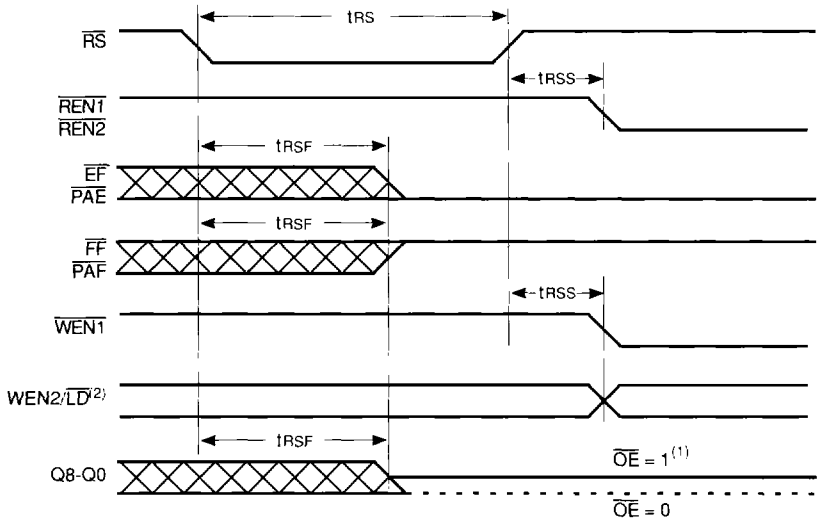
T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

		Speed (ns)						
		-25		-35		-50		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
fS	Clock Cycle Frequency	—	40	—	28.6	—	20	MHz
tA	Data Access Time	2	15	2	20	—	25	ns
tCLK	Clock Cycle Time	25	—	35	—	50	—	ns
tCLKH	Clock HIGH Time	10	—	14	—	20	—	ns
tCLKL	Clock LOW Time	10	—	14	—	20	—	ns
tDS	Data Setup Time	6	—	8	—	10	—	ns
tDH	Data Hold Time	1	—	2	—	2	—	ns
tENS	Enable Setup Time	6	—	8	—	10	—	ns
tENH	Enable Hold Time	1	—	2	—	2	—	ns
tRS	Reset Pulse Width[1]	25	—	35	—	50	—	ns
tRSS	Reset Setup Time	25	—	35	—	50	—	ns
tRSF	Reset to Flag and Output Valid	—	25	—	35	—	50	ns
tOE	Output Enable to Output Valid	3	13	3	15	3	25	ns
tOLZ	Output Enable to Output LOW[2]	0	—	0	—	0	—	ns
tOHZ	Output Enable to Output HIGH[2]	3	13	3	15	3	25	ns
tWFF	Write Clock to Full Flag	—	15	—	20	—	30	ns
tREF	Read Clock to Empty Flag	—	15	—	20	—	30	ns
tPAF	Write Clock to Programmable Almost-Full Flag	—	15	—	20	—	30	ns
tPAE	Read Clock to Programmable Almost-Empty Flag	—	15	—	20	—	30	ns
tSKEW1	Skew Time between Read Clock and Write Clock for Empty Flag and Full Flag	10	—	12	—	15	—	ns
tSKEW2	Skew Time between Read Clock and Write Clock for Almost-Empty and Almost-Full Flag	40	—	42	—	45	—	ns

Notes: 1. Pulse widths less than minimum values are not allowed.
2. Values are generated by design, not currently tested.

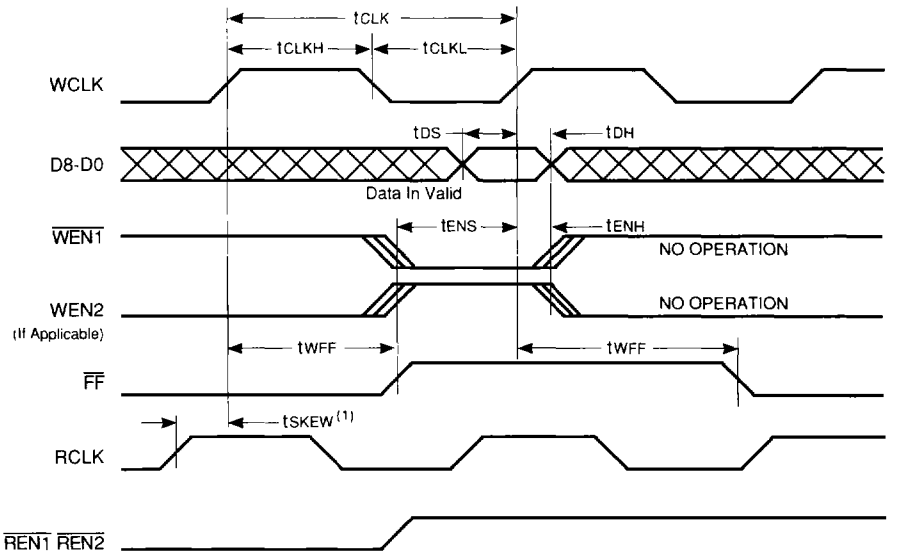
TIMING DIAGRAMS

FIGURE 4. RESET TIMING



Notes:
1. After reset, the outputs will be low if $\overline{OE}$ = 0 and three-state if $\overline{OE}$ = 1.
2. If WEN2/$\overline{LD}$ is LOW during a reset, then it will be configured as a $\overline{LD}$ pin.
   If WEN2/$\overline{LD}$ is HIGH during a reset, then it will be configured as a WEN2 pin.
3. The clock (RCLK, WCLK) can be free-running during reset.

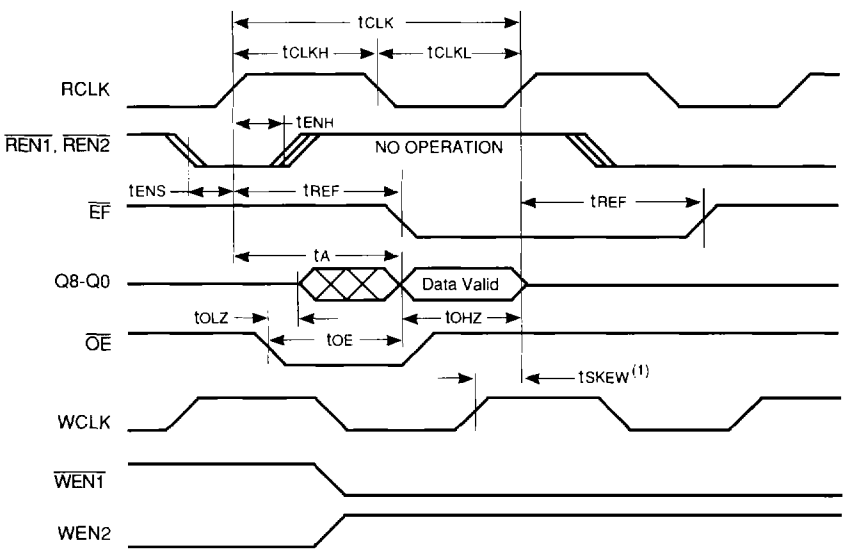
FIGURE 5. WRITE CYCLE TIMING



Notes:

1. t_{SKEW1} is the minimum time between the rising edge of RCLK and the rising edge of WCLK for an $\overline{FF}$ transition to occur in that clock cycle. If the t_{SKEW1} is not satisfied, then an $\overline{FF}$ transition may not occur until the next WCLK edge.

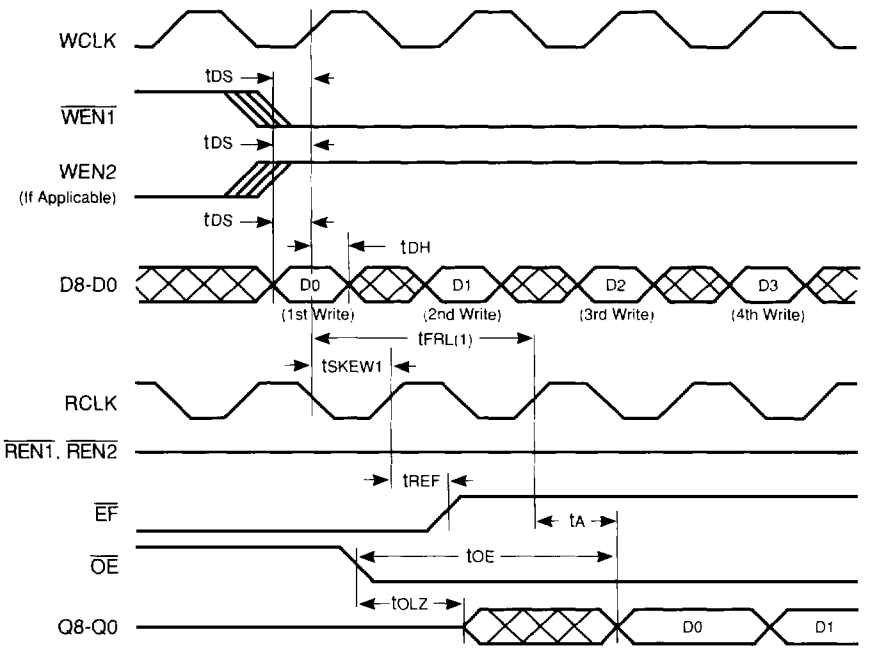
FIGURE 6. READ CYCLE TIMING



Notes:

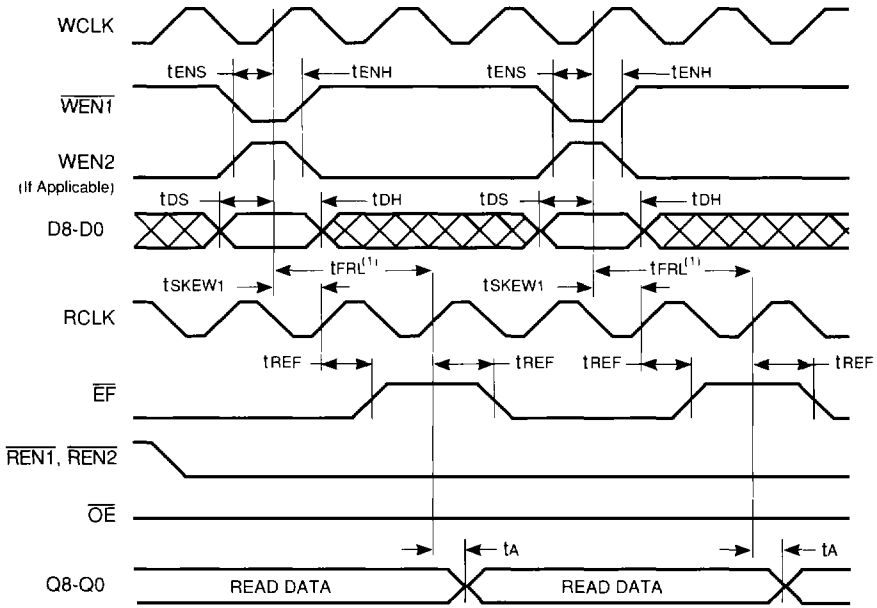
1. t_{SKEW1} is the minimum time between the rising edge of WCLK and the rising edge of RCLK for an $\overline{EF}$ transition to occur in that clock cycle. If the t_{SKEW1} is not satisfied, then an $\overline{EF}$ transition may not occur until the next RCLK edge.

FIGURE 7. FIRST DATA WORD LATENCY TIMING



Notes:
1. The latency timing is only relevant when the Empty flag is LOW.
   When t_{SKEW1} is greater than minimum specifications, $t_{FRL} = t_{CLK} + t_{SKEW1}$.
   When t_{SKEW1} is less than minimum specifications, $t_{FRL} = 2(t_{CLK}) + t_{SKEW1}$.

FIGURE 8. EMPTY FLAG TIMING



Notes:

1. The latency timing is only relevant when the Empty flag is LOW.
   When tSKEW1 is greater than minimum specifications, $t_{FRL} = t_{CLK} + t_{SKEW1}$.
   When t_{SKEW1} is less than minimum specifications, $t_{FRL} = 2(t_{CLK}) + t_{SKEW1}$.

FIGURE 9. FULL FLAG TIMING

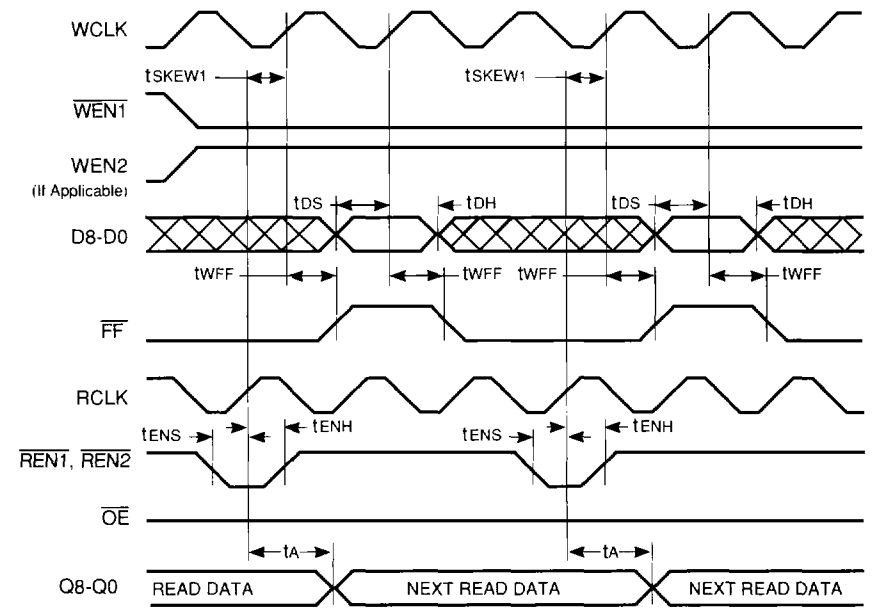
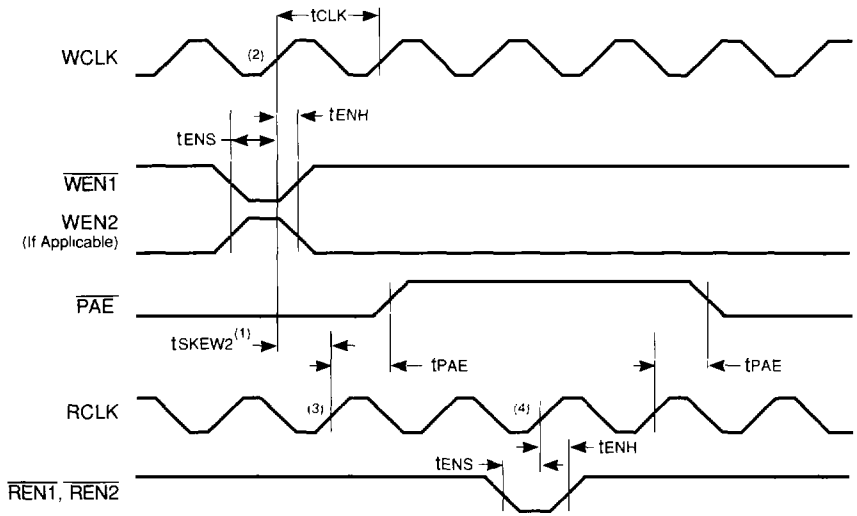


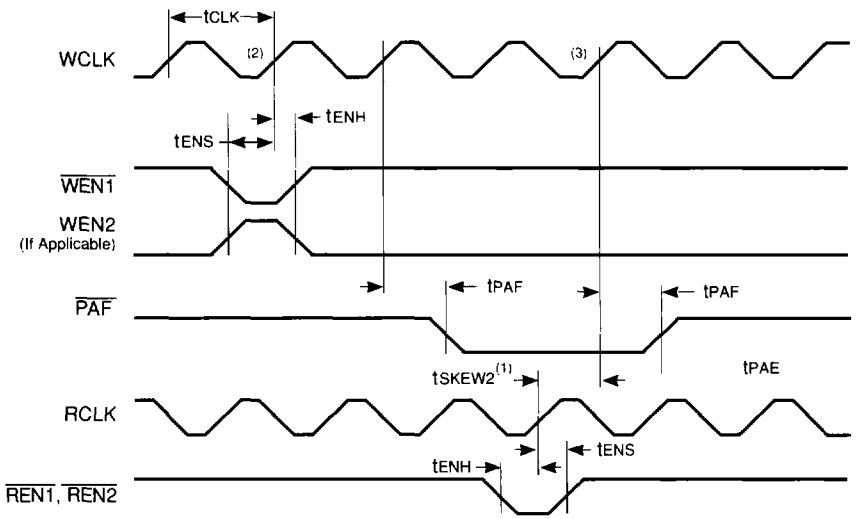
FIGURE 10. PROGRAMMABLE ALMOST-EMPTY FLAG TIMING



Notes:

1. t_{SKEW2} is the minimum time between the rising edge of WCLK and the rising edge of RCLK to guarantee that $\overline{PAE}$ will make a transition to HIGH during that clock cycle. If t_{SKEW2} timing is not met, then $\overline{PAE}$ may not make a transition to HIGH until the next rising edge of RCLK.
2. This write cycle is (N+1) locations ahead of the read pointer. N is the value in the programmable Almost-Empty flag register.
3. $\overline{PAE}$ is synchronized to the rising edge of RCLK.
4. $\overline{PAE}$ is synchronized to the rising edge of RCLK, but the $\overline{PAE}$ transition takes place in the next clock cycle.

FIGURE 11. PROGRAMMABLE ALMOST-FULL FLAG TIMING



Notes:

1 t_{SKEW2} is the minimum time between the rising edge of RCLK and the rising edge of WCLK to guarantee that $\overline{PAE}$ will make a transition to HIGH during that clock cycle. If t_{SKEW2} timing is not met, then $\overline{PAE}$ may not make a transition to HIGH until the next rising edge of WCLK.

2 This write cycle is FULL–N locations ahead of the read pointer. N is the value in the programmable Almost-Full flag register.

3. $\overline{PAF}$ is synchronized to the rising edge of WCLK.

4. $\overline{PAF}$ is synchronized to the rising edge of WCLK, but the $\overline{PAF}$ transition takes place in the next clock cycle.

FIGURE 12. WRITE OFFSET REGISTER TIMING

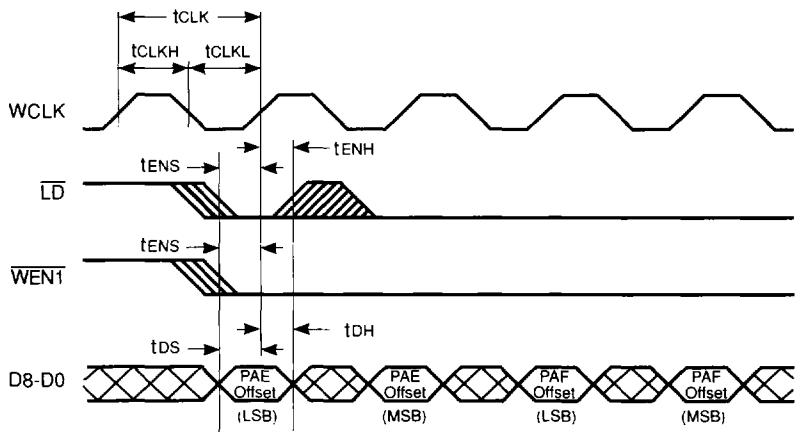
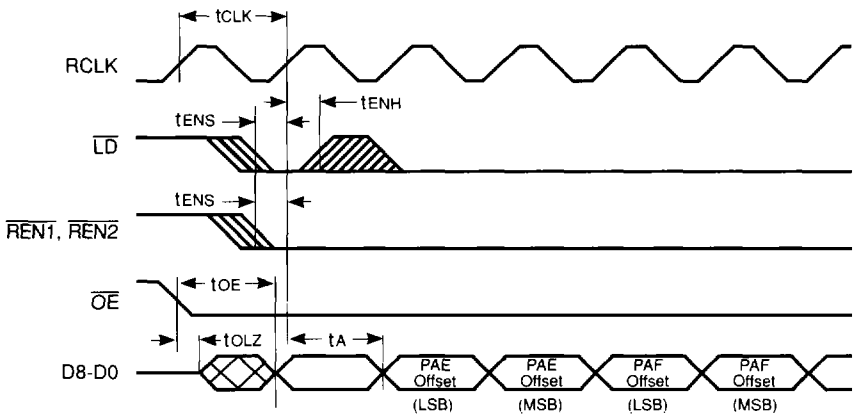


FIGURE 13. READ OFFSET REGISTER TIMING



OPERATING MODES

Single-Device Mode
A single QS72211/221/231/241 may be used when the user requirements are for 512, 1K, 2K or 4K words, respectively. Figure 15 depicts the FIFO in this mode. Read enable 2 ($\overline{REN2}$) is grounded and WEN2/$\overline{LD}$ is LOW during reset, so this signal functions as a register load pin ($\overline{LD}$).

Depth-Expansion Mode
The second write enable (WEN2) is for applications requiring depth expansion. WEN2/$\overline{LD}$ is HIGH during reset, so the signal functions as a WEN2. External logic is then used to direct the flow of data into the cascaded FIFOs.

Width-Expansion Mode
The width of the data word can be increased by connecting corresponding input control signals to multiple FIFOs. Figure 16 shows an 18-bit word width using two QS72V2X1 devices. The word width can be increased by using additional FIFOs. In the example, read enable 2 ($\overline{REN2}$) is grounded and WEN2/$\overline{LD}$ is LOW during reset, so the signal functions as a register load pin ($\overline{LD}$). The status of the flags can be had from any one of the FIFOs.

FIGURE 15. SINGLE-DEVICE MODE

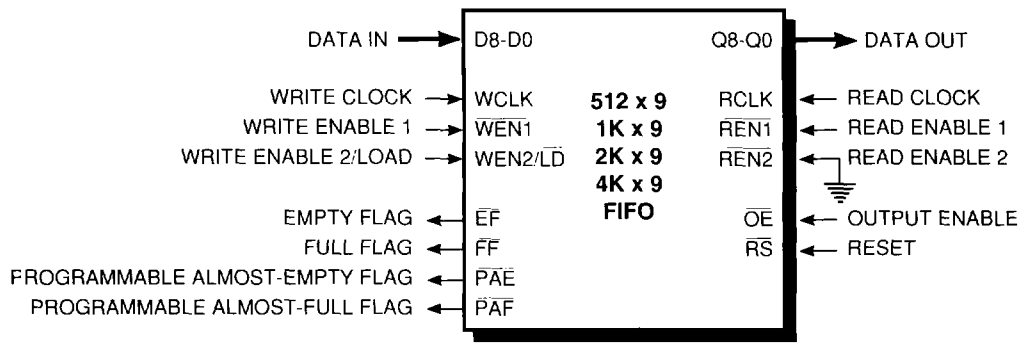
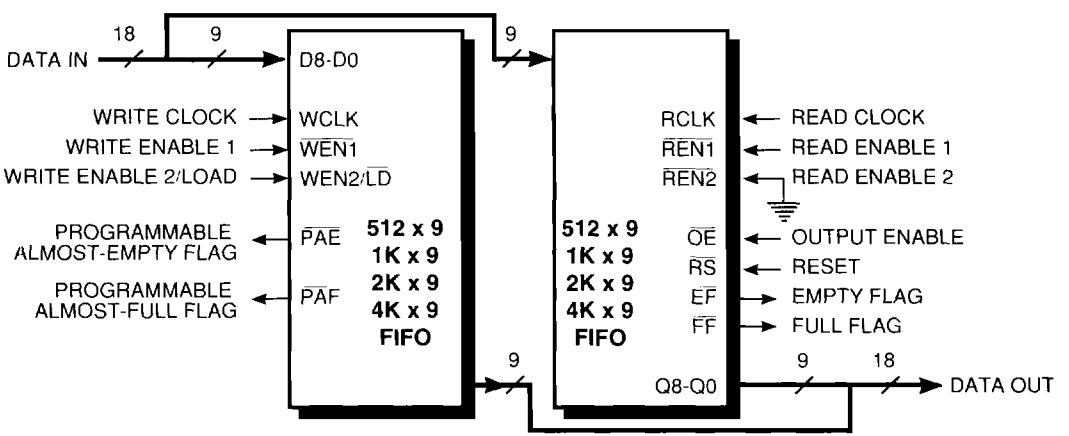


FIGURE 16. WIDTH-EXPANSION MODE



ORDERING INFORMATION

Example: