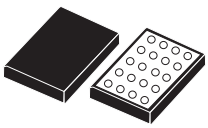
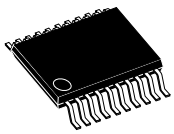
ST2378E

8-bit dual supply 1.71 V to 5.5 V level translator with I/O V_{CC} ±15 kV ESD protection

Datasheet - production data



Flip-Chip20



TSSOP20

Features

- High speed
  - t_{PD} = 15 ns (max.) at T_A = 85 °C
  - V_L = 1.8 V
  - V_{CC} = 5.5 V
- Guaranteed data rate
  - 13 Mbps (1.8 V ≤ V_L ≤ V_{CC} ≤ 5.5 V)
- Low power dissipation
  - I_{TS-VL} = I_{TS-VCC} = 1 µA (max.) at T_A = 85 °C
  - I_{QVL} = 100 µA (max.) at T_A = 85 °C
  - I_{QCC} = 10 µA (max.) at T_A = 85 °C
- Output impedance
  - $|I_{OHA}|$ = 20 µA (min.) at V_L = 1.8 V; V_{CC} = 5.5 V
  - I_{OLA} = 1.0 µA (min.) at V_L = 1.8 V; V_{CC} = 5.5 V
- Bidirectional level translation
- Totem pole and open drain driving for I^2C communications
- 5 V tolerant on enable pin
- Wide operating voltage range
  - V_L (opr.) = 1.71 V to V_{CC}
  - V_{CC} (opr.) = 1.71 V to 5.5 V
- ESD performance
- HBM > 15 kV ESD protection on I/O V_{CC} lines
- Lead-free Flip-Chip and TSSOP package

Description

The ST2378E device is an 8-bit, dual supply, bidirectional level translator with ±15 kV ESD protection on I/Os at V_{CC} side. It is designed to interface data transfer between low voltage ASICs/PLDs and higher voltage systems. Externally applied voltage, V_{CC} and V_L, set logic levels at both sides with the range specified as 1.71 V ≤ V_L ≤ 5.5 V and V_L ≤ V_{CC} ≤ 5.5 V. For proper operation, V_{CC} should be set higher than V_L.

Utilizing a transmission-gate-based design, this device allows bidirectional asynchronous data transfer, which means each channel is allowed to have either V_{CC} to V_L or V_L to V_{CC} data transfer direction independently and no direction pin is required. The ST2378E device operates at a guaranteed data rate of 13 Mbps over the entire specified operating voltage range.

Among the other features, the OE pin allows disable mode operation whereby current consumption is reduced to less than 1 µA.

Table 1. Device summary

Part number	Temp. range (°C)	Package	Marking
ST2378EBJR	-40 to 85	Flip-Chip20	ST2378E
ST2378ETTR	-40 to 85	TSSOP20	ST2378E

Contents

1 Block diagram

Figure 1. Block diagram

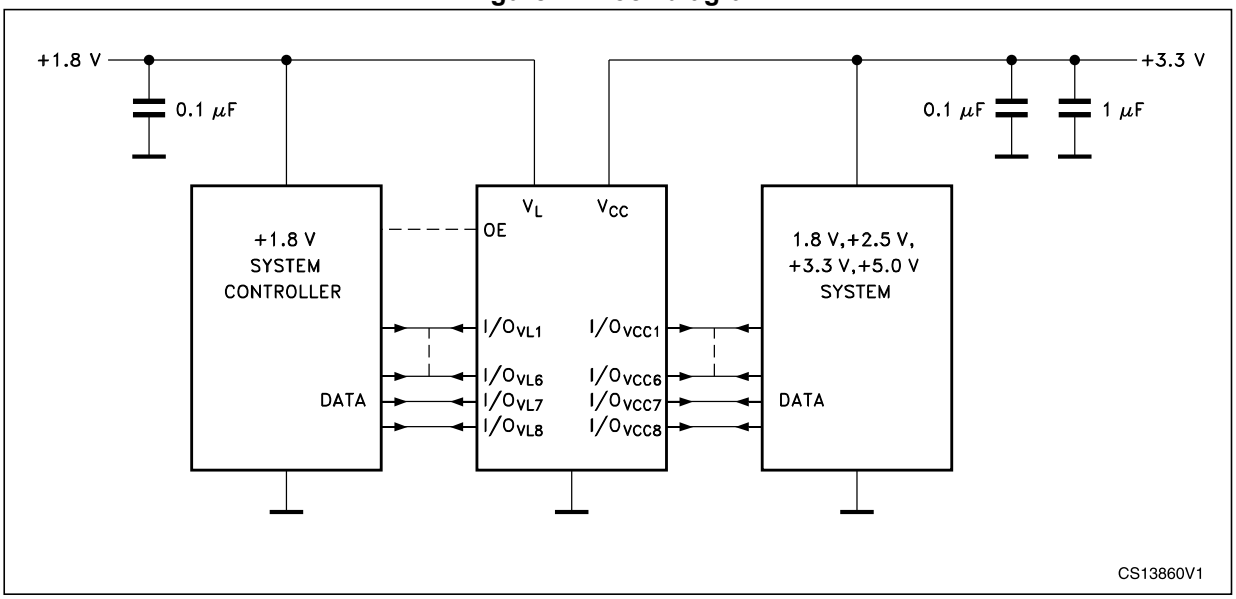
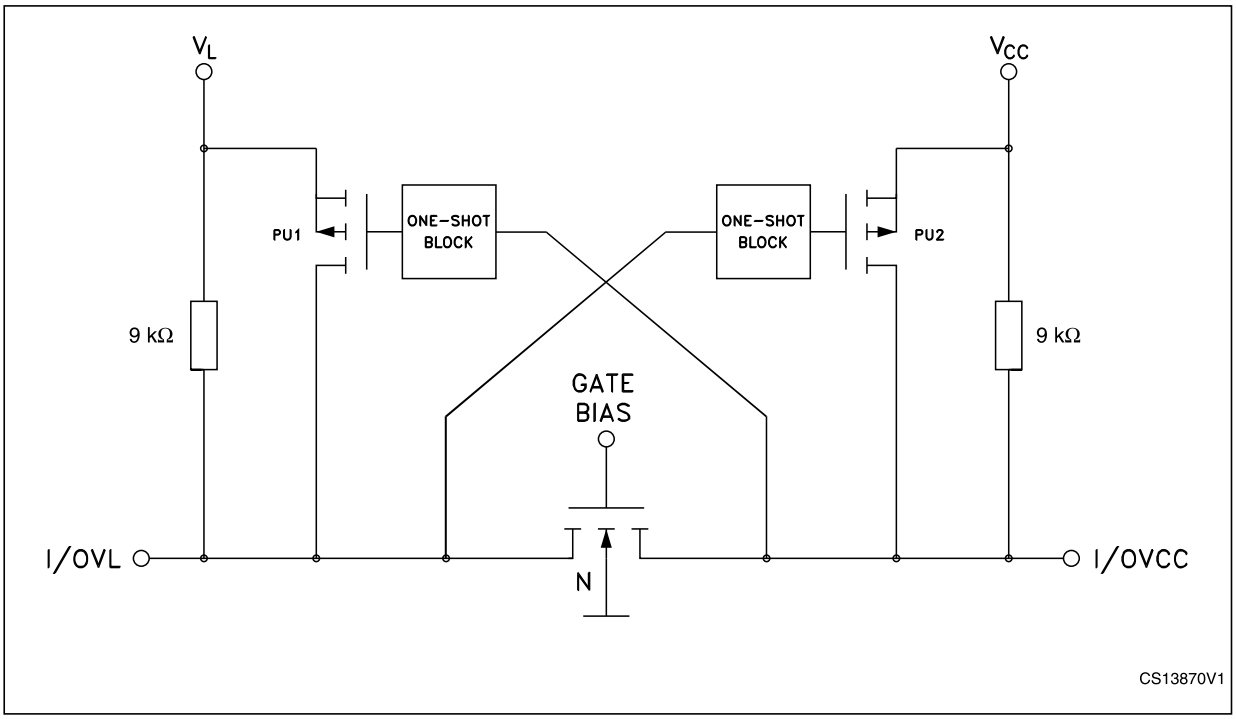


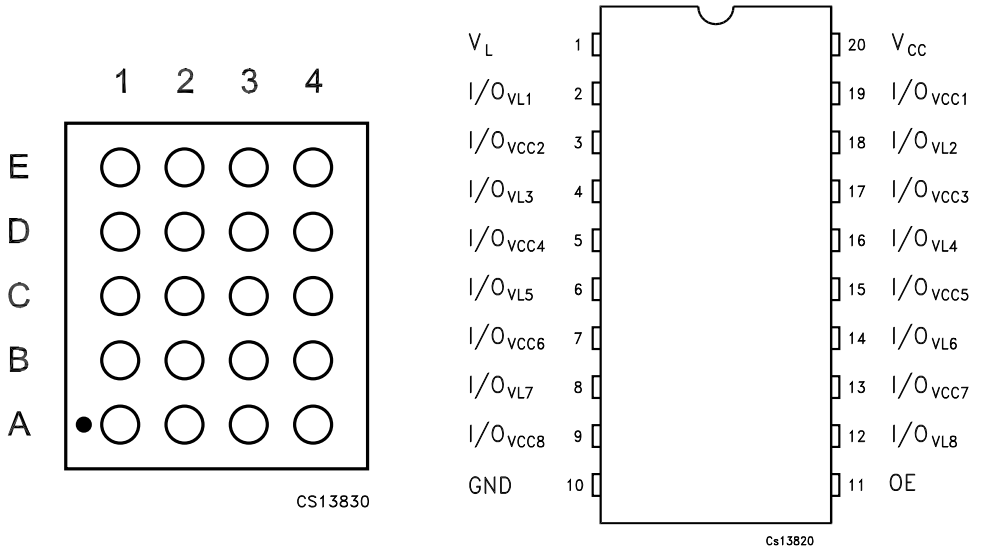
Figure 2. Functional diagram (1 I/O line)



2 Pin settings

2.1 Pin connection

Figure 3. Pin connection



Flip-Chip20
(bottom view) bump side

TSSOP20 (top view)

2.2 Pin description

Table 2. Pin description

Flip-Chip20 pin N°	TSSOP20 pin N°	Symbol	Name and function
E2, D1, D2, C1, C2, B1, B2, A1	2, 18, 4, 16, 6, 14, 8, 12	I/O_{VL1} to I/O_{VL8}	Data inputs/outputs
E3, D4, D3, C4, C3, B4, B3, A4	19, 3, 17, 5, 15, 7, 13, 9	I/O_{VCC1} to I/O_{VCC8}	Data inputs/outputs
A2	11	OE	Output enable inputs
A3	10	GND	Ground (0 V)
E1	1	V_L	Positive supply voltage
E4	20	V_{CC}	Positive supply voltage

3 Electrical data

3.1 Maximum ratings

Table 3. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_L	Supply voltage	-0.3 to V_{CC}	V
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{OE}	DC control input voltage	-0.3 to +7.0	V
$V_{I/OVL}$	DC I/O_{VL} input voltage (OE = GND or V_L)	-0.3 to V_L + 0.3	V
$V_{I/OVCC}$	DC I/O_{VCC} input voltage (OE = GND or V_L)	-0.3 to V_{CC} + 0.3	V
I_{IK}	DC input diode current (OE control pin)	– 20	mA
I_{IOVL}	DC output current	± 25	mA
I_{IOVCC}	DC output current	± 25	mA
I_{SCTOUT}	Short-circuit duration I/O_{VL}, I/O_{VCC} driven from 40 mA source	Continuous	mA
I_{CCB}	DC V_{CC} or ground current	± 100	mA
P_d	Power dissipation(1)	500	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec.)	300	°C

1. 500 mW: ≅ 65 °C derated to 300 mW by 10 mW/°C: 65 °C to 85 °C.

3.2 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_L	Supply voltage		1.71 to V_{CC}	V
V_{CC}	Supply voltage		1.71 to 5.5	V
V_I	Input voltage (OE output enable pin, V_L power supply referred)		0 to 5.5	V
$V_{I/OVL}$	I/O_{VL} voltage		0 to V_L	V
$V_{I/OVCC}$	I/O_{VCC} voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time (OE control pin)(1)		0 to 10	ns/V
dt/dv	Input rise and fall time(2)	$1.71 < V_L < V_{CC} < 5$ V	0 to 10	ns/V
		$V_{CC} = V_L = 5$ V	0 to 3	ns/V

1. V_{OE} from 10% V_L to 90% V_L.
2. V_{IOVL} from 10%V_L to 90%V_L; V_{IOVCC} from 10% V_{CC} to 90% V_{CC}.

4 Electrical characteristics

Table 5. DC specification

Symbol	Parameter	Test condition(1)			Value					Unit
					T_A = 25 °C			-40 to 85 °C		
		V_L (V)(2)	V_{CC} (V)(2)		Min.	Typ.(3)	Max.	Min.	Max.	
V_{IHL}	High level input voltage (I/O_{VL})	1.8	V_L to 5.5		V_L-0.2			V_L-0.2		V
		2.5	V_L to 5.5		0.75 V_L			0.75 V_L		
		3.3	V_L to 5.5		0.75 V_L			0.75 V_L		
		5.0	V_L to 5.5		0.75 V_L			0.75 V_L		
V_{ILL}	Low level input voltage (I/O_{VL})	1.8	V_L to 5.5				0.15		0.15	V
		2.5	V_L to 5.5				0.30		0.30	
		3.3	V_L to 5.5				0.30		0.30	
		5.0	V_L to 5.5				0.30		0.30	
V_{IHC}	High level input voltage (I/O_{VCC})	1.8	V_L to 5.5		V_L-0.2			V_L-0.2		V
		2.5	V_L to 5.5		0.75 V_{CC}			0.75 V_{CC}		
		3.3	V_L to 5.5		0.75 V_{CC}			0.75 V_{CC}		
		5.0	V_L to 5.5		0.75 V_{CC}			0.75 V_{CC}		
V_{ILC}	Low level input voltage (I/O_{VCC})	1.8	V_L to 5.5				0.15		0.15	V
		2.5	V_L to 5.5				0.30		0.30	
		3.3	V_L to 5.5				0.30		0.30	
		5.0	V_L to 5.5				0.30		0.30	
V_{IH-TS}	High level input voltage (OE)	1.8	V_L to 5.5		V_L-0.2			V_L-0.2		V
		2.5	V_L to 5.5		0.75 V_L			0.75 V_L		
		3.3	V_L to 5.5		0.75 V_L			0.75 V_L		
		5.0	V_L to 5.5		0.75 V_L			0.75 V_L		
V_{IL-TS}	Low level input voltage (OE)	1.8	V_L to 5.5				0.15		0.15	V
		2.5	V_L to 5.5				0.25 V_L		0.25 V_L	
		3.3	V_L to 5.5				0.25 V_L		0.25 V_L	
		5.0	V_L to 5.5				0.25 V_L		0.25 V_L	
V_{OHL}	High level output voltage I/O_{VL}	1.8 to 5.5	V_L to 5.5	I_O = -20 µA $I/O_{VCC} \geq V_{CC}$ -0.2	0.67 V_L			0.67 V_L		V
V_{OLL}	Low level output voltage I/O_{VL}			I_O = 1.0 mA $I/O_{VCC} \leq$ 0.15 V			0.40		0.40	

Table 5. DC specification (continued)

Symbol	Parameter	Test condition(1)			Value					Unit
					T_A = 25 °C			-40 to 85 °C		
		V_L (V)(2)	V_{CC} (V)(2)		Min.	Typ.(3)	Max.	Min.	Max.	
V_{OHC}	High level output voltage I/O_{VCC}	1.8 to 5.5	V_L to 5.5	I_O = -20 µA $I/O_{VL} \geq V_L$ -0.2	0.67 V_{CC}			0.67 V_{CC}		V
V_{OLC}	Low level output voltage I/O_{VCC}			I_O = 1.0 mA $I/O_{VL} \leq$ 0.15 V			0.40		0.40	
I_{TSL}	Control input leakage current (OE)	1.8 to 5.5	V_L to 5.5	V_I = GND or 5.5			1		1	µA
I_{TS-LKG}	High impedance input leakage current (IO_{VL}, I/O_{VCC})	1.8 to 5.5	V_L to 5.5	OE = GND			1		1	µA
I_{QVCC}	Quiescent supply current V_{CC}	1.8 to 5.5	V_L to 5.5	I/O_{VL}, I/O_{VCC} unconnected		0.1	1		10	µA
I_{QVL}	Quiescent supply current V_L	1.8 to 5.5	V_L to 5.5	I/O_{VL}, I/O_{VCC} unconnected		13	20		100	µA
I_{TS-VL}	High impedance mode quiescent supply current V_L	1.8 to 5.5	V_L to 5.5	OE = GND I/O_{VL}= GND to V_L I/O_{VCC} = GND to V_{CC}			1		1	µA

1. For normal operation, ensure $V_L < (V_{CC} + 0.3\ V)$. During power-up, $V_L > (V_{CC} + 0.3\ V)$ will not damage the device.
2. Power supply range: V_L, V_{CC} 1.8 V ± 5%, 2.5 ± 0.2 V, 3.3 ± 0.3 V, 5.0 ± 0.5 V.
3. Typical values are referred to T_A = 25 °C.

Table 6. AC electrical characteristics (totem pole driving)

Symbol	Parameter		Test condition[1]		Value			Unit
			C_L= 15 pF, $t_r = t_f \leq$ 6 ns[2] Driver output $R_T \leq$ 50 Ω		-40 to +85 °C			
			V_L (V)[3]	V_{CC} (V)[3]	Min.	Typ.[4]	Max.	
t_{RVCC}	Rise time I/O_{VCC}[5]		1.8	1.8		11	15	ns
			1.8	2.5		11	15	
			1.8	3.3		10	15	
			1.8	5.0		9	15	
			2.5	3.3		8	15	
t_{FVCC}	Fall time I/O_{VCC}[5]		1.8	1.8		6	15	ns
			1.8	2.5		7	15	
			1.8	3.3		8	15	
			1.8	5.0		10	15	
			2.5	3.3		6	15	
t_{RVL}	Rise time I/O_{VL}[5]		1.8	1.8		12	15	ns
			1.8	2.5		10	15	
			1.8	3.3		9	15	
			1.8	5.0		10	15	
			2.5	3.3		7	15	
t_{FVL}	Fall time I/O_{VL}[5]		1.8	1.8		7	15	ns
			1.8	2.5		6	15	
			1.8	3.3		6	15	
			1.8	5.0		7	15	
			2.5	3.3		4	15	
$t_{IOVL-VCC}$	Propagation delay time[6] I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}	1.8	1.8		6	15	ns
			1.8	2.5		7	15	
			1.8	3.3		7	15	
			1.8	5.0		7	15	
			2.5	3.3		4	15	
		t_{PHL}	1.8	1.8		5	15	
			1.8	2.5		5	15	
			1.8	3.3		6	15	
			1.8	5.0		8	15	
			2.5	3.3		4	15	

Table 6. AC electrical characteristics (totem pole driving) (continued)

Symbol	Parameter		Test condition(1)		Value			Unit
			C_L = 15 pF, $t_r = t_f \leq$ 6 ns(2) Driver output $R_T \leq$ 50 Ω		-40 to +85 °C			
			V_L (V)(3)	V_{CC} (V)(3)	Min.	Typ.(4)	Max.	
$t_{IOVCC-VL}$	Propagation delay time(6) I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-HL}	t_{PLH}	1.8	1.8		2	15	ns
			1.8	2.5		2	15	
			1.8	3.3		2	15	
			1.8	5.0		2	15	
			2.5	3.3		2	15	
		t_{PHL}	1.8	1.8		5	15	
			1.8	2.5		5	15	
			1.8	3.3		5	15	
			1.8	5.0		6	15	
			2.5	3.3		4	15	
t_{PZL} t_{PZH} t_{PLZ} t_{PZL}	Output enable and disable time		1.8	1.8		60	80	ns
			1.8	5.0		150	200	
t_{OSLH} t_{OSHL}	Channel to channel skew time(7),(8)		1.8	1.8		0.1	1	ns
			1.8	5.0		0.5	1	
DR	Maximum data rate		1.8 to 5.0	V_L to 5.0	13			Mbps

1. For normal operation, ensure $V_L < (V_{CC} + 0.3\ V)$. During power-up, $V_L > (V_{CC} + 0.3\ V)$ will not damage the device.
2. For $V_{CC} = V_L = 1.8$ V, $t_r = t_f \leq$ 4 ns.
3. Power supply range: V_L, V_{CC} 1.8 V ± 5%, 2.5 ± 0.2 V, 3.3 ± 0.3 V, 5.0 ± 0.5 V.
4. Typical values are referred to T_A = 25 °C.
5. Rise time: 10% to 90%, fall time 90% to 10%.
6. Propagation delay time: 50% to 50%.
7. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |\ t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |\ t_{PHLm} - t_{PHLn}|$.
8. Each translator equally loaded; parameter guaranteed by design.

Table 7. AC characteristic (open drain driving)

Symbol	Parameter		Test condition[1]		Value			Unit
			C_L = 15 pF, $t_r = t_f \leq$ 6 ns[2] Driver output $R_T \leq$ 50 Ω		-40 to +85 °C			
			V_L (V)[3]	V_{CC} (V)[3]	Min.	Typ.[4]	Max.	
t_{RVCC}	Rise time I/O_{VCC}[5]		1.8	1.8		210	300	ns
			1.8	5.0		59	150	
t_{FVCC}	Fall time I/O_{VCC}[5]		1.8	1.8		12	30	ns
			1.8	5.0		20	30	
t_{RVL}	Rise time I/O_{VL}[5]		1.8	1.8		210	300	ns
			1.8	5.0		96	150	
t_{FVL}	Fall time I/O_{VL}[5]		1.8	1.8		11	30	ns
			1.8	5.0		11	30	
$t_{IOVL-VCC}$	Propagation delay time[6] I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}	1.8	1.8		210	300	ns
			1.8	5.0		100	150	
		t_{PHL}	1.8	1.8		7	20	
			1.8	5.0		14	20	
$t_{IOVCC-VL}$	Propagation delay time[6] I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-HL}	t_{PLH}	1.8	1.8		210	300	ns
			1.8	5.0		57	150	
		t_{PHL}	1.8	1.8		7	20	
			1.8	5.0		8	20	
t_{PZL} t_{PZH} t_{PLZ} t_{PZL}	Output enable and disable time		1.8	1.8		60	80	ns
			1.8	5.0		150	200	
t_{OSLH} t_{OSHL}	Channel to channel skew time[7],[8]		1.8	1.8		10	20	ns
			1.8	5.0		2	10	
DR	Maximum data rate		1.8 to 5.0	V_L to 5.0	800			kbps

1. For normal operation, ensure $V_L < (V_{CC} + 0.3\ V)$. During power-up, $V_L > (V_{CC} + 0.3\ V)$ will not damage the device.
2. For $V_{CC} = V_L = 1.8$ V, $t_r = t_f \leq$ 4 ns.
3. Power supply range: V_L, V_{CC} 1.8 V ± 5%, 2.5 ± 0.2 V, 3.3 ± 0.3 V, 5.0 ± 0.5 V.
4. Typical values are referred to T_A = 25 °C.
5. Rise time:10% to 90%, fall time 90% to 10%.
6. Propagation delay time: 50% to 50%.
7. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
8. Each translator equally loaded; parameter guaranteed by design.

5 Test circuit

Figure 4. Test circuit

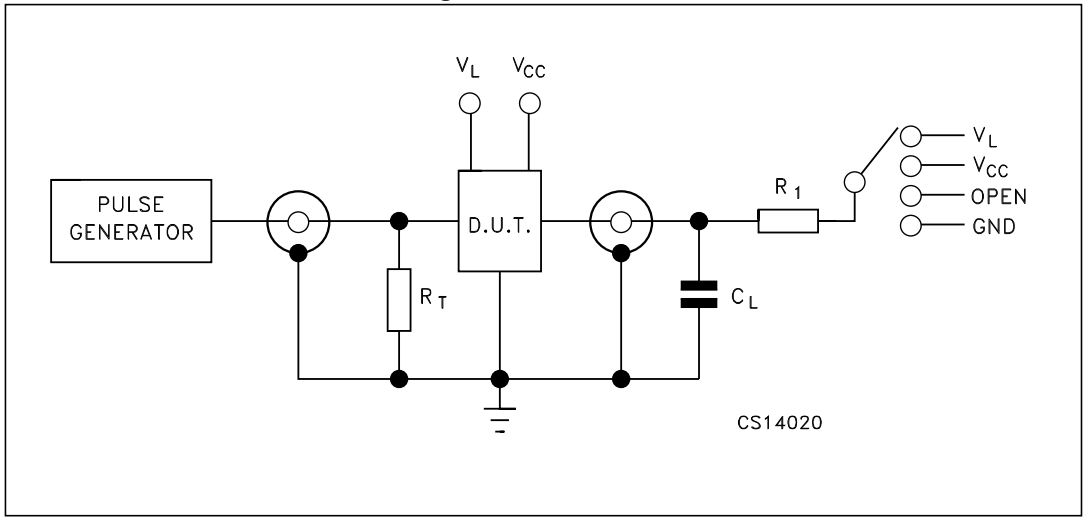


Table 8. Test circuit switches

Test	Switch		
	Driving I/O_{VL}	Driving I/O_{VCC}	Open drain driving
t_{PLH}, t_{PHL}	Open	Open	Open
t_{PZL}, t_{PLZ}	V_{CC}	V_L	-
t_{PZH}, t_{PHZ}	GND	GND	-

Note: C_L = 15/50 pF or equivalent (includes jig and probe capacitance).
R_1 = 1 kΩ or equivalent.
R_T = Z_{OUT} of pulse generator (typically 50 Ω).

Table 9. Truth table

Control pin	Bidirectional input/outputs	
OE	I/O_{VL}	I/O_{VCC}
H(1)	H(1)	H(2)
H(1)	L	L
L	Z	Z

1. High level V_L power supply referred.
2. High level V_{CC} power supply referred.

Note: X = do not care; Z = high impedance.

6 Waveforms

Table 10. Waveform symbol value

Symbol	Driving I/O_{VL}		Driving I/O_{VCC}	
	1.8 V ≤ V_L ≤ V_{CC} ≤ 2.5 V	3.3 V ≤ V_L ≤ V_{CC} ≤ 5.0 V	1.8 V ≤ V_L ≤ V_{CC} ≤ 2.5 V	3.3 V ≤ V_L ≤ V_{CC} ≤ 5.0 V
V_{IH}	V_L	V_L	V_{CC}	V_{CC}
V_{IM}	50% V_L	50% V_L	50% V_{CC}	50% V_{CC}
V_{OM}	50% V_{CC}	50% V_{CC}	50% V_{CC}	50% V_{CC}
V_X	V_{OL} +0.15 V	V_{OL} +0.3 V	V_{OL} +0.15 V	V_{OL} +0.3 V
V_Y	V_{OH} -0.15 V	V_{OH} -0.3 V	V_{OH} -0.15 V	V_{OH} -0.3 V

Figure 5. Waveform - propagation delay (f = 1 MHz; 50% duty cycle)

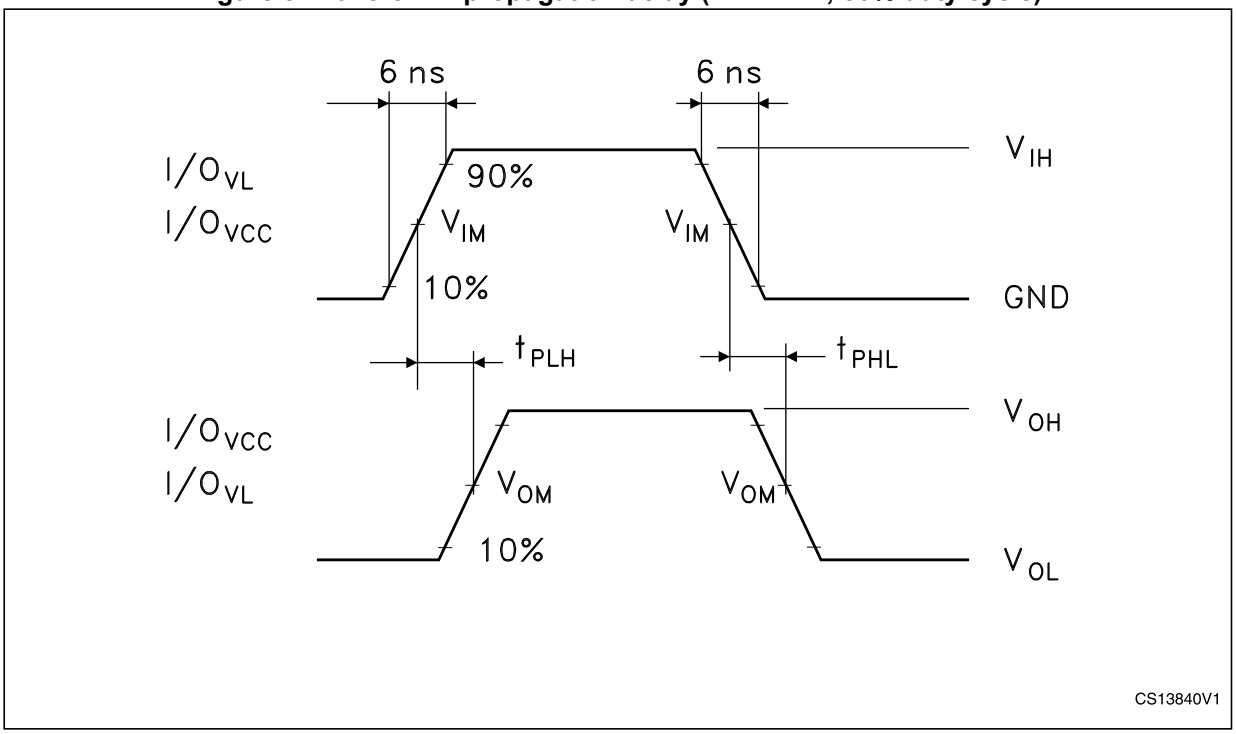
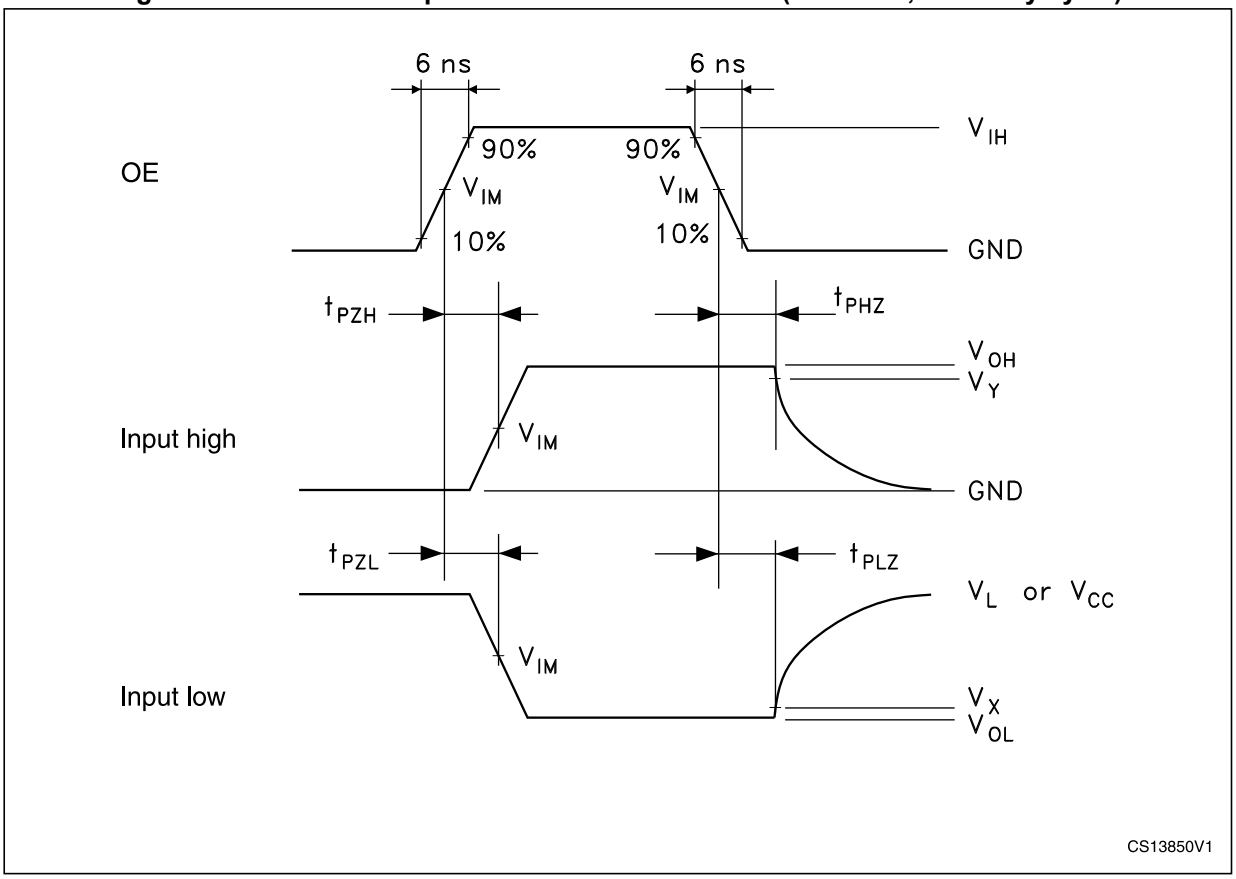


Figure 6. Waveform - output enable and disable time (f = 1 MHz; 50% duty cycle)



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

7.1 TSSOP20 package information

Figure 7. TSSOP20 package outline

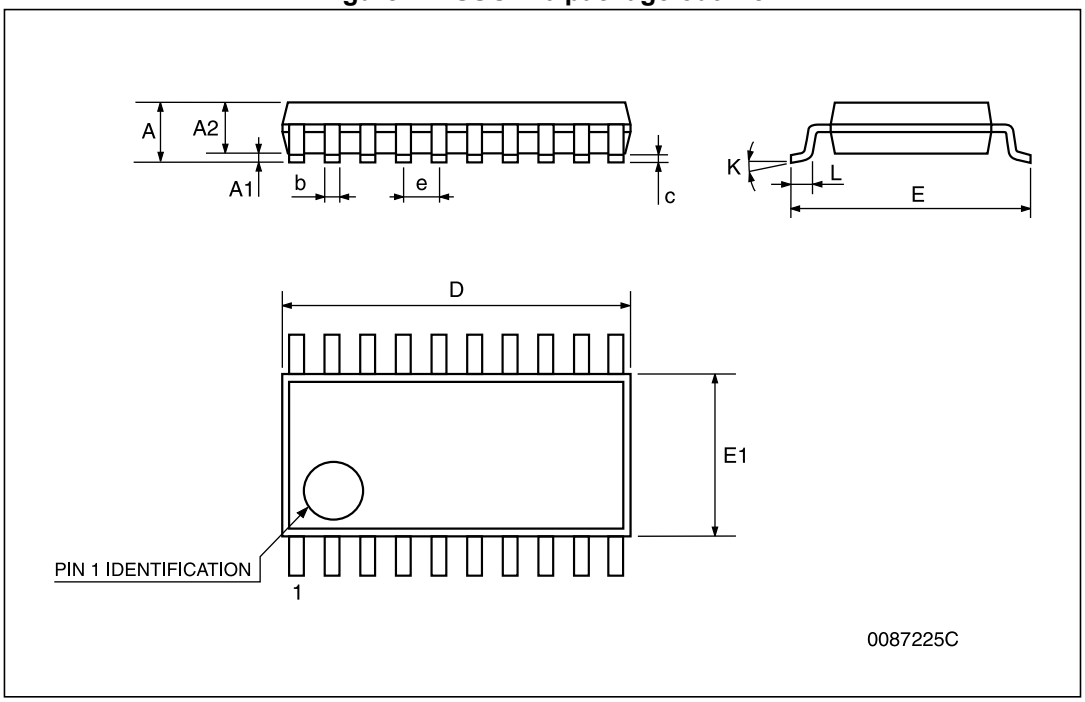
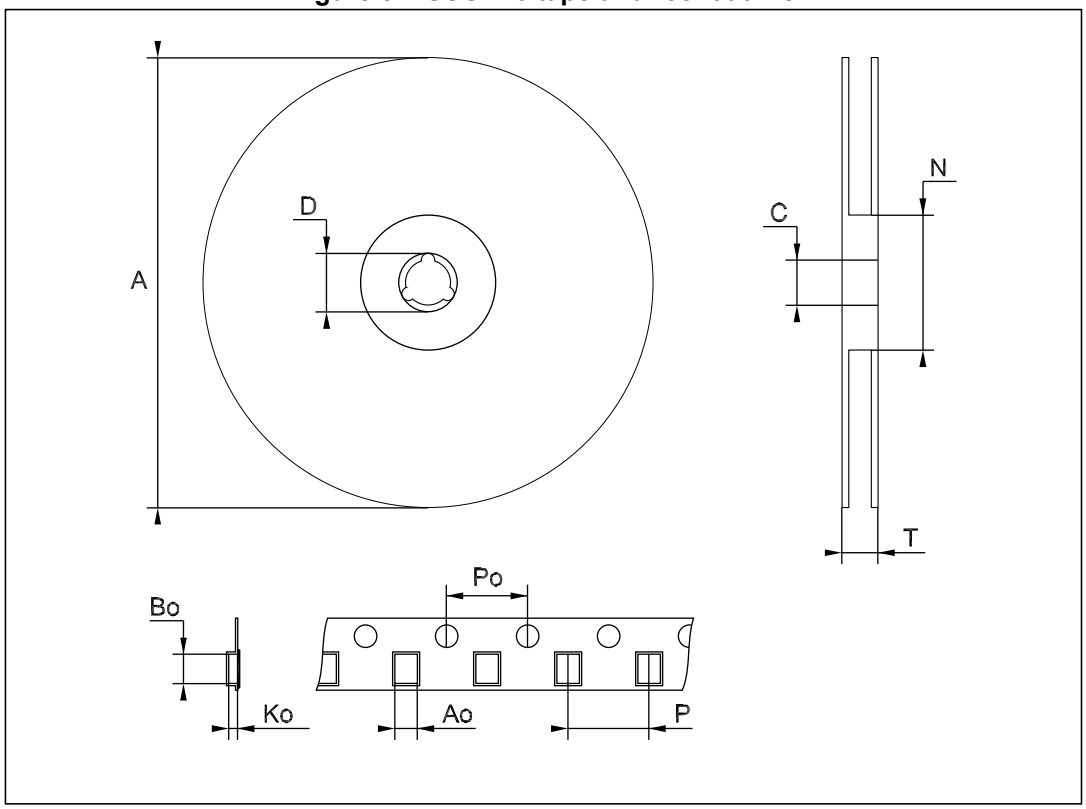


Table 11. TSSOP20 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

7.2 TSSOP20 packing information

Figure 8. TSSOP20 tape and reel outline



1. Drawing not to scale.

Table 12. TSSOP20 tape and reel mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	6.9		7.1	0.272		0.280
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

7.3 Flip-Chip20 package information

Figure 9. Flip-Chip20 package outline

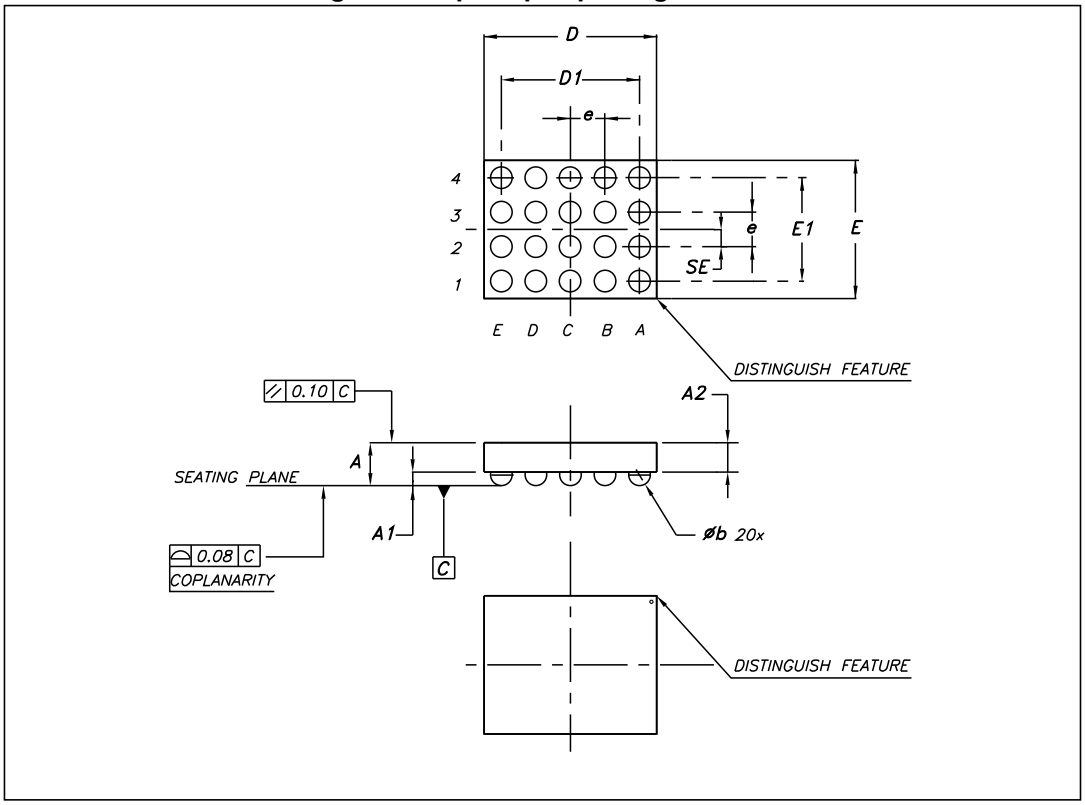
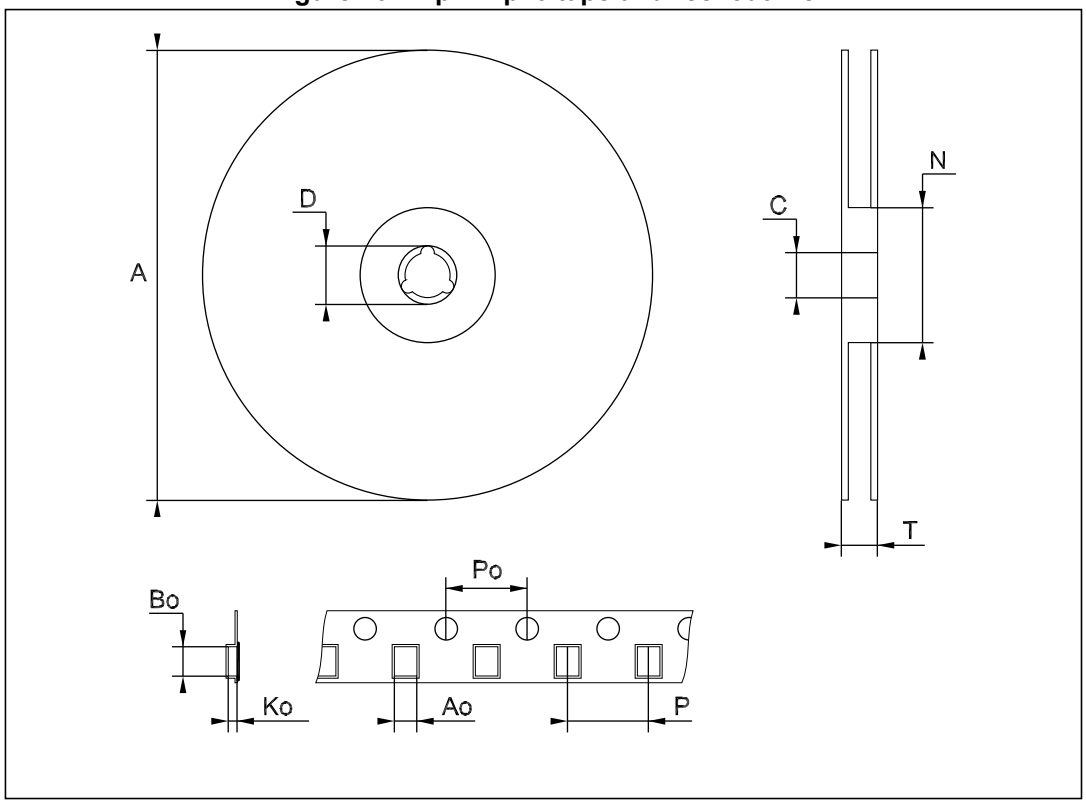


Table 13. Flip-Chip20 package mechanical data

Symbol	Dimensions					
	mm			mils		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.81	0.89	1.00	31.9	35.0	39.4
A1	0.15	0.24	0.35	5.9	9.4	13.8
A2		0.65			25.6	
b	0.25	0.30	0.35	9.8	11.8	13.8
D	2.41	2.46	2.51	94.9	96.9	98.8
D1		2.00			78.7	
E	1.93	1.98	2.03	76.0	78.0	79.9
E1		1.5			59.1	
e		0.50			19.7	
SE		0.25			9.8	

7.4 Flip-Chip20 packing information

Figure 10. Flip-Chip20 tape and reel outline



1. Drawing not to scale.

Table 14. Flip-Chip20 tape and reel mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			180			7.086
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	2.13	2.23	2.33	0.084	0.088	0.092
Bo	2.62	2.72	2.82	0.103	0.107	0.111
Ko	1.05	1.15	1.25	0.041	0.045	0.049
Po	3.9		4.1	0.153		0.161
P	3.9		4.1	0.153		0.161

8 Revision history

Table 15. Document revision history

Date	Revision	Changes
10-Apr-2006	1	Initial release.
18-Sep-2012	2	Updated *Figure 2* (added resistor values). Updated notes and cross-references of the notes below *Table 5* to *Table 7*, replaced t_{FCC} by t_{FVCC} in *Table 6* and *Table 7*. Updated ECOPACK text in *Section 7.*, reformatted *Section 7* (added *Table 11* to *Table 14*, moved note below *Figure 8* and *Figure 10*). Minor corrections throughout document.
18-May-2015	3	Added *Table 1: Device summary*. Revised presentation of *Section 7: Package information*. Minor textual updates.