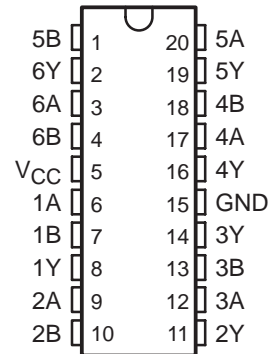


SN74AS1804 HEX 2-INPUT NAND DRIVER

SDAS042C – AUGUST 1984 – REVISED JANUARY 1995

- High Capacitive-Drive Capability
- Typical Delay Time of 2.6 ns ($C_L = 50$ pF) and Typical Power Dissipation of Less Than 9 mW Per Gate
- Center V_{CC} and GND Configuration Provides Minimum Lead Inductance in High-Current Switching Applications
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs

DW OR N PACKAGE
(TOP VIEW)



description

This device contains six independent 2-input NAND drivers. It performs the Boolean functions $Y = A \cdot B$ or $Y = \overline{A + B}$ in positive logic.

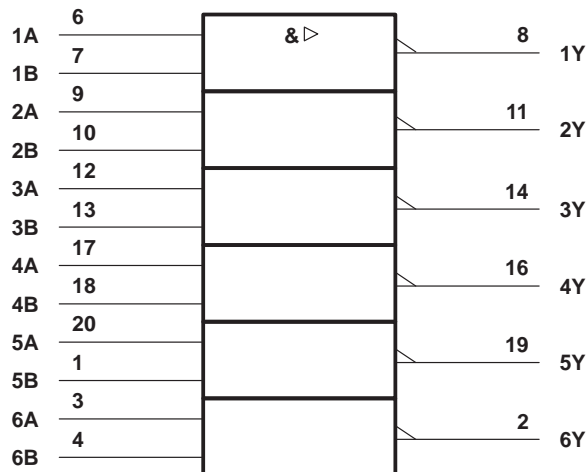
The center-pin configuration reduces lead inductance when compared to the 'AS804B. The reduced lead inductance minimizes noise generated onto either the V_{CC} or GND bus. This reduction is significant in high-current switching applications.

The SN74AS1804 is characterized for operation from 0°C to 70°C.

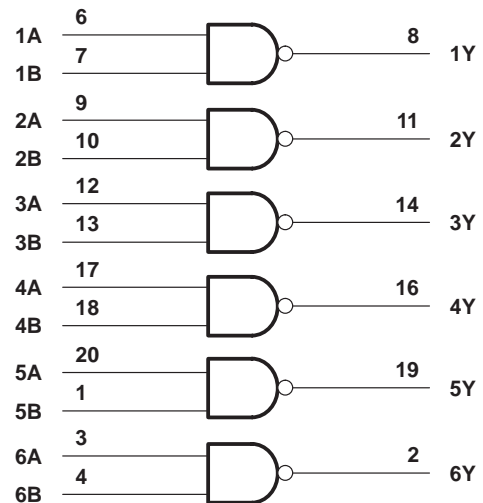
FUNCTION TABLE
(each driver)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74AS1804

HEX 2-INPUT NAND DRIVER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions‡

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{OH} High-level output current			-48	mA
I_{OL} Low-level output current			48	mA
T_A Operating free-air temperature	0		70	°C

‡ This high sink- or source-current device is not recommended for use above 40 MHz.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			-1.2	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -2$ mA	$V_{CC} - 2$			V
	$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA	2.4	3.2	
		$I_{OH} = -48$ mA	2		
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 48$ mA		0.35	0.5	V
I_I	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20	μA
I_{IL}	$V_{CC} = 5.5$ V, $V_I = 0.4$ V			-0.5	mA
I_O^{\parallel}	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	-50		-200	mA
I_{CCH}	$V_{CC} = 5.5$ V, $V_I = 0$		3.5	5	mA
I_{CCL}	$V_{CC} = 5.5$ V, $V_I = 4.5$ V		16	27	mA

§ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

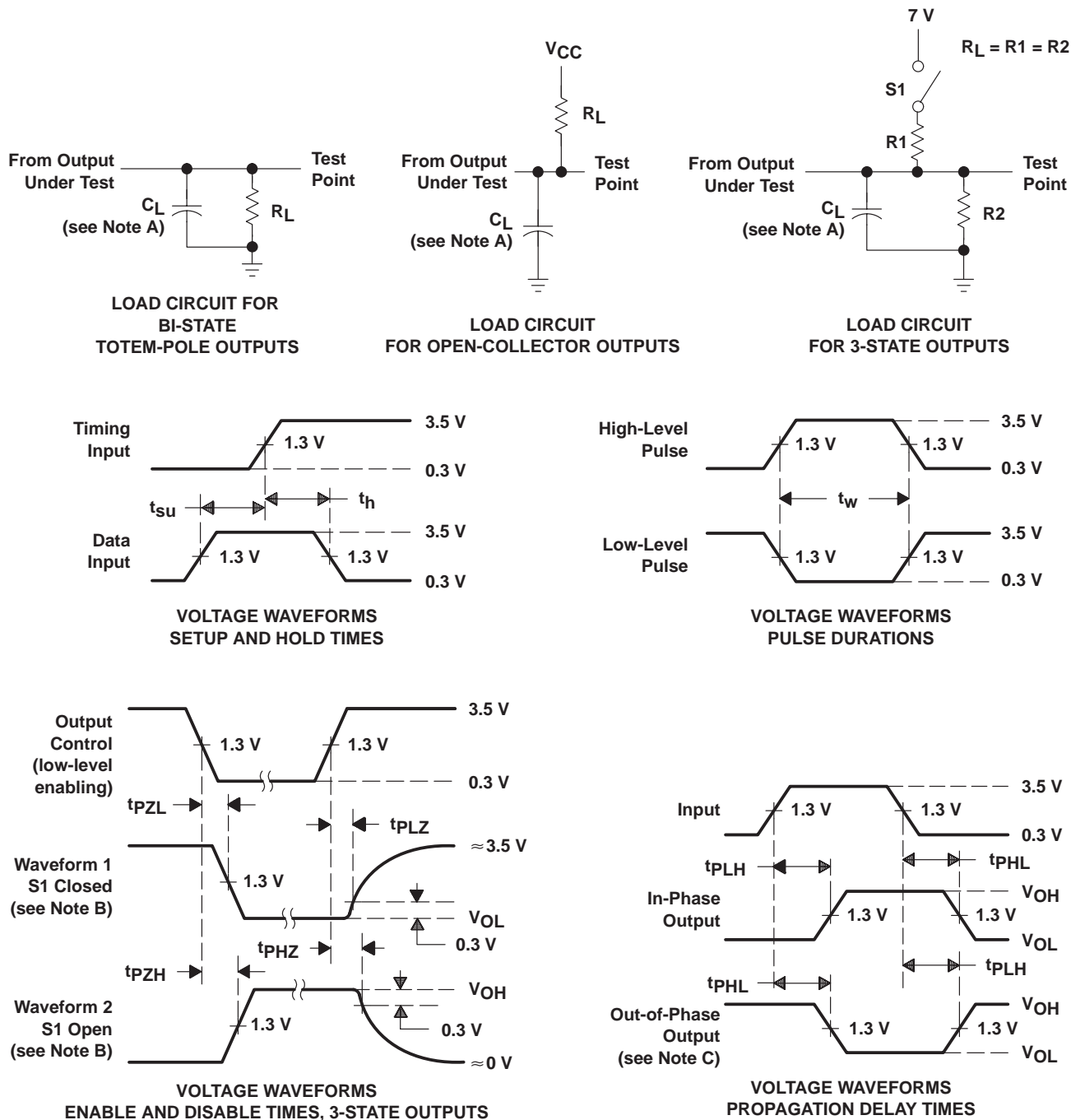
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5$ V to 5.5 V, $C_L = 50$ pF, $R_L = 500 \Omega$, $T_A = \text{MIN to MAX}^\#$		UNIT
			MIN	MAX	
t_{PLH}	A or B	Y	1	4	ns
t_{PHL}			1	4	

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74AS1804N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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