

MC74HC03A

Quad 2-Input NAND Gate with Open-Drain Outputs High-Performance Silicon-Gate CMOS

The MC74HC03A is identical in pinout to the LS03. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

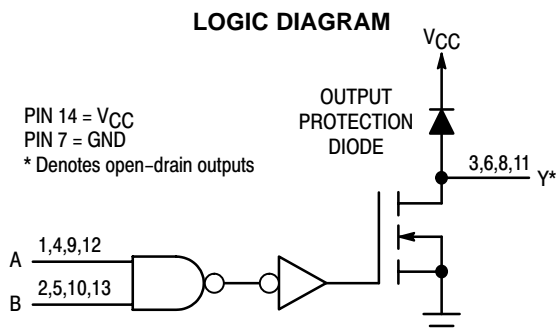
The HC03A NAND gate has, as its outputs, a high-performance MOS N-Channel transistor. This NAND gate can, therefore, with a suitable pullup resistor, be used in wired-AND applications. Having the output characteristic curves given in this data sheet, this device can be used as an LED driver or in any other application that only requires a sinking current.

- Output Drive Capability: 10 LSTTL Loads With Suitable Pullup Resistor
- Outputs Directly Interface to CMOS, NMOS and TTL
- High Noise Immunity Characteristic of CMOS Devices
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1µA
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 28 FETs or 7 Equivalent Gates

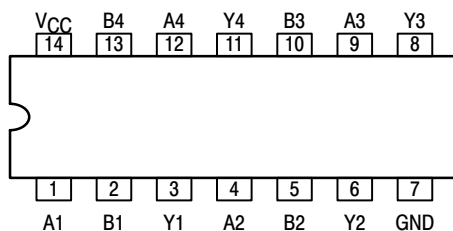
DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	7.0	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	µW
Speed Power Product	0.0075	pJ

* Equivalent to a two-input NAND gate

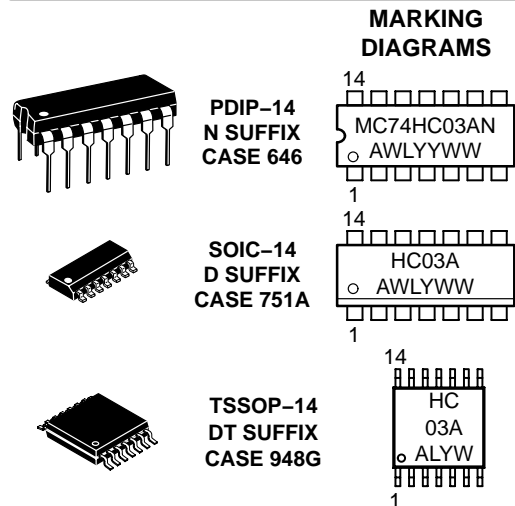


Pinout: 14-Lead Packages (Top View)



ON Semiconductor

<http://onsemi.com>



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

Z = High Impedance

ORDERING INFORMATION

Device	Package	Shipping
MC74HC03AN	PDIP-14	2000 / Box
MC74HC03AD	SOIC-14	55 / Rail
MC74HC03ADR2	SOIC-14	2500 / Reel
MC74HC03ADT	TSSOP-14	96 / Rail
MC74HC03ADTR2	TSSOP-14	2500 / Reel

MC74HC03A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air	Plastic DIP†	750
		SOIC Package†	500
		TSSOP Package†	450
T_{stg}	Storage Temperature	- 65 to + 150	C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: - 10 mW/ C from 65 to 125 C

SOIC Package: - 7 mW/ C from 65 to 125 C

TSSOP Package: - 6.1 mW/ C from 65 to 125 C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	- 55	+ 125	C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0\text{ V}$	0	1000
		$V_{CC} = 4.5\text{ V}$	0	500
		$V_{CC} = 6.0\text{ V}$	0	400

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit	
				-55 to 25°C	≤85°C	≤125°C		
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1\text{V or } V_{CC} - 0.1\text{V}$ $ I_{out} \leq 20\mu\text{A}$	2.0	1.50	1.50	1.50	V	
			3.0	2.10	2.10	2.10		
			4.5	3.15	3.15	3.15		
			6.0	4.20	4.20	4.20		
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1\text{V or } V_{CC} - 0.1\text{V}$ $ I_{out} \leq 20\mu\text{A}$	2.0	0.50	0.50	0.50	V	
			3.0	0.90	0.90	0.90		
			4.5	1.35	1.35	1.35		
			6.0	1.80	1.80	1.80		
V_{OL}	Maximum Low-Level Output Voltage	$V_{out} = 0.1\text{V or } V_{CC} - 0.1\text{V}$ $ I_{out} \leq 20\mu\text{A}$	2.0	0.1	0.1	0.1	V	
			4.5	0.1	0.1	0.1		
			6.0	0.1	0.1	0.1		
		$V_{in} = V_{IH} \text{ or } V_{IL}$	$ I_{out} \leq 2.4\text{mA}$	3.0	0.26	0.33		0.40
			$ I_{out} \leq 4.0\text{mA}$	4.5	0.26	0.33		0.40
			$ I_{out} \leq 5.2\text{mA}$	6.0	0.26	0.33		0.40
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$	6.0	± 0.1	± 1.0	± 1.0	μA	
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0\mu\text{A}$	6.0	1.0	10	40	μA	
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or } GND$	6.0	± 0.5	± 5.0	± 10	μA	

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

MC74HC03A

AC CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			-55 to 25°C	≤85°C	≤125°C	
t _{PLZ} , t _{PZL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	120	150	180	ns
		3.0	45	60	75	
		4.5	24	30	36	
		6.0	20	26	31	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance		10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Buffer)*	Typical @ 25°C, VCC = 5.0 V, VEE = 0 V	pF
		8.0	

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

MC74HC03A

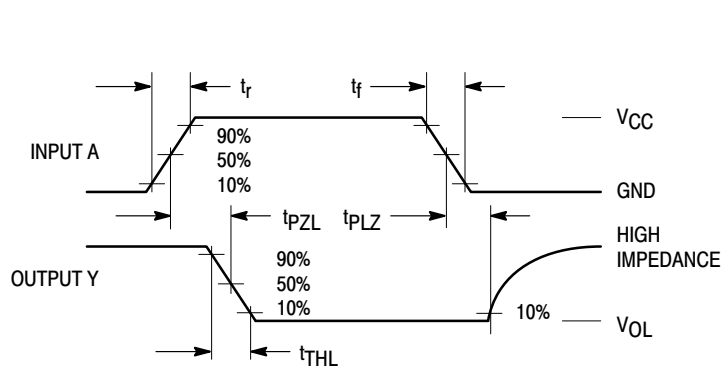


Figure 1. Switching Waveforms

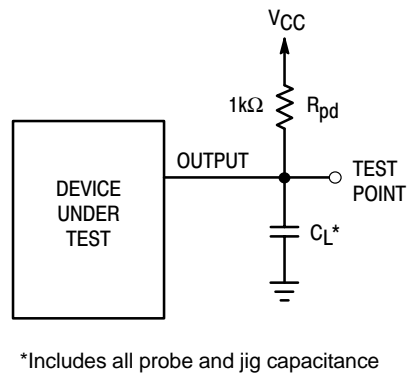
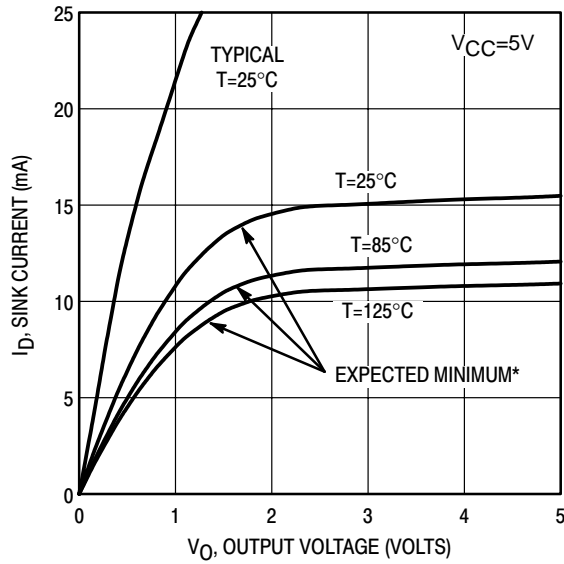
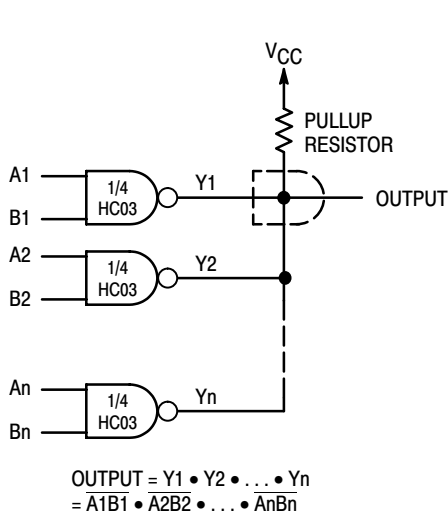


Figure 2. Test Circuit



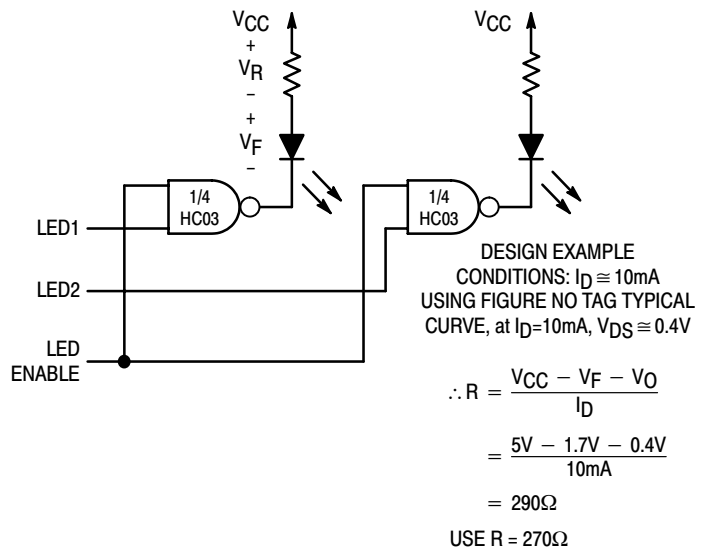
*The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open-Drain Output Characteristics



$$\begin{aligned} \text{OUTPUT} &= Y1 \cdot Y2 \cdot \dots \cdot Yn \\ &= A1B1 \cdot A2B2 \cdot \dots \cdot AnBn \end{aligned}$$

Figure 4. Wired AND



DESIGN EXAMPLE
CONDITIONS: $I_D \approx 10\text{mA}$
USING FIGURE NO TAG TYPICAL
CURVE, at $I_D=10\text{mA}$, $V_{DS} \approx 0.4\text{V}$

$$\begin{aligned} \therefore R &= \frac{V_{CC} - V_F - V_O}{I_D} \\ &= \frac{5\text{V} - 1.7\text{V} - 0.4\text{V}}{10\text{mA}} \\ &= 290\Omega \end{aligned}$$

USE $R = 270\Omega$

Figure 5. LED Driver With Blanking