

# Shock Sensor (Impact Sensor) IC

## BD3852MUZ-Z

### General Description

BD3852MUZ-Z is connected with an external shock sensor. It is equipped with a function to amplify the shock detection signal from the shock sensor and transmit the amplified signal externally. It delivers high S/N characteristics and is ideal for control system applications such as HDD processing.

### Features

- Operating Power Supply Voltage Range: 1.6 V to 2.3 V, Single Power Supply Operation
- Freely Tunable Frequency Characteristics and the Gain according to Applications
- Built-in Notch Filter for Reducing the Effect of the Shock Sensor Resonance Point (fo: 31 kHz)

### Applications

- HDD/light Pick-up Shock Detection and Write Protection
- HDD/light Pick-up Inertial Force Fluctuation Feed Forward Control

### Key Specifications

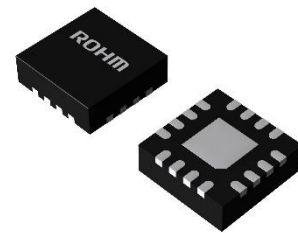
- Recommended Operating Power Supply Voltage Range: 1.6 V to 2.3 V
- Notch Frequency: 31 kHz (Typ)
- Notch Attenuation Rate: -23 dB (Max)
- Current Consumption: 3.9 mA (Typ)
- Recommended Operating Temperature Range: -40 °C to +85 °C

### Package

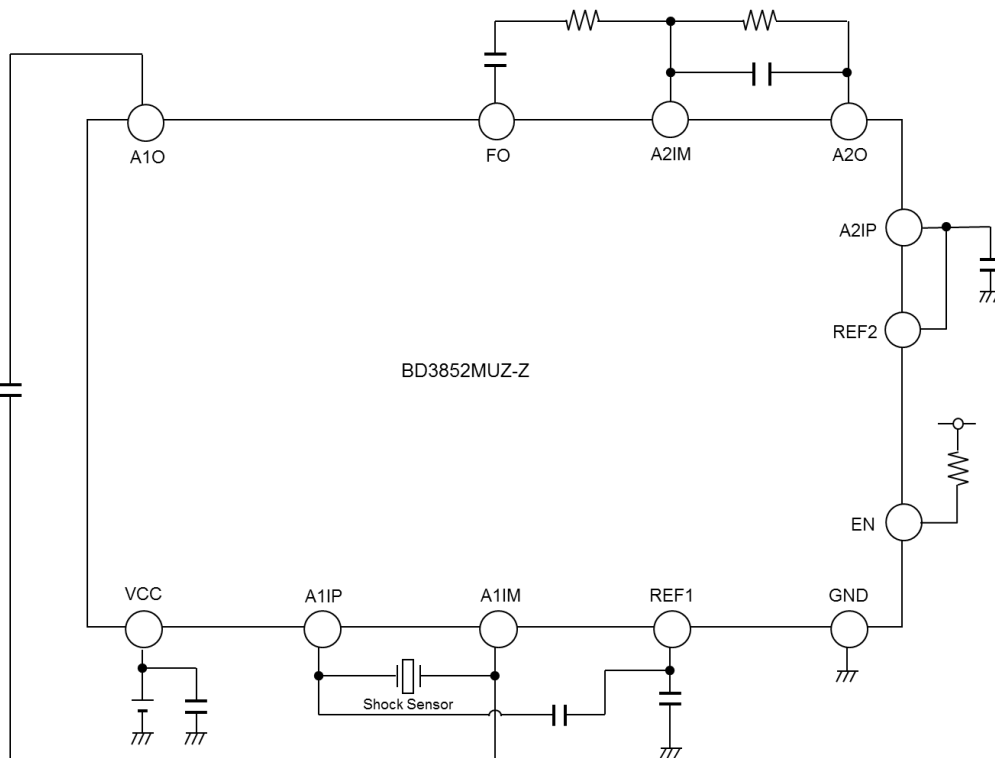
VQFN16Z3030A

### W (Typ) x D (Typ) x H (Max)

3.0 mm x 3.0 mm x 0.4 mm

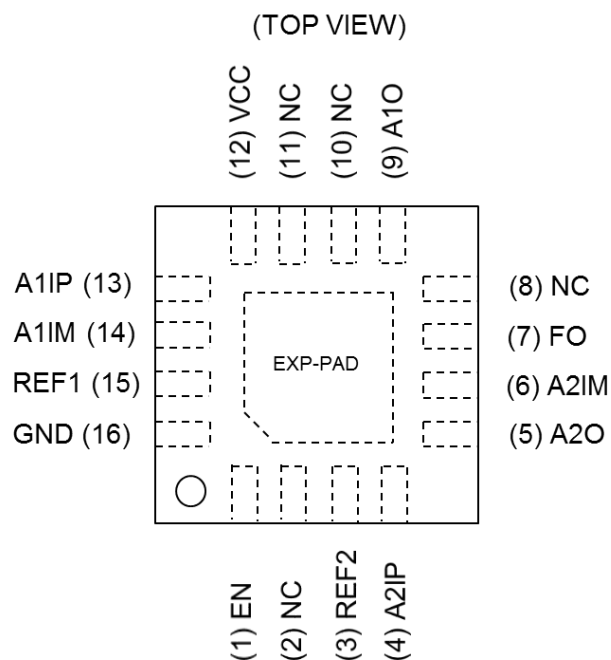


### Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

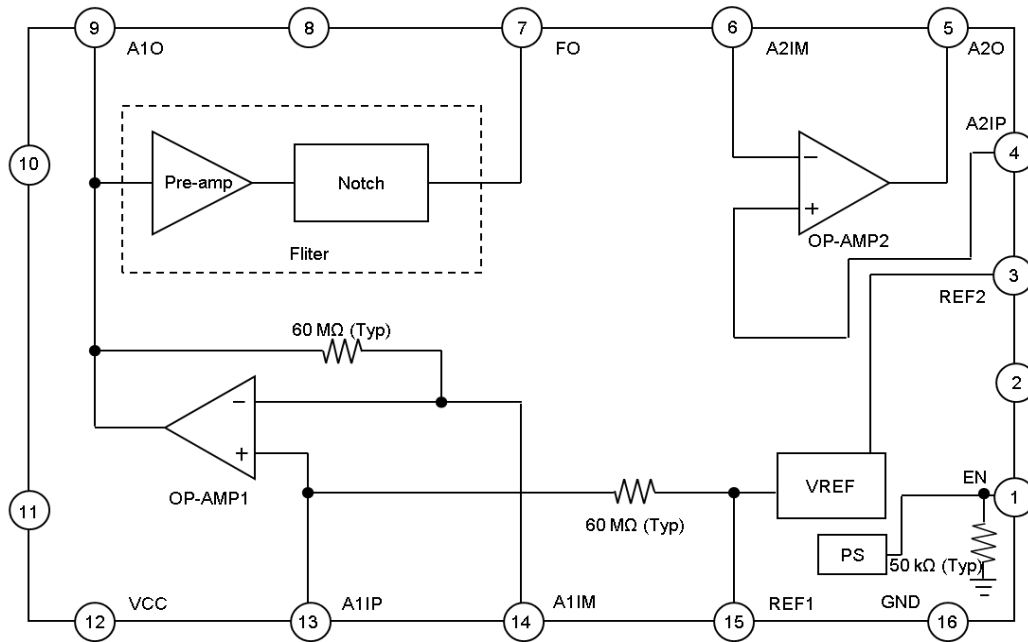
## Pin Configuration



## Pin Description

Pin No.	Pin Name	Function
1	EN	Enable input pin (H input: Power ON, L input: Power saving) Pull-down at 50 kΩ inside the IC
2	NC	Connect to the GND pin
3	REF2	Reference output pin (0.8 V)
4	A2IP	OP-AMP2 non-inverting input pin
5	A2O	OP-AMP2 output pin
6	A2IM	OP-AMP2 inverting input pin
7	FO	Filter output pin
8	NC	Connect to the GND pin
9	A1O	OP-AMP1 output pin
10	NC	Connect to the GND pin
11	NC	Connect to the GND pin
12	VCC	Power supply voltage pin
13	A1IP	OP-AMP1 non-inverting input pin
14	A1IM	OP-AMP1 inverting input pin
15	REF1	Reference output pin (0.4 V)
16	GND	Ground pin
-	EXP-PAD	The EXP-PAD connect to the GND pin

## Block Diagram



## Description of Blocks

OP-AMP1: Detects the charge signal generated in the shock sensor by the charge amplifier configuration.

Filter: Amplifies by 13.9 dB with the preamplifier, and attenuates the  $f_0$  component of the shock sensor resonance frequency (Typ: 31 kHz) with the notch filter.

OP-AMP2: Serves as the amplifier for the signal amplification and the filter. (The gain is configurable using add-on R and C.)

VREF: Generates the REF1 and REF2 output voltages.

PS: Switches between the power saving and power ON states according to the EN pin input voltage.

## Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	$V_{CC}$	4.5	V
Input Voltage	$V_{A1IM}, V_{A1IP}, V_{A2IM}, V_{A2IP}, V_{EN}$	-0.3 to $V_{CC} + 0.3$	V
Output Voltage	$V_{A1O}, V_{A2O}, V_{FO}, V_{REF1}, V_{REF2}$	-0.3 to $V_{CC} + 0.3$	V
Maximum Junction Temperature	$T_{jmax}$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C

**Caution 1:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Caution 2:** Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

## Power Dissipation

Parameter	Symbol	Rating	Unit
Power Dissipation <sup>(Note 1)</sup>	$P_d$	3.00	W

(Note 1) When a 114.3 mm x 76.2 mm x 1.6 mm glass epoxy substrate (JEDEC substrate) is mounted. Reduced at 24.9 mW/°C in  $T_a > 25$  °C.

## Recommended Operating Conditions

Parameter	Symbol	Operating Range			Unit
		Min	Typ	Max	
Power Supply Voltage	$V_{CC}$	1.6	1.8	2.3	V
Operating Temperature	$T_{opr}$	-40	+25	+85	°C

(Note 2) A short circuit between the adjacent pins, reverse connection, rotated connection, short circuit with the power supply, ground fault, and so on may destroy the IC. Since an overload voltage or overload current may be applied to peripheral components, pay sufficient attention during the design and installation.

Electrical Characteristics ( $V_{CC} = 1.8\text{ V}$ ,  $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified.)

Parameter	Symbol	Standard Values			Unit	Conditions
		Min	Typ	Max		
Current Consumption	$I_{CC}$	1.6	3.9	4.5	mA	H input to the EN pin
	$I_{CCPS}$	-	-	10	$\mu\text{A}$	L input to the EN pin

## 1. EN Pin

Parameter	Symbol	Standard Values			Unit	Conditions
		Min	Typ	Max		
Input Voltage	$V_{IH1}$	$V_{CC} \times 0.7$	-	$V_{CC} + 0.3$	V	
	$V_{IL1}$	-0.3	-	$V_{CC} \times 0.3$	V	
Built-in Pull-down Resistance	$R_{UD}$	35	50	65	$\text{k}\Omega$	

## 2. OP-AMP Characteristics

## (1) OP-AMP1

Parameter	Symbol	Standard Values			Unit	Conditions
		Min	Typ	Max		
Output DC Voltage	$V_{DC1}$	0.3	0.4	0.5	V	With no signal
Output Load Fluctuations (Source)	$V_{SOURCE1}$	-100	-	-	mV	Difference between the output DC voltage with no load and the output DC voltage when $80\text{ }\mu\text{A}$ is subtracted
Output Load Fluctuations (Sink)	$V_{SINK1}$	-	-	+100	mV	Difference between the output DC voltage with no load and the output DC voltage when $80\text{ }\mu\text{A}$ is added

## (2) OP-AMP2

Parameter	Symbol	Standard Values			Unit	Conditions
		Min	Typ	Max		
Input Current	$I_{IN}$	-50	-	+50	nA	
Output DC Voltage 1	$V_{DC21}$	0.67	0.80	0.93	V	When the A2IP and REF2 pins are connected
Output DC Voltage 2	$V_{DC22}$	0.75	0.80	0.85	V	When 0.8 V is input to the A2IP pin
Output Voltage Range (L side)	$V_{OL2}$	-	-	0.3	V	
Output Voltage Range (H side)	$V_{OH2}$	$V_{CC} - 0.3$	-	-	V	
Output Source Current	$I_{ASO2}$	80	-	-	$\mu\text{A}$	Current flowing into the A2O pin when $V_{CC} - 0.3\text{ V}$ is applied to the A2O pin
Output Sink Current	$I_{ASI2}$	80	-	-	$\mu\text{A}$	Current flowing out of the A2O pin when 0.3 V is applied to the A2O pin

## 2. OP-AMP Characteristics – continued

## (3) Filter

Parameter	Symbol	Standard Values			Unit	Conditions
		Min	Typ	Max		
Output DC Voltage	$V_{DC3}$	200	400	600	mV	
Output Load Fluctuations (Source)	$V_{SOURCE3}$	-100	-	-	mV	Difference between the output DC voltage with no load and the output DC voltage when 80 $\mu$ A is subtracted
Output Load Fluctuations (Sink)	$V_{SINK3}$	-	-	+100	mV	Difference between the output DC voltage with no load and the output DC voltage when 80 $\mu$ A is added
Voltage Gain	$G_V$	-	13.9	-	dB	
Notch Attenuation Rate	ATT	-	-	-23	dB	Attenuation rate at $f_o = 31$ kHz when the signal amplitude of the A1O pin is 5 mVpp

## (4) VREF

Parameter	Symbol	Standard Values			Unit	Conditions
		Min	Typ	Max		
REF1 Output Voltage	$V_{REF1}$	0.35	0.40	0.45	V	With no load
REF2 Output Voltage	$V_{REF2}$	0.68	0.80	0.92	V	With no load
REF2 Output Load Fluctuations (Source)	$V_{REF2SO}$	-100	-	-	mV	Difference in the output DC voltages with no load and when 80 $\mu$ A is subtracted
REF2 Output Load Fluctuations (Sink)	$V_{REF2SI}$	-	-	+100	mV	Difference in the output DC voltages with no load and when 80 $\mu$ A is added

## Reference Data (Note 3)

(Note 3) No shipping test is performed for the reference data.

## 1. OP-AMP1

Parameter	Symbol	Standard Values			Unit	Conditions
		Min	Typ	Max		
Input Bias Voltage	$V_{IN}$	-	0.4	-	V	With no signal
Input Impedance	$Z_{IN}$	-	60	-	M $\Omega$	
GBW (Cut-off Frequency)	$f_{T1}$	-	1.5	-	MHz	

## 2. OP-AMP2

Parameter	Symbol	Standard Values			Unit	Conditions
		Min	Typ	Max		
GBW (Cut-off Frequency)	$f_{T2}$	-	1.5	-	MHz	

## 3. Filter

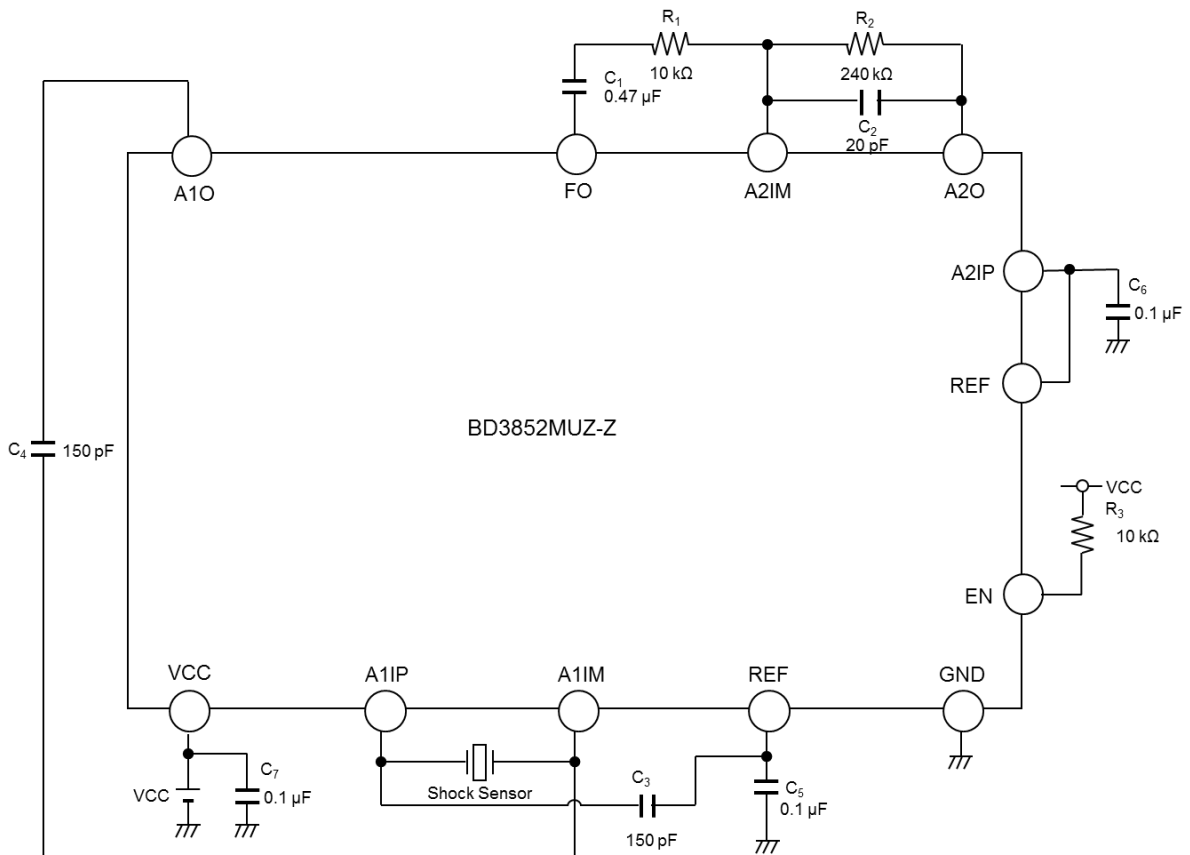
Parameter	Symbol	Standard Values			Unit	Conditions
		Min	Typ	Max		
Notch Frequency	$f_o$	-	31	-	kHz	When the signal amplitude of the A1O pin is 5 mVpp

Reference Data – continued

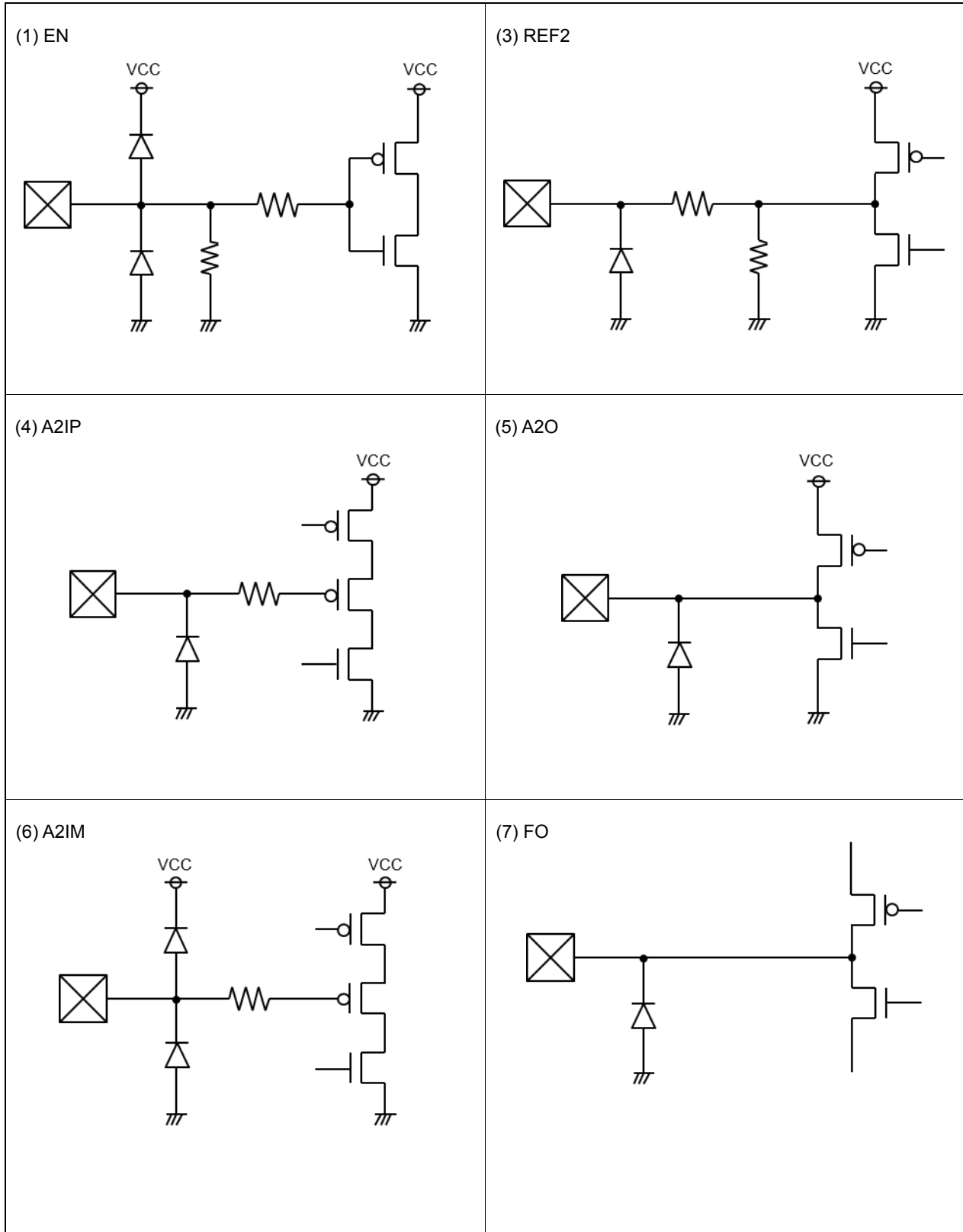
4. Specifications of the EN Pin at Startup and during Power Saving

Parameter	Symbol	Standard Values			Unit	Conditions
		Min	Typ	Max		
Shutdown Time	$t_{SD}$	-	6	10	$\mu s$	Time elapsed after the EN pin input is changed from H to L until the REF2 output voltage is decreased to 10 % of $V_{REF2}$ or less
Startup Time	$t_{SU}$	-	10	50	ms	Time elapsed after the EN pin input is changed from H to L until the REF2 output voltage is increased to 90 % of $V_{REF2}$ or more

Application Example

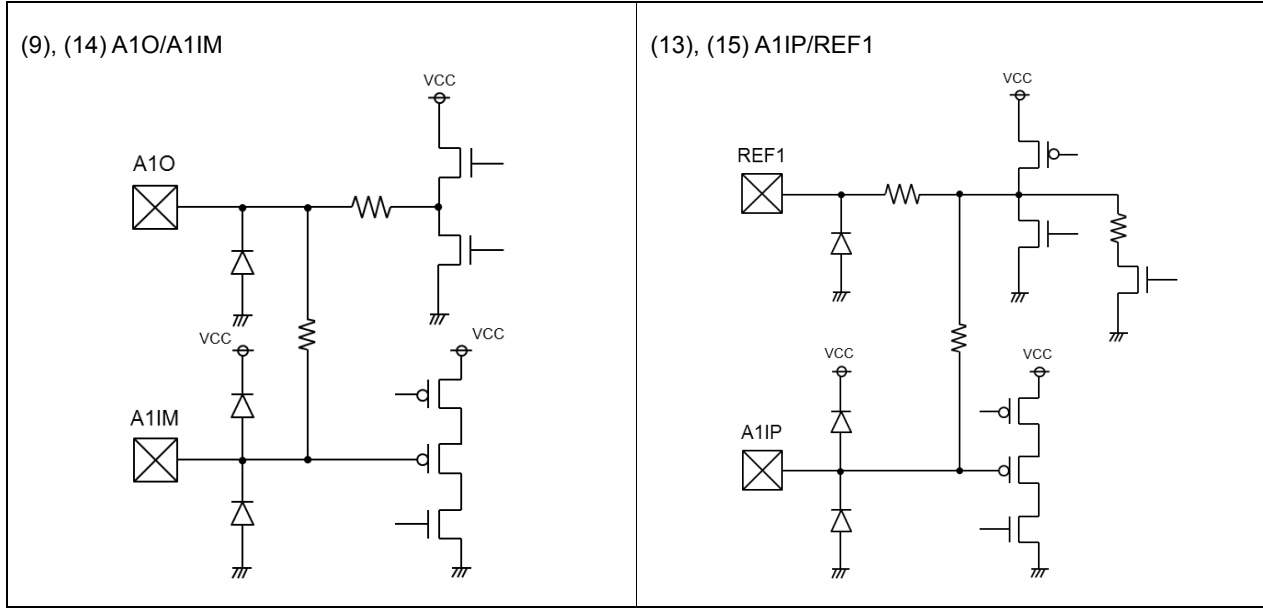


I/O Equivalence Circuits





I/O Equivalence Circuits – continued



## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

### 6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

## Operational Notes – continued

**8. Inter-pin Short and Mounting Errors**

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

**9. Unused Input Pins**

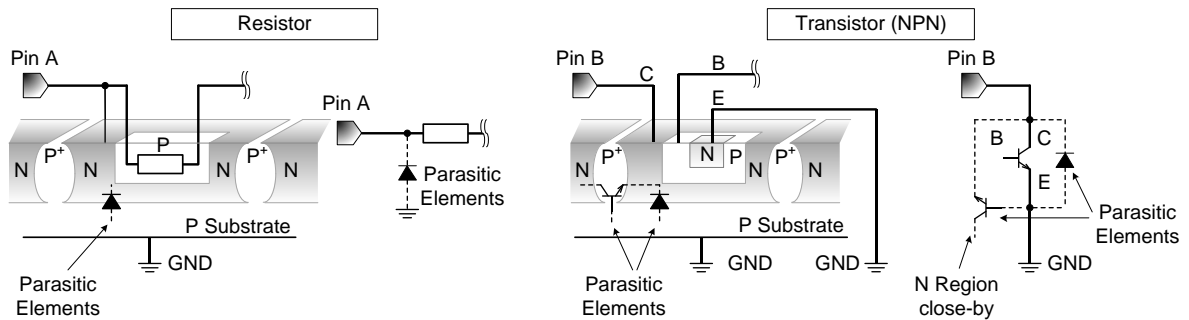
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

**10. Regarding the Input Pin of the IC**

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.  
When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of Monolithic IC Structure

**11. Ceramic Capacitor**

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

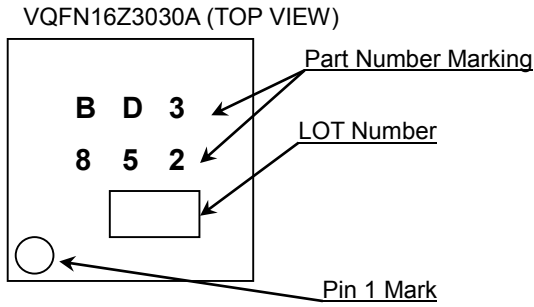
Ordering Information

B D 3 8 5 2 M U Z - ZTR

Package  
MUZ:  
VQFN16Z3030A

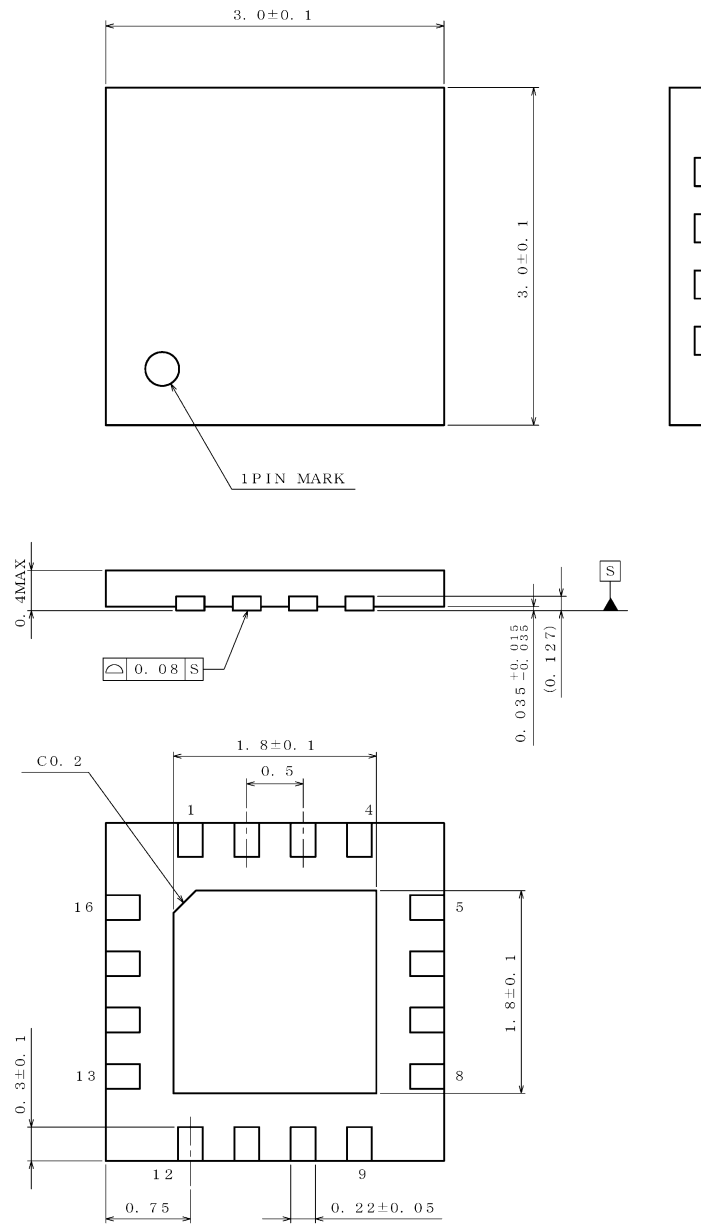
Packaging and forming specification  
TR: Embossed tape and reel

Marking Diagram



Physical Dimension and Packing Information

Package Name	VQFN16Z3030A
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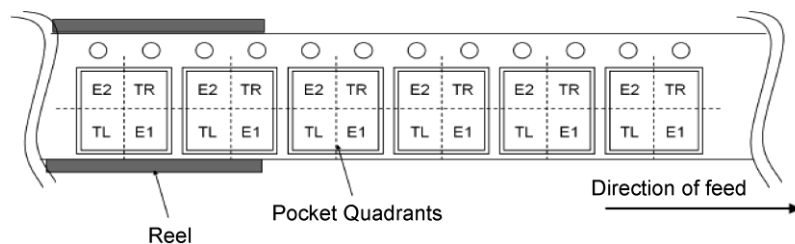


(UNIT : mm)

PKG : VQFN16Z3030A  
Drawing No. EX001-0029

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	TR The direction is the pin 1 of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
11.Mar.2020	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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  - Use of the Products in places subject to dew condensation
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- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
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- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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**Precaution for Storage / Transportation**

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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