HARRIS SEMICONDUCTOR

RFD8P06LE, RFD8P06LESM, RFP8P06LE

8A, 60V, 0.300 Ohm, ESD Rated, Logic Level, P-Channel Power MOSFET

July 1997

Features

- 8A, 60V
- $r_{DS(ON)} = 0.300\Omega$
- 2kV ESD Protected
- *Temperature Compensating* PSPICE Model
- PSPICE Thermal Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFD8P06LE	TO-251AA	F8P6LE
RFD8P06LESM	TO-252AA	F8P6LE
RFP8P06LE	TO-220AB	FP8P06LE

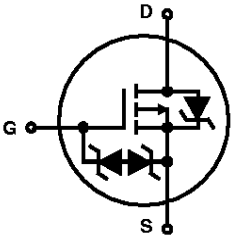
NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RFD8P06LESM9A.

Description

These products are P-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

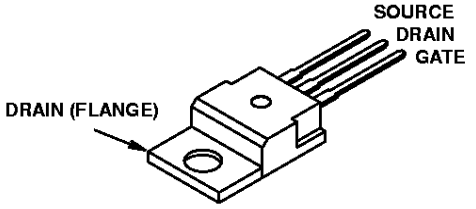
Formerly developmental type TA49203.

Symbol

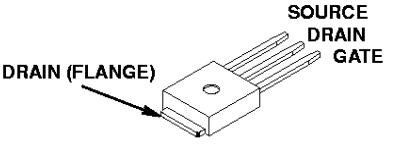


Packaging

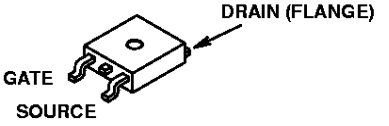
JEDEC TO-220AB



JEDEC TO-251AA



JEDEC TO-252AA



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

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File Number **4273**

Absolute Maximum Ratings $T_C = 25^oC$ Unless Otherwise Specified

		RFD8P06LE, RFD8P06LESM, RFP8P06LE	UNITS
Drain to Source Voltage	V_{DS}	-60	V
Drain to Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	-60	V
Continuous Drain Current			
$T_C = 25^oC$	I_D	-8	A
$T_C = 100^oC$	I_D	-6.3	A
Pulsed Drain Current	I_{DM}	See Figure 5	
Gate to Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation	P_D	48	W
Dissipation Derating Factor		0.32	W/^{o}C
Single Pulse Avalanche Energy Rating	E_{AS}	See Figure 6	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^{o}C
Maximum Lead Temperature for Soldering (0.063in (1.6mm) from case for 10s)	T_L	300	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_C = 25^oC$ Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA		-1	-	-2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =- 60V, V_{GS} = 0V	$T_J = 25^oC$	-	-	-1	μA
			$T_J = 150^oC$	-	-	-50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	±10	μA
On Resistance (Note 1)	$r_{DS(ON)}$	I_D = 8A, V_{GS} = -5V		-	-	0.300	Ω
		I_D = 8A, V_{GS} = -4.5V		-	-	0.330	Ω
Turn-On Time	t_{ON}	V_{DD} = -30V, $I_D \cong$ 8A, R_{GS} = 9.1Ω, R_L = 3.75Ω		-	-	90	ns
Turn-On Delay Time	$t_{d(ON)}$			-	10	-	ns
Rise Time	t_r			-	50	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	30	-	ns
Fall Time	t_f			-	20	-	ns
Turn-Off Time	t_{OFF}			-	-	75	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0 to -10V	V_{DD} = -48V, $I_D \cong$ 8A, R_L = 6Ω	-	25	30	nC
Gate Charge at -5V	$Q_{g(-5)}$	V_{GS} = 0 to -5V		-	15	18	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0 to -1V		-	1.2	1.5	nC
Input Capacitance	C_{ISS}	V_{DS} =- 25V, V_{GS} = 0V, f = 1MHz (Figure 15)		-	675	-	pF
Output Capacitance	C_{OSS}			-	175	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	50	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	3.125	^{o}C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251AA, TO-252AA		-	-	100	^{o}C/W
		TO-220AB				80	^{o}C/W

Source to Drain Diode Specifications $T_C = 25^oC$ Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 1)	V_{SD}	$T_J = 25^oC$, I_{SD} =- 8A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, I_{SD} =- 8A, dI_{SD}/dt = 100A/μs	-	-	125	ns

NOTE:

1. Pulse Test: Pulse width ≤300μs, Duty Cycle ≤2%.

Typical Performance Curves Unless Otherwise Specified

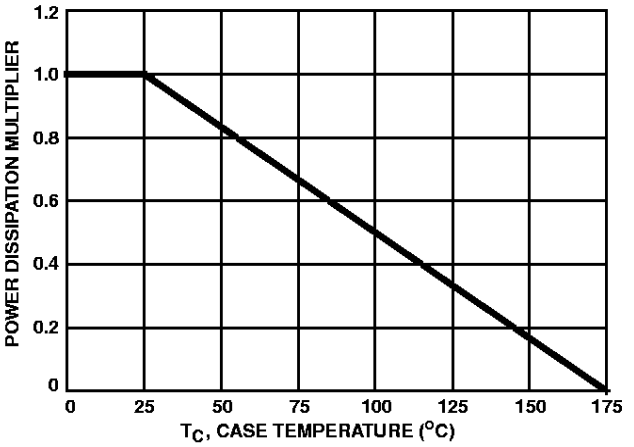


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

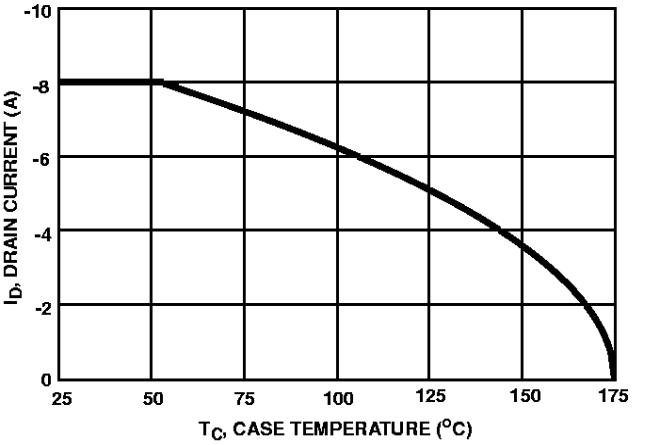


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

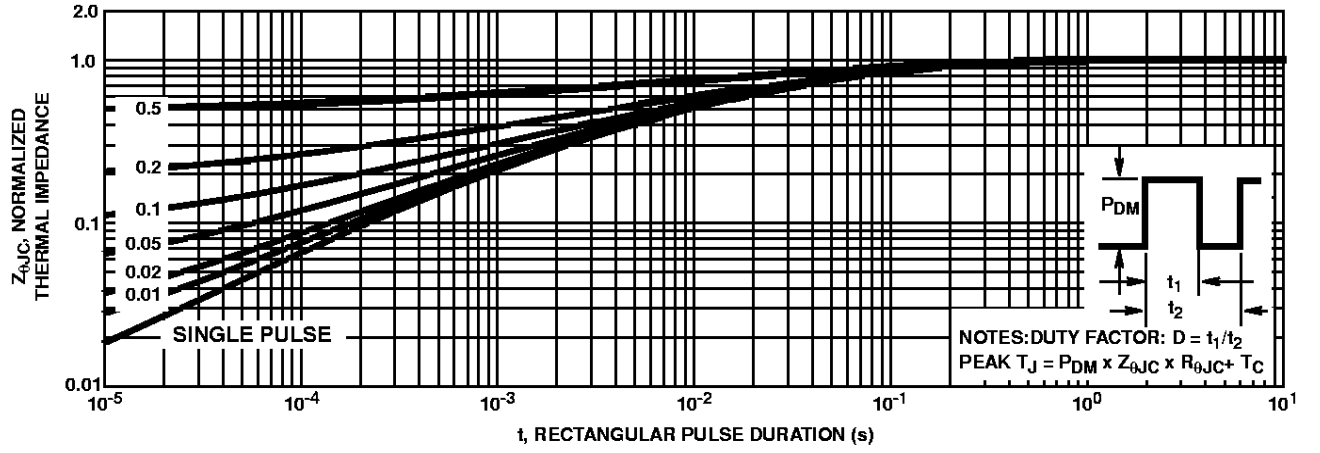


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

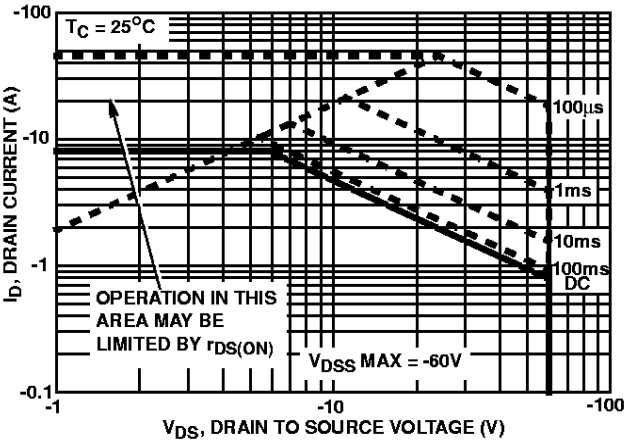


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

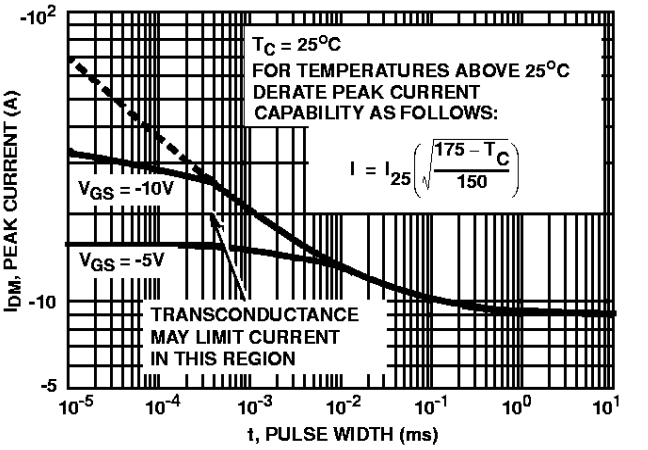
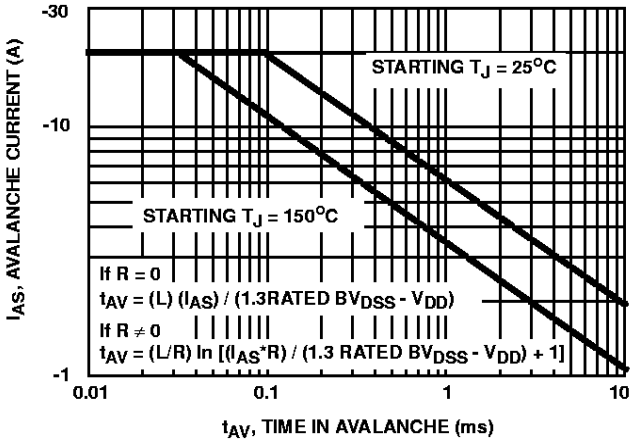


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified



NOTE: Refer to Harris Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

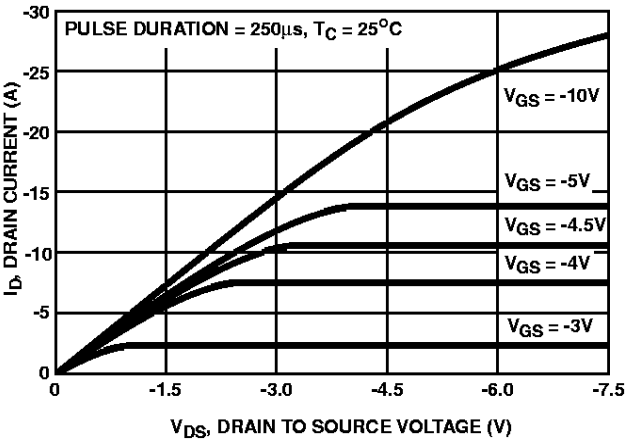


FIGURE 7. SATURATION CHARACTERISTICS

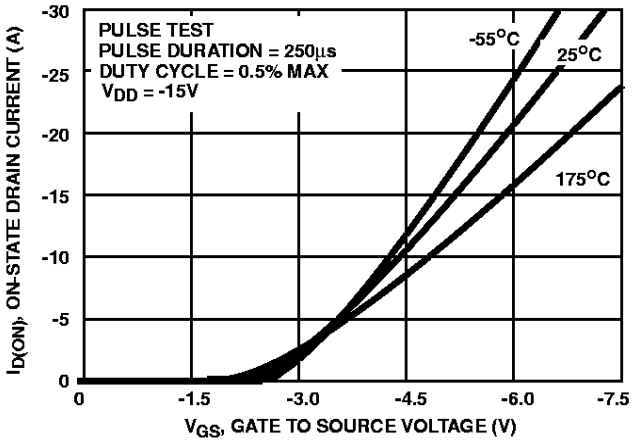


FIGURE 8. TRANSFER CHARACTERISTICS

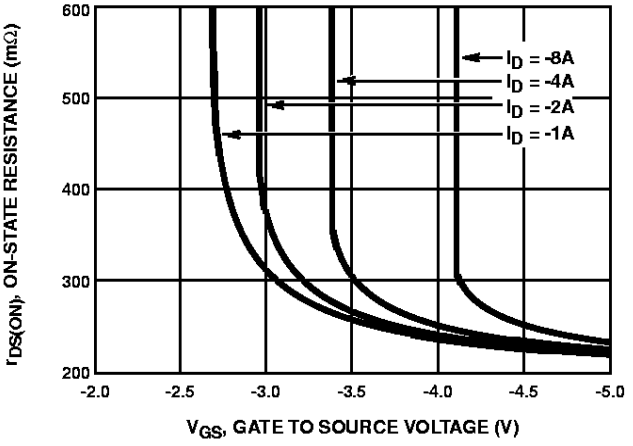


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

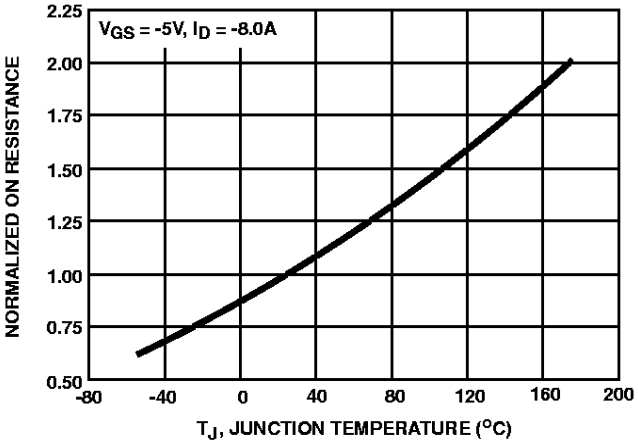


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

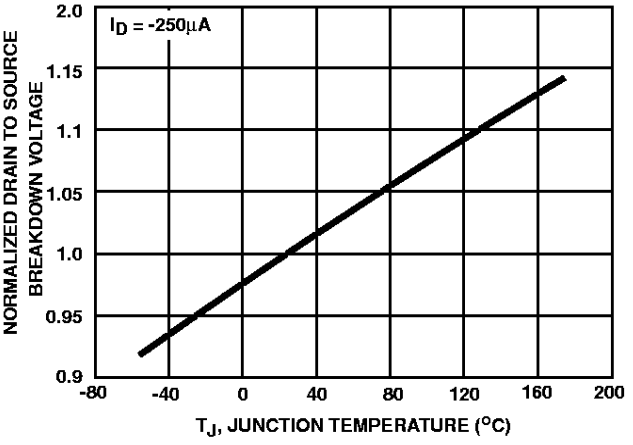


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified

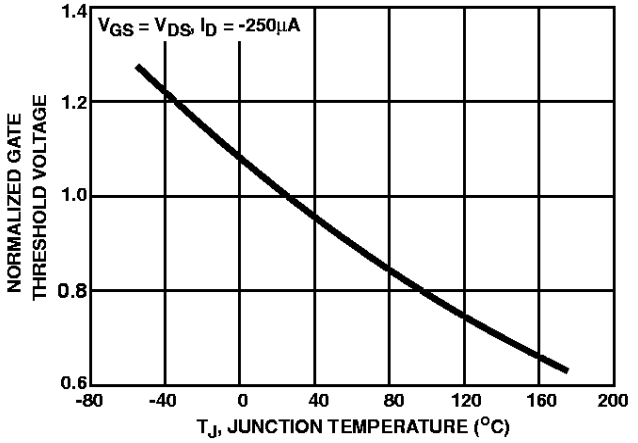


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

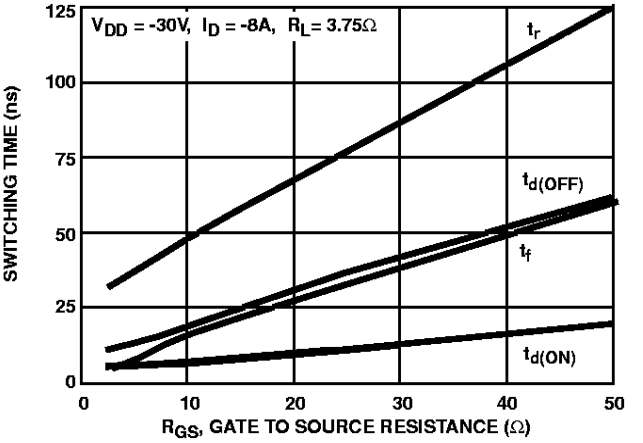
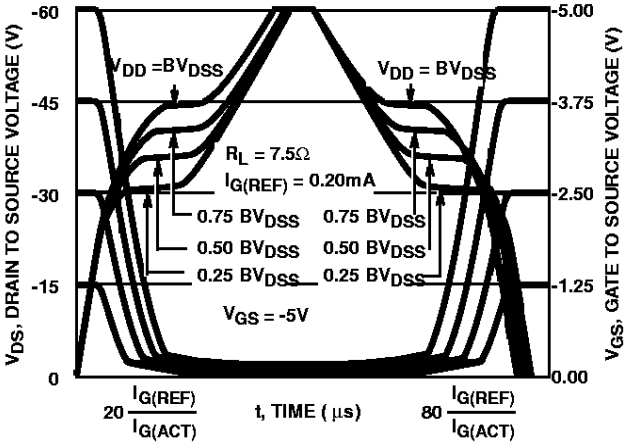


FIGURE 13. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE



NOTE: Refer to Application Note AN7254 and AN7260.

FIGURE 14. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

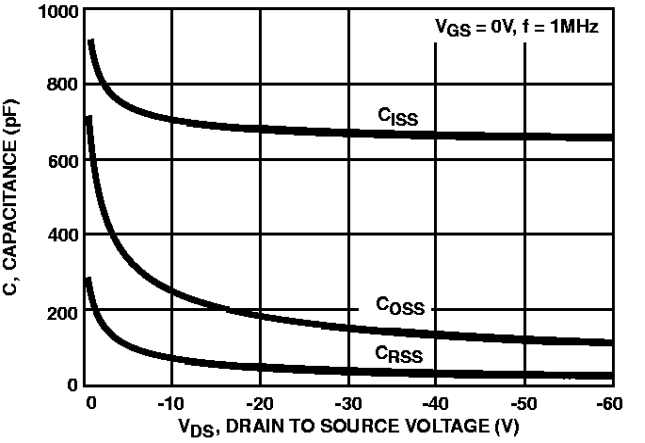


FIGURE 15. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Test Circuits and Waveforms

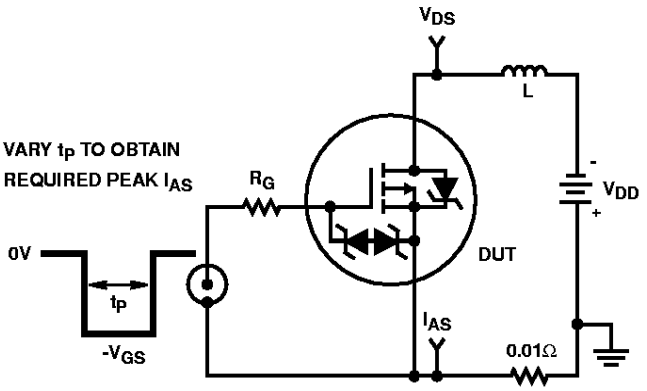


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

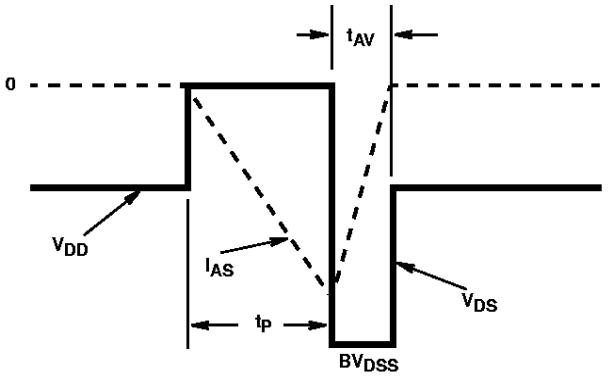


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

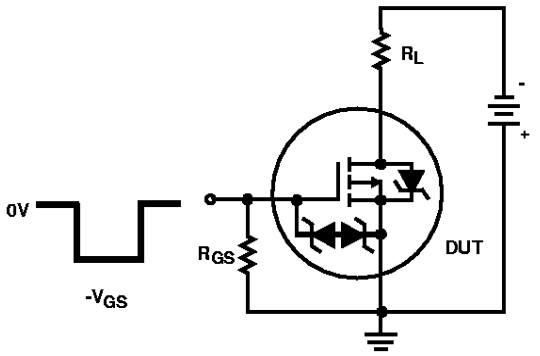


FIGURE 18. SWITCHING TIME TEST CIRCUIT

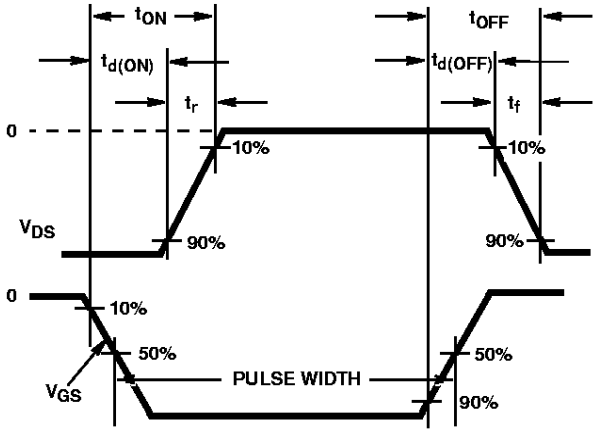


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

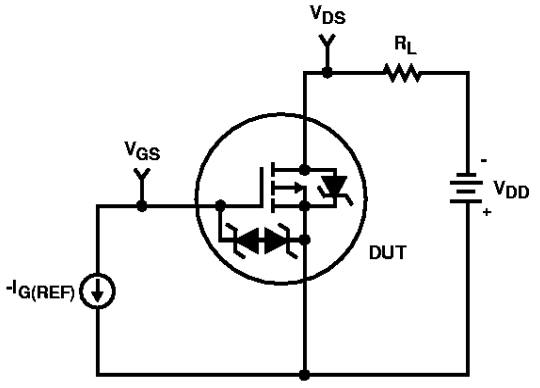


FIGURE 20. GATE CHARGE TEST CIRCUIT

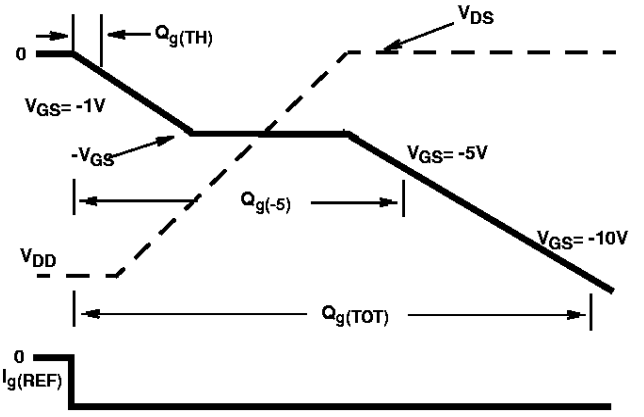
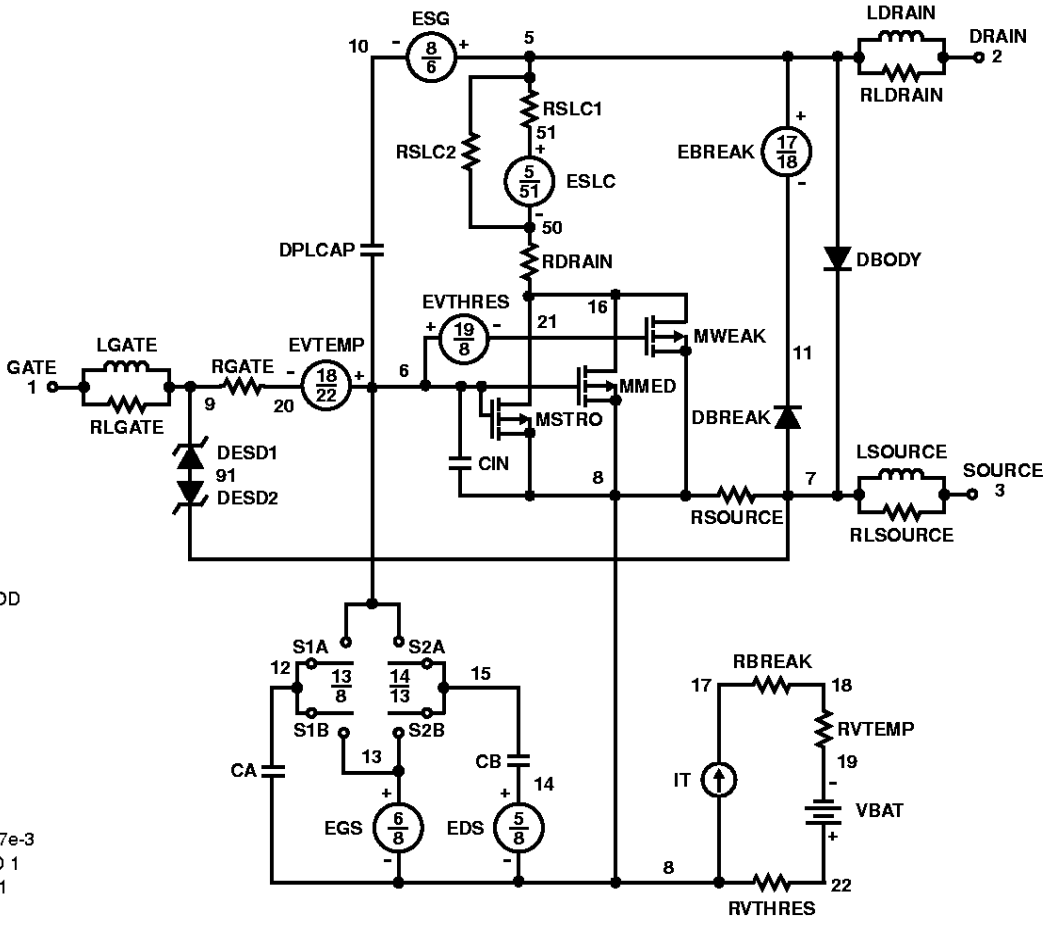


FIGURE 21. GATE CHARGE WAVEFORMS

PSpice Electrical Model

```
.SUBCKT RFD8P06LE  2  1  3        REV 7/29/96

CA 12 8 1.50e-9
CB 15 14 1.50e-9
CIN 6 8 6.30e-10

DBODY 5  7  DBDMOD
DBREAK 7 11 DBKMOD
DESD1  91  9  DESD1MOD
DESD2  91  7  DESD2MOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18  -67.9
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTHRES 21 6 19 8 1
EVTEMP 6 20 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-10
LGATE 1 9 2.92e-9
LSOURCE 3 7 2.92e-9

MSTRONG 16 6 8 8 MstrongMOD
MMED 16 6 8 8 MmedMOD
MWEAK 16 21 8 8 MweakMOD

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 95e-3
RGATE 9 20 2.89
RIN 6 8 1e9
RSCL1  5  51  RSCLMOD  1e-6
RSCL2  5  50  1e3
RSOURCE 8 7 RSourceMOD 97e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESCL  51  50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/26,7))}

.MODEL DBDMOD D (IS=2.5e-12 RS=4e-2 IKF=0.01 N=0.97 TIKF=0.012 TRS1=0.8e-4 TRS2=-5e-6 CJO=5.25e-10 VJ=0.75 M=0.41 TT=7.50e-8)
.MODEL DBKMOD D (IKF=5 N=0.75 RS=0.245 TRS1=1e-3 TRS2=1.6e-4)
.MODEL DESD1MOD D (BV=16.4 TBV1=-1.25e-3  TBV2=5.79e-7  RS=36  NBV=50  IBV=7e-6)
.MODEL DESD2MOD D (BV=16.2 TBV1=-8.3e-4  TBV2=8.9e-7  NBV=50  IBV=7e-6)
.MODEL DPLCAPMOD D (CJO=4.25e-10 IS=1e-30 N=10 VJ=0.499 M=0.561)
.MODEL MSTRONGMOD PMOS (VTO=-1.91 KP=11.55 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MMEDMOD PMOS (VTO=-1.51 KP=0.95 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MWEAKMOD PMOS (VTO=-1.18 KP=0.03 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=1.045e-3 TC2=-3.5e-7)
.MODEL RDSMOD RES (TC1=0.92e-2 TC2=1.55e-5)
.MODEL RSOURCEMOD RES (TC1=2e-3 TC2=0.5e-6)
.MODEL RSCLMOD  RES (TC1=2e-3  TC2=0)
.MODEL RVTHRESMOD RES (TC1=-2.5e-3 TC2=0)
.MODEL RVTEMPMOD RES (TC1=-1.55e-3 TC2=7.5e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=5.25 VOFF=1.75)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.75 VOFF=5.25)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.5 VOFF=-0.5)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=0.5)
.ENDS
```



NOTE: For further discussion of the PSPICE model consult A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options; authored by William J. Hepp and C. Frank Wheatley.

PSpice Thermal Model

REV 7/29/96

RFP8P06LE

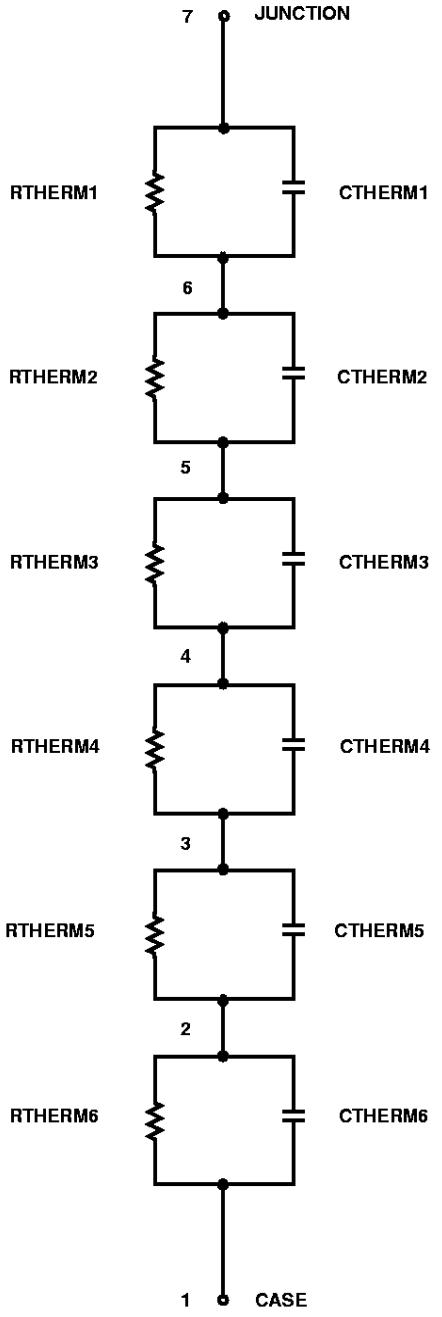
CTHERM1 7 6 1.3e-4
CTHERM2 6 5 4.5e-4
CTHERM3 5 4 1e-3
CTHERM4 4 3 2e-3
CTHERM5 3 2 1.5e-2
CTHERM6 2 1 0.55

RTHERM1 7 6 3.0e-2
RTHERM2 6 5 5.0e-2
RTHERM3 5 4 0.1
RTHERM4 4 3 1.15
RTHERM5 3 2 1.20
RTHERM6 2 1 0.55

RFD8P06LE, RFD8P06LESM

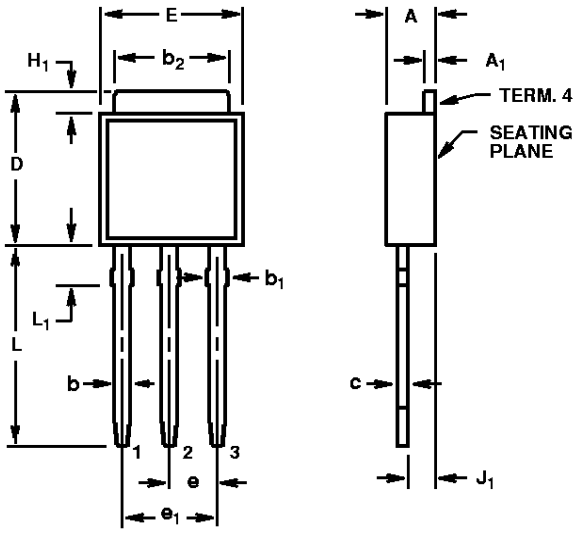
CTHERM1 7 6 1.3e-4
CTHERM2 6 5 4.5e-4
CTHERM3 5 4 1e-3
CTHERM4 4 3 2e-3
CTHERM5 3 2 1.5e-2
CTHERM6 2 1 0.12

RTHERM1 7 6 3.0e-2
RTHERM2 6 5 5.0e-2
RTHERM3 5 4 0.1
RTHERM4 4 3 1.15
RTHERM5 3 2 1.20
RTHERM6 2 1 0.55



TO-251AA

3 LEAD JEDEC TO-251AA PLASTIC PACKAGE



LEAD NO. 1 - GATE
LEAD NO. 2 - DRAIN
LEAD NO. 3 - SOURCE
TERM. 4 - DRAIN

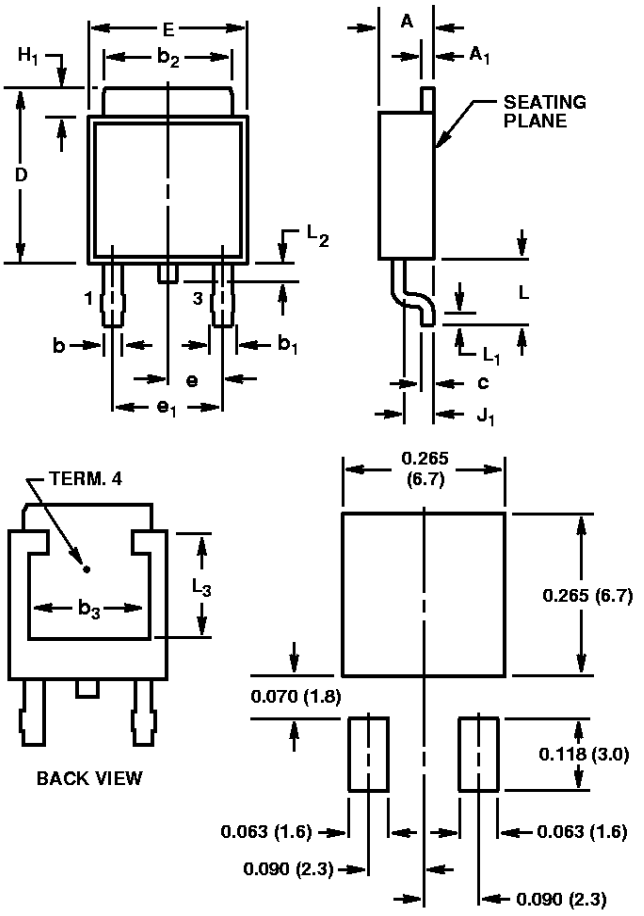
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	3, 4
b	0.028	0.032	0.72	0.81	3, 4
b_1	0.033	0.040	0.84	1.01	3
b_2	0.205	0.215	5.21	5.46	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		5
e_1	0.180 BSC		4.57 BSC		5
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	6
L	0.355	0.375	9.02	9.52	-
L_1	0.075	0.090	1.91	2.28	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-251AA outline dated 9-88.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 10-95.

TO-252AA

SURFACE MOUNT JEDEC TO-252AA PLASTIC PACKAGE



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

LEAD NO. 1 - GATE

LEAD NO. 3 - SOURCE

TERM. 4 - DRAIN

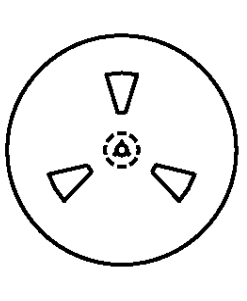
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	4, 5
b	0.028	0.032	0.72	0.81	4, 5
b_1	0.033	0.040	0.84	1.01	4
b_2	0.205	0.215	5.21	5.46	4, 5
b_3	0.190	-	4.83	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		7
e_1	0.180 BSC		4.57 BSC		7
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	-
L	0.100	0.115	2.54	2.92	-
L_1	0.020	-	0.51	-	4, 6
L_2	0.025	0.040	0.64	1.01	3
L_3	0.170	-	4.32	-	2

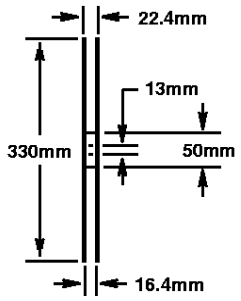
NOTES:

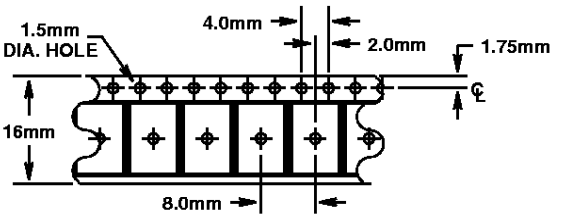
1. These dimensions are within allowable dimensions of Rev. B of JEDEC TO-252AA outline dated 9-88.
2. L_3 and b_3 dimensions establish a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.090 inches (2.28mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 6 dated 10-96.

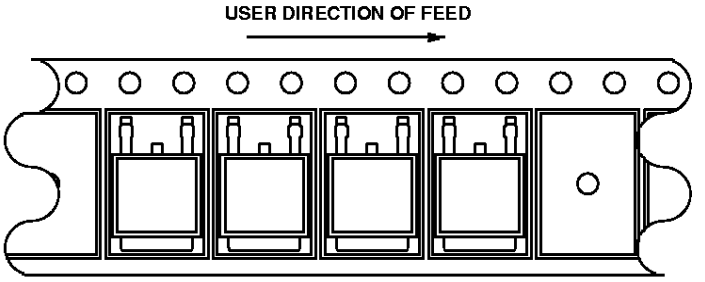
TO-252AA

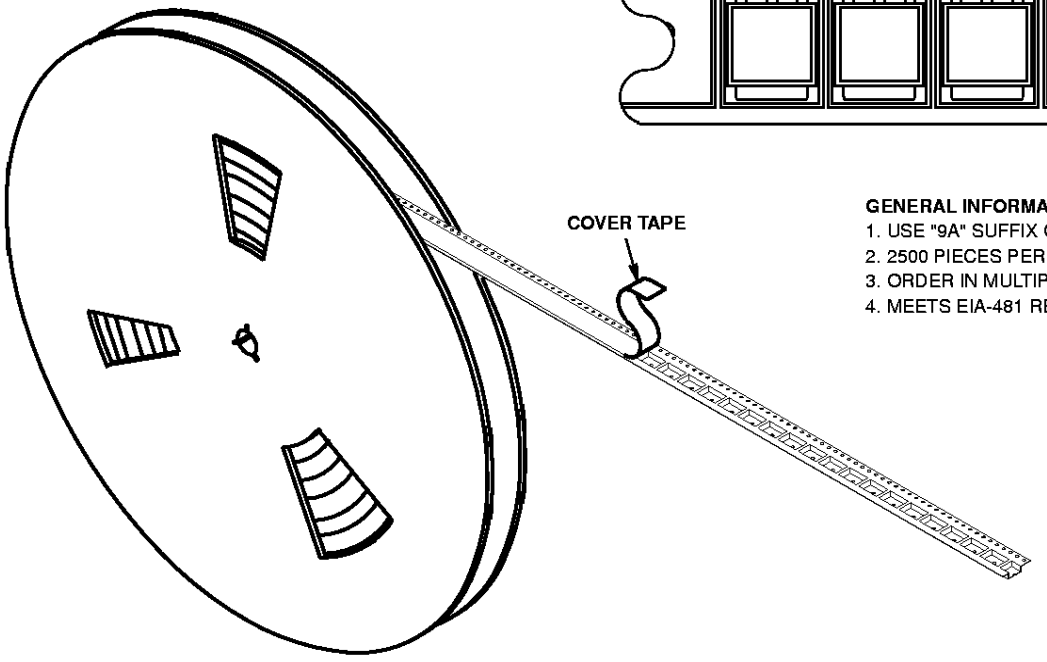
16mm TAPE AND REEL











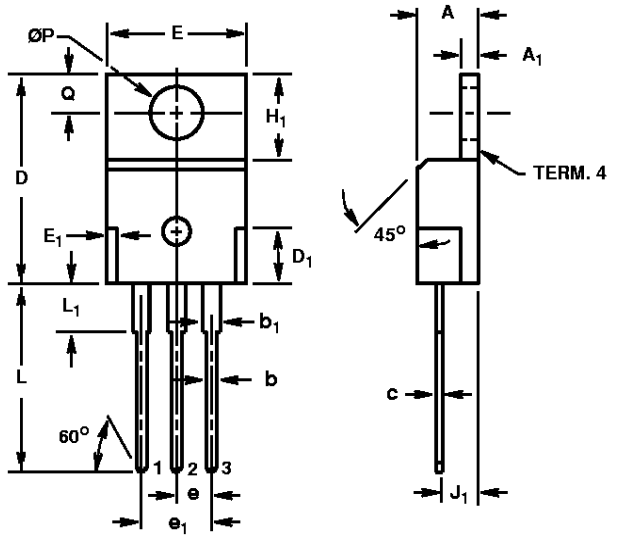
GENERAL INFORMATION

1. USE "9A" SUFFIX ON PART NUMBER.
2. 2500 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 6 dated 10-96

TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



LEAD NO. 1 - GATE
LEAD NO. 2 - DRAIN
LEAD NO. 3 - SOURCE
TERM. 4 - DRAIN

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L_1	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

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