ANALOG DEVICES

T-73-53

Voltage Comparator

AD96685/AD96687

1.1 Scope.

This specification covers the requirements for an ultrafast voltage comparator. The AD96685 is a single comparator with a 2.5 ns propagation delay, and the AD96687 is an equally fast dual comparator.

1.2 Part Number.

The complete part number per Table 1 this specification is as follows:

Device	Part Number
−1	AD96685T(X)/883B
−2	AD96687T(Y)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	(Y)	Package	Description
E	E	E-20A	20-Contact LCC
Q	Q	Q-16	16-Pin Ceramic DIP
H		H-10A	10-Pin TO-100 Can

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage . . . . . ±6.5 V
Power Dissipation . . . . . AD96685 = 500 mW; AD96687 = 600 mW
Input Voltage Range . . . . . ±5 V
Differential Input Voltage . . . . . 5.5 V
Output Current . . . . . 30 mA
Latch Enable Voltage . . . . . $-V_S$ to 0 V
Junction Temperature . . . . . +175°C
Operating Temperature Range (Case) . . . . . −55°C to +125°C
Storage Temperature Range (Case) . . . . . −65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . . +300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 31°C for E-20A (AD96687)
θ_{JA} = 82°C/W for E-20A (AD96687)
θ_{JC} = 65°C/W for E-20A (AD96685)
θ_{JA} = 172°C/W for E-20A (AD96685)
θ_{JC} = 52°C/W for H-10A
θ_{JA} = 172°C/W for H-10A
θ_{JC} = 57°C/W for Q-16
θ_{JA} = 115°C/W for Q-16

AD96685/AD96687 – SPECIFICATIONS

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Test	Symbol	Device	Design Limit @+25°C	Sub Group 1	Sub Group[2] 2, 3	Sub Group 4	Sub Group[2, 3, 4, 5] 5, 6	Sub Group 9	Test Condition[1]	Units
Input Offset Current	I_{IO}	−1	±1	±1	±1.6				V_{CM} = +0.5 V	µA max
		−2	±1	±1	±1.2				V_{CM} = 0 V; +0.5 V $-V_{CM}$ = −0.5 V	
Input Offset Voltage	V_{OS}	−1	±2	±2.0	±3.0				R_S = 100 Ω	mV max
		−2	±2	±2.0	±3.0				V_{CM} = 0 V	
Input Offset Voltage Tempco	$\Delta V_{OS}/\Delta T$	−1	±20	±20	±20				R_S = 100 Ω V_{CM} = 0 V	µV/°C max
		−2	±20	±20	±20					
Input Bias Current	I_{IB}	−1	10	10	16				$+V_{CM}$ = +0.5 V $-V_{CM}$ = −0.5 V	µA max
		−2	10	10	16				R_S = 100 Ω V_{CM} = 0 V; ±0.5 V	
Input Voltage Range	V_{CM}	−1, 2	−2.5	−2.5	−2.5					V min
			+5.0	+5.0	+5.0					V max
Common Mode Rejection Ratio	CMRR	−1, 2	90			80	80		−2.5 V ≤ V_{CM} ≤ +5.0 V	dB min
Power Supply Rejection Ratio	PSRR	−1	70			60	60		R_S = 100 Ω ΔV_S = ±5%	dB min
		−2				60	60			
High Level Output Voltage	V_{OH}	−1, 2		−1.10	−1.10					V min
Low Level Output Voltage	V_{OL}	−1, 2		−1.50	−1.50					V max
Positive Supply Current	$+I_{CC}$	−1	9	9	9					mA max
		−2	18	18	18					
Negative Supply Current	$-I_{CC}$	−1	18	18	18					mA max
		−2	36	36	36					
Propagation Delay Time	t_{PD}±	−1	2.5					9	See Note 6	ns max
		−2	2.5					1.5		ns min
								3.5		ns max
Propagation Delay Time Latch Enable to Output	$t_{PD\pm(E)}$	−1	2.5					3.5		ns max
		−2	2.5					3.5		

NOTES
[1]Unless otherwise specified, T_A = +25°C; $+V_S$ = +5.0 V; V_S = −5.2 V.
[2]−55°C ≤ T_A ≤ +125°C.
[3]$+V_S$ = +5.0 V; V_S = −5.2 V; V_T = −2.0 V; R_L = 50 Ω.
[4]Devices require a thermal equilibrium to be established with a transverse airflow of >500 LFPM.
[5]Production pulse test devices at correlated temperatures of −35°C and +145°C to compensate for high power steadystate operation.
[6]This parameter measured with 100 mV pulse (10 mV overdrive), to 50% of the transition output point.

Table 1.

REV. A

3.2.1 Functional Block Diagram and Terminal Assignments.

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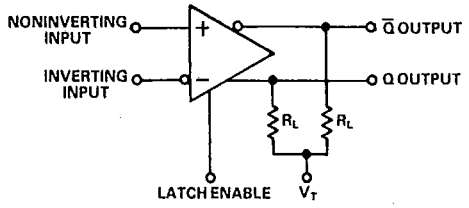
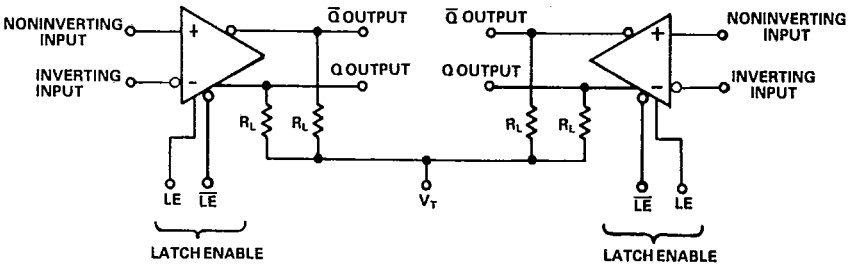


AD96685

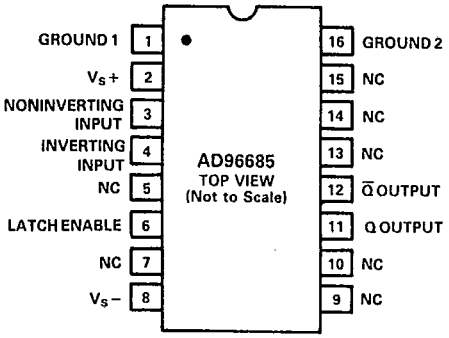


THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω – 200Ω CONNECTED TO –2.0V, OR 200Ω – 2000Ω

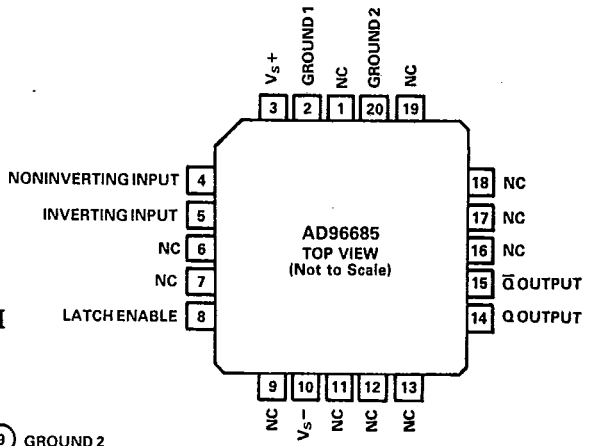
AD96687

Pin Assignments

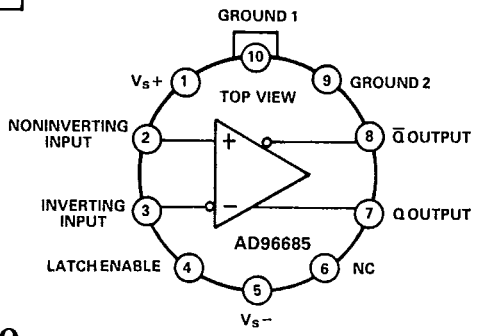
AD96685TQ



AD96685TE

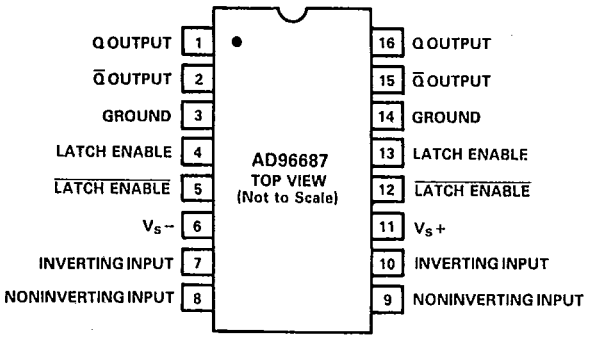


AD96685TH

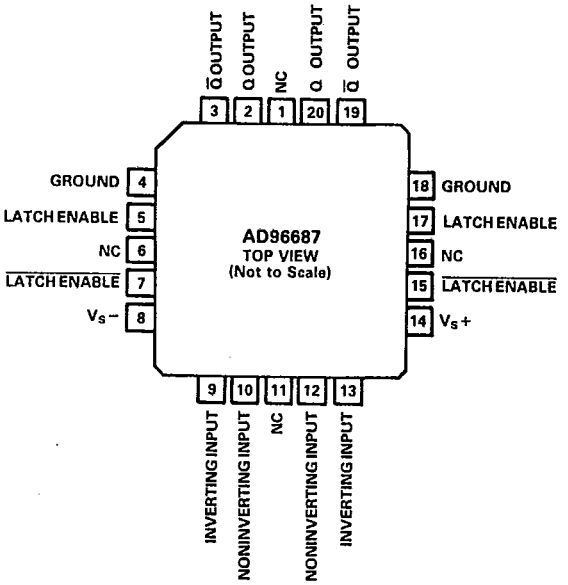


(PIN 5 CONNECTED TO CASE)

AD96687TQ



AD96687TE



AD96685/AD96687

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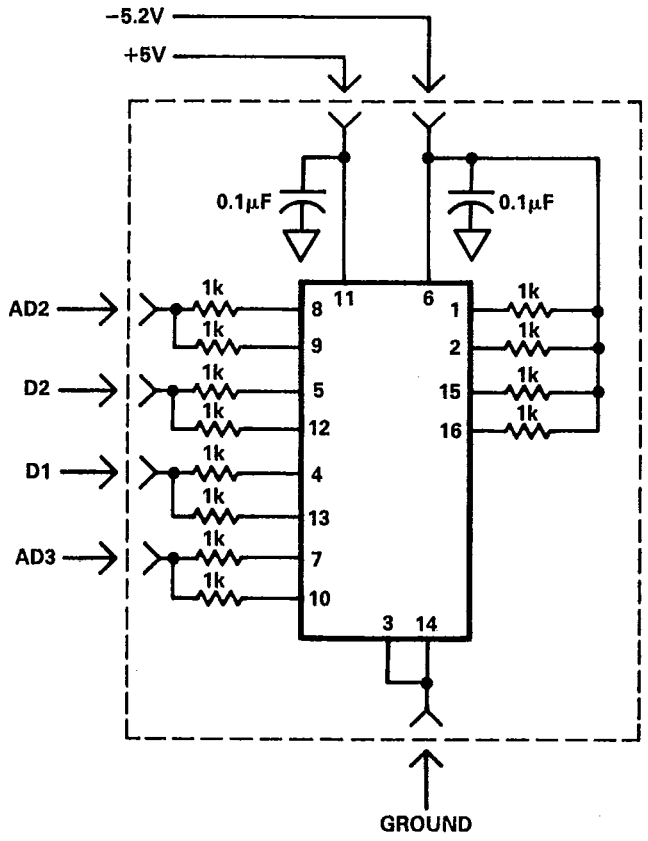
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (D-50).

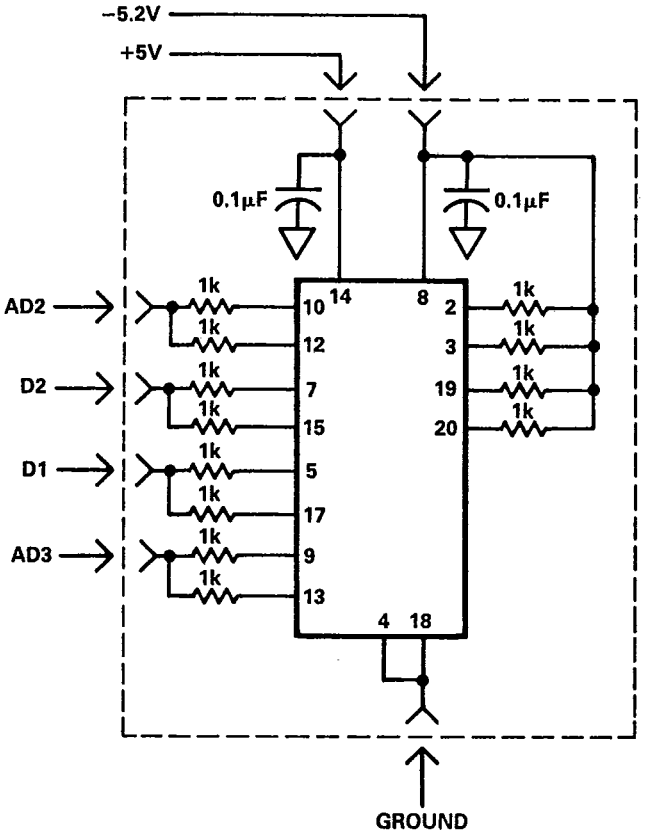
4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ALL RESISTORS ±5%
$+V_S$ = +5.0V ±5%
$-V_S$ = −5.2V ±5%

AD96687 (16-Pin DIP)



ALL RESISTORS ±5%
$+V_S$ = +5.0V ±5%
$-V_S$ = −5.2V ±5%

AD96687 (20-Pin LCC)

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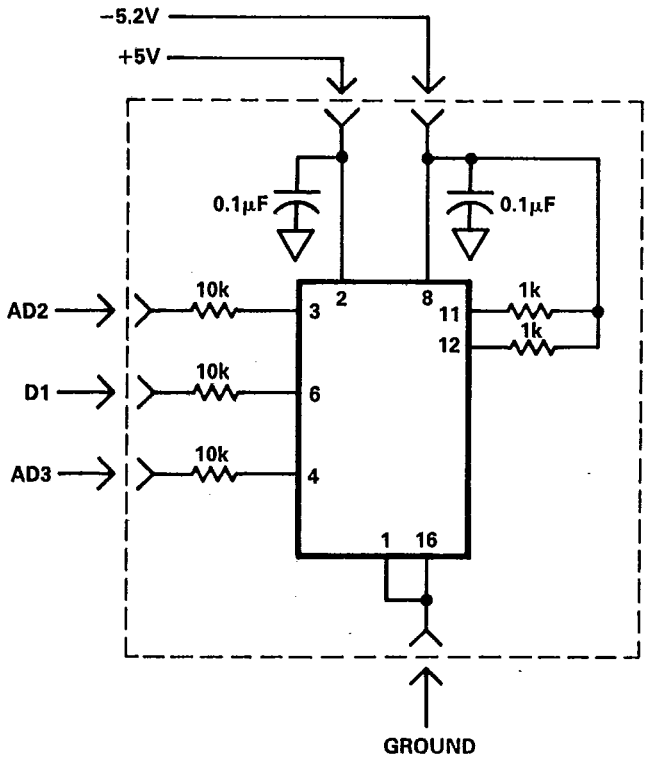
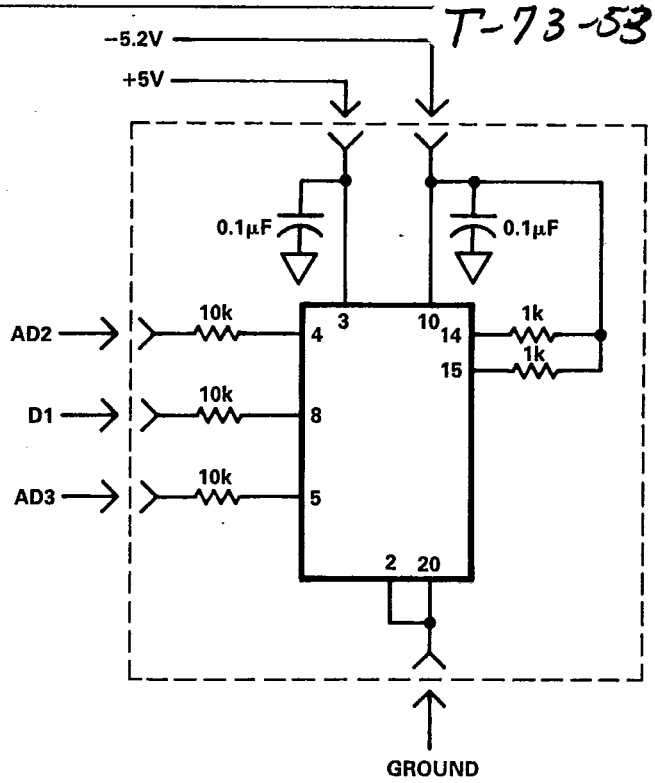


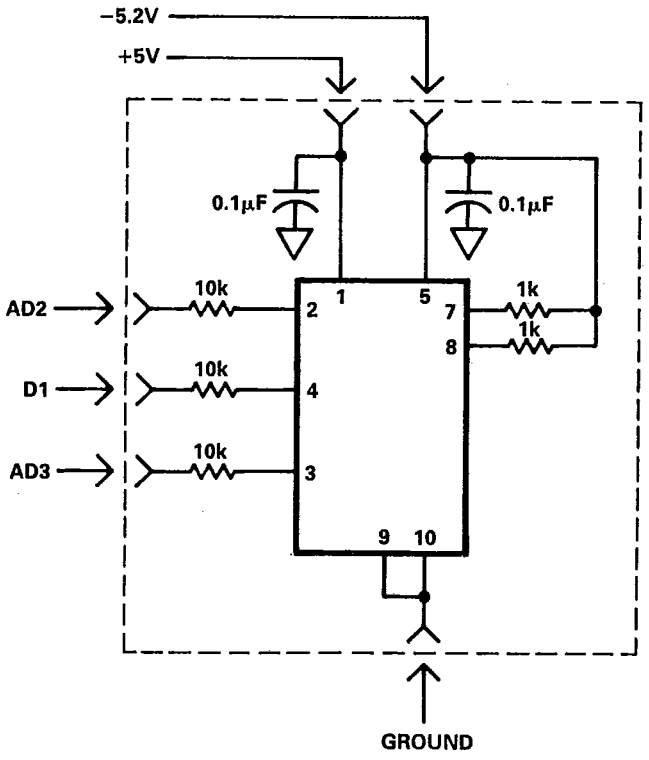
ALL RESISTORS ±5%
$+V_S$ = +5.0V ±5%
$-V_S$ = −5.2V ±5%

AD96685 (16-Pin DIP)



ALL RESISTORS ±5%
$+V_S$ = +5.0V ±5%
$-V_S$ = −5.2V ±5%

AD96685 (20-Pin LCC)



ALL RESISTORS ±5%
$+V_S$ = +5.0V ±5%
$-V_S$ = −5.2V ±5%

AD96685 (TO-100)