2N4918 - 2N4920 Series

Medium-Power Plastic PNP Silicon Transistors

These medium−power, high−performance plastic devices are designed for driver circuits, switching, and amplifier applications.

Features

- Low Saturation Voltage − $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 1.0 A
- Excellent Power Dissipation, P_D = 30 W @ T_C = 25°C
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 A
- Complement to NPN 2N4921, 2N4922, 2N4923
- Pb−Free Package is Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector − Emitter Voltage 2N4918 2N4919 2N4920	V_{CEO}	 40 60 80	Vdc
Collector − Base Voltage 2N4918 2N4919 2N4920	V_{CBO}	 40 60 80	Vdc
Emitter − Base Voltage	V_{EBO}	5.0	Vdc
Collector Current − Continuous (Note 1)	I_C (Note 2)	1.0 3.0	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	30 0.24	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The 1.0 A max I_C value is based upon JEDEC current gain requirements. The 3.0 A max value is based upon actual current−handling capability of the device (See Figure 5).
2. Indicates JEDEC Registered Data for 2N4918 Series.

THERMAL CHARACTERISTICS (Note 3)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	θ_{JC}	4.16	°C/W

3. Recommend use of thermal compound for lowest thermal resistance.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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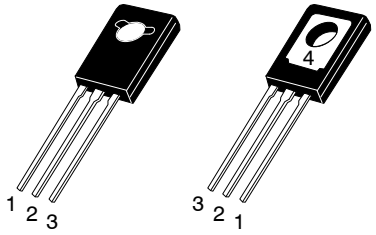
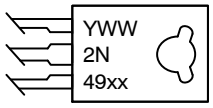
3.0 A, 40−80 V, 30 W GENERAL PURPOSE POWER TRANSISTORS



FRONT VIEW **BACK VIEW**

TO−225
CASE 077
STYLE 1

MARKING DIAGRAM



xx = 18, 19, 20
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Note 4) (I_C = 0.1 Adc, I_B = 0)	2N4918 2N4919 2N4920	$V_{CEO(sus)}$	 40 60 80	 – – –	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	 2N4918 2N4919 2N4920	I_{CEO}	 – – –	 0.5 0.5 0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C		I_{CEX}	 – –	 0.1 0.5	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 4) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		h_{FE}	 40 30 10	 – 150 –	–
Collector–Emitter Saturation Voltage (Note 4) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	–	0.6	Vdc
Base–Emitter Saturation Voltage (Note 4) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$	–	1.3	Vdc
Base–Emitter On Voltage (Note 4) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.3	Vdc
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain – Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	3.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	100	pF
Small–Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

4. Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%

ORDERING INFORMATION

Device	Package	Shipping†
2N4918	TO–225	500 Unit / Bulk
2N4919	TO–225	500 Unit / Bulk
2N4920	TO–225	500 Unit / Bulk
2N4920G	TO–225 (Pb–Free)	500 Unit / Bulk

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

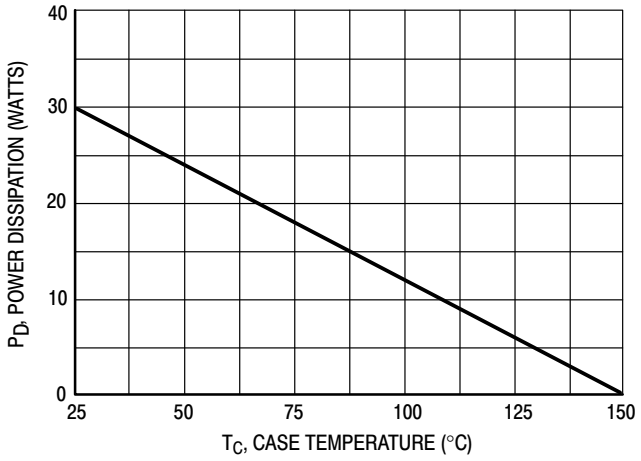


Figure 1. Power Derating

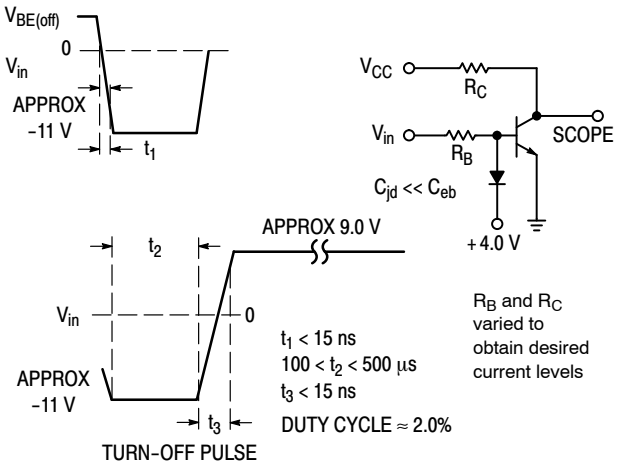


Figure 2. Switching Time Equivalent Test Circuit

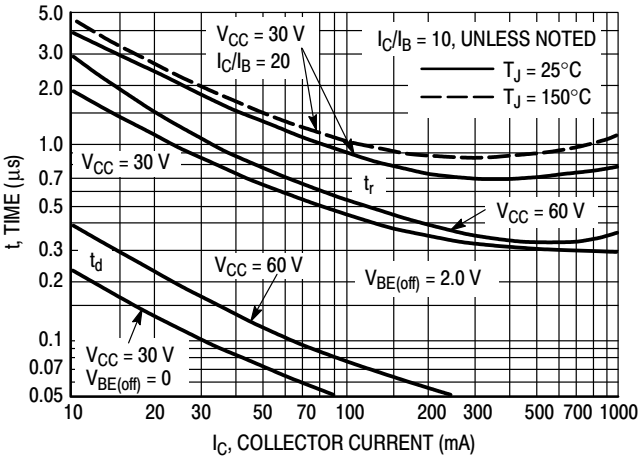


Figure 3. Turn−On Time

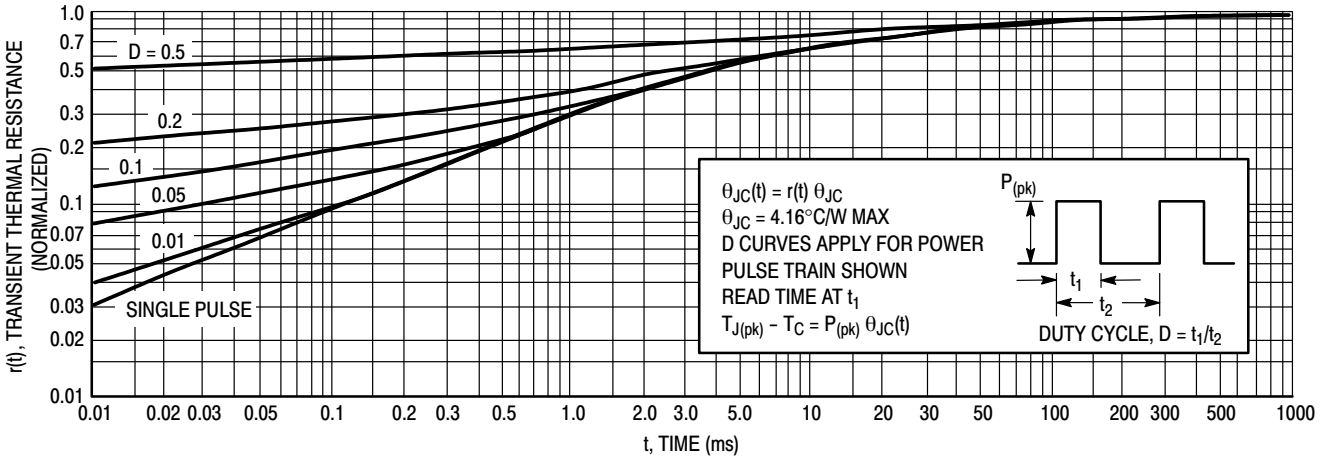


Figure 4. Thermal Response

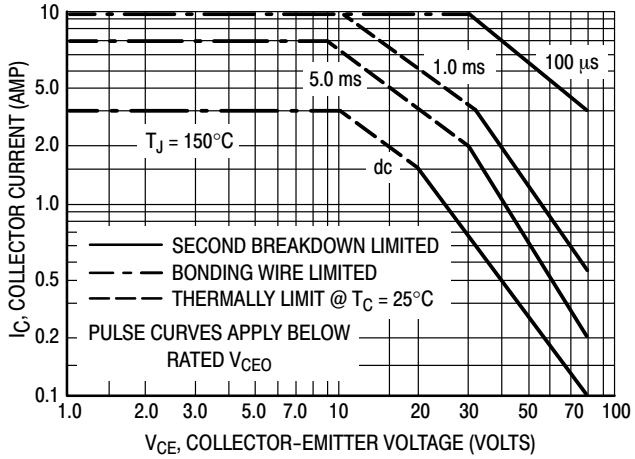


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

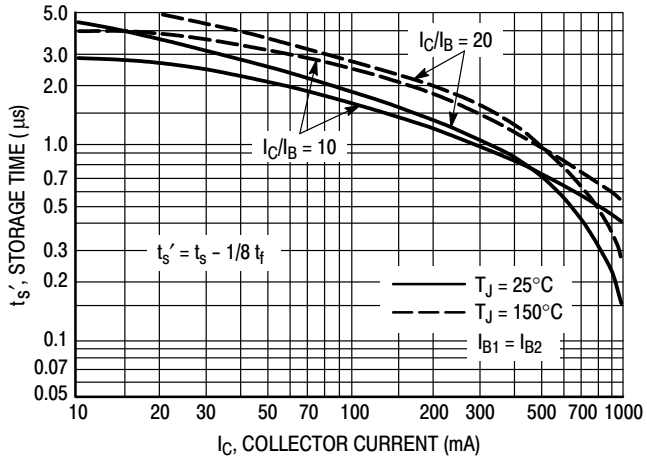


Figure 6. Storage Time

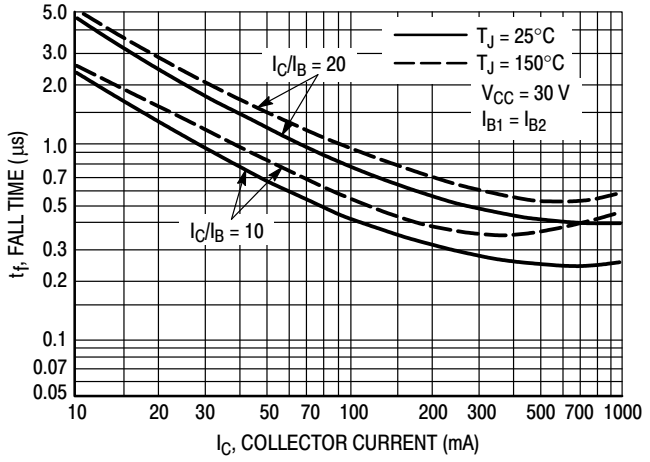


Figure 7. Fall Time

TYPICAL DC CHARACTERISTICS

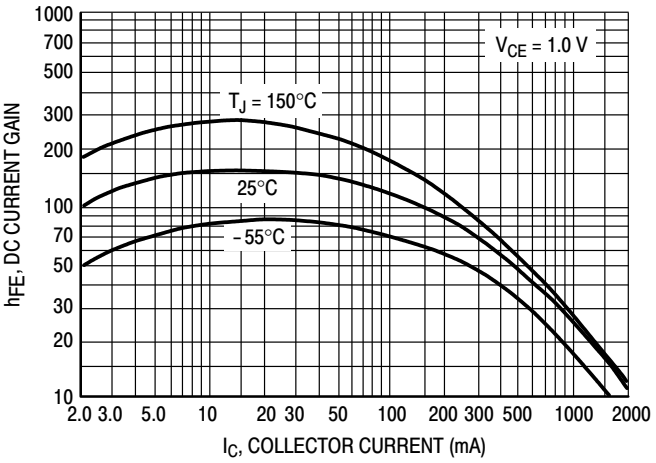


Figure 8. Current Gain

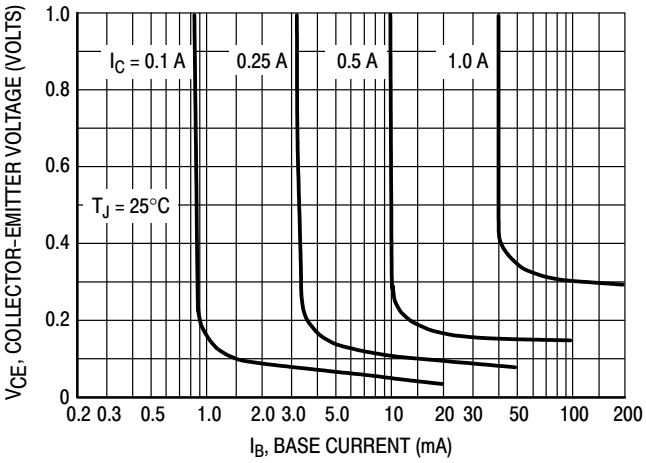


Figure 9. Collector Saturation Region

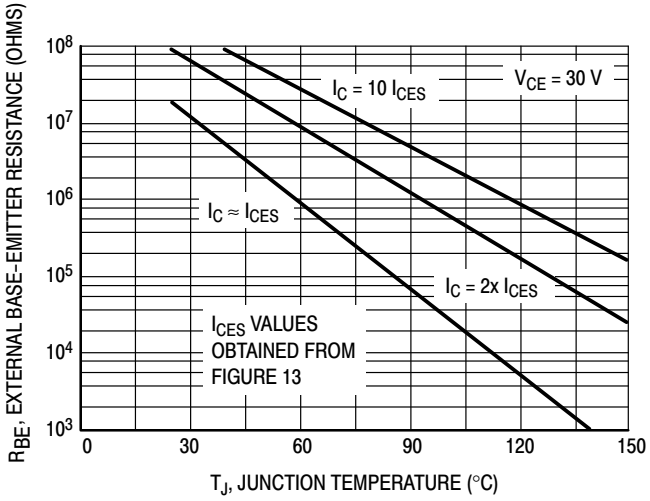


Figure 10. Effects of Base−Emitter Resistance

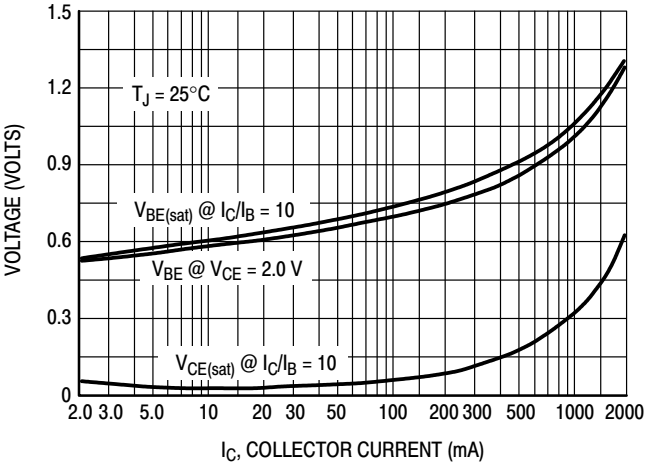


Figure 11. “On” Voltage

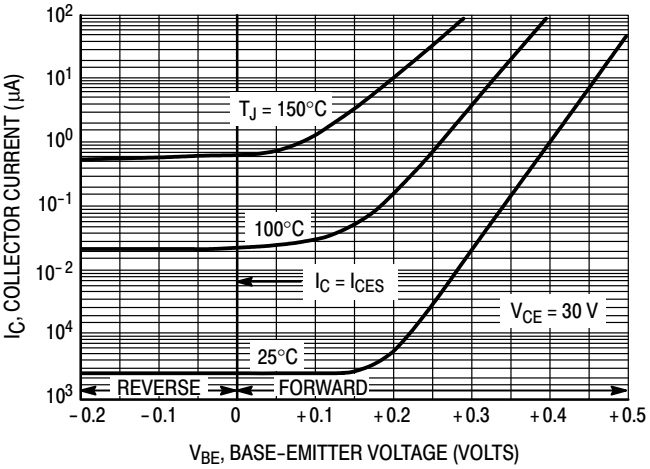


Figure 12. Collector Cut−Off Region

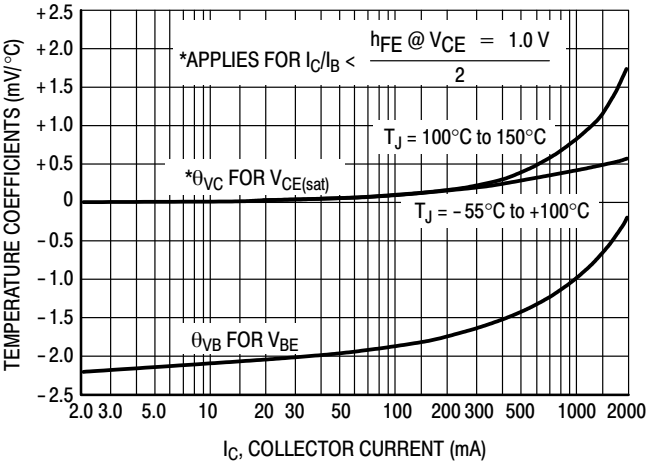


Figure 13. Temperature Coefficients

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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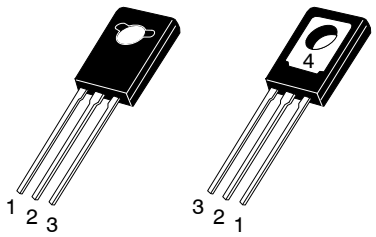
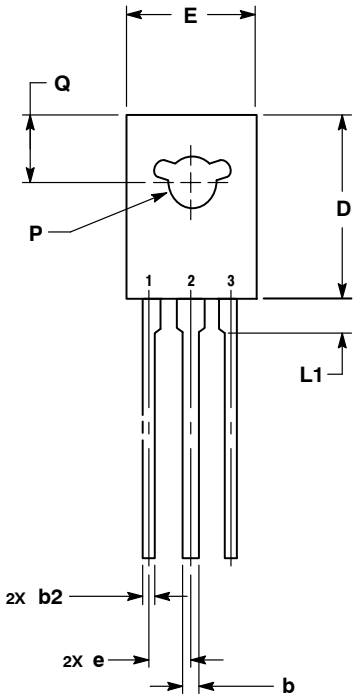
TO−225
CASE 77−09
ISSUE AD

DATE 25 MAR 2015

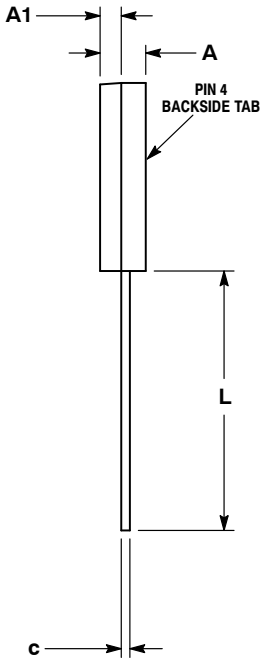


FRONT VIEW **BACK VIEW**

SCALE 1:1



FRONT VIEW

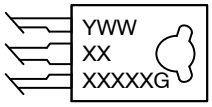


SIDE VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. NUMBER AND SHAPE OF LUGS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	2.40	3.00
A1	1.00	1.50
b	0.60	0.90
b2	0.51	0.88
c	0.39	0.63
D	10.60	11.10
E	7.40	7.80
e	2.04	2.54
L	14.50	16.63
L1	1.27	2.54
P	2.90	3.30
Q	3.80	4.20

GENERIC MARKING DIAGRAM*



Y = Year
WW = Work Week
XXXXX = Device Code
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1:
PIN 1. EMITTER
2., 4. COLLECTOR
3. BASE

STYLE 2:
PIN 1. CATHODE
2., 4. ANODE
3. GATE

STYLE 3:
PIN 1. BASE
2., 4. COLLECTOR
3. EMITTER

STYLE 4:
PIN 1. ANODE 1
2., 4. ANODE 2
3. GATE

STYLE 5:
PIN 1. MT 1
2., 4. MT 2
3. GATE

STYLE 6:
PIN 1. CATHODE
2., 4. GATE
3. ANODE

STYLE 7:
PIN 1. MT 1
2., 4. GATE
3. MT 2

STYLE 8:
PIN 1. SOURCE
2., 4. GATE
3. DRAIN

STYLE 9:
PIN 1. GATE
2., 4. DRAIN
3. SOURCE

STYLE 10:
PIN 1. SOURCE
2., 4. DRAIN
3. GATE

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DESCRIPTION:	**TO−225**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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TECHNICAL SUPPORT
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