Key Features

- SMPTE 259M and 344M compliant
- Supports data rates of 143, 177, 270, 360, and 540Mb/s
- Supports DVB-ASI at 270Mb/s
- Auto and Manual Modes for rate selection
- Standards indication in Auto Mode
- 4:1 input multiplexor
- Lock Detect Output
- On-chip Input and Output Termination
- Differential 50Ω inputs and outputs
- Mute, Bypass and Autobypass functions
- Pb-free and Green
- Single 3.3V power supply
- Operating temperature range: 0°C to 70°C

Applications

- SMPTE 259M and SMPTE 344M Serial Digital Interfaces

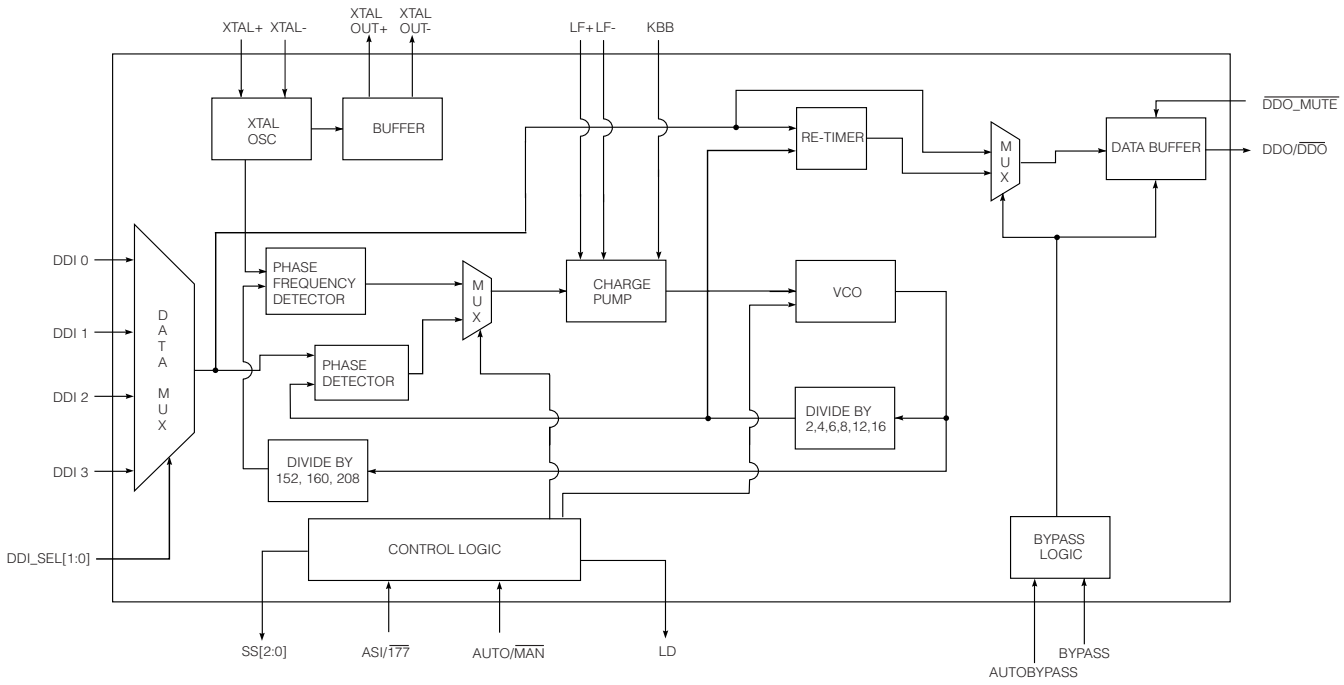
Description

The GS9065 Multi-Rate Serial Digital Reclocker is designed to automatically recover the embedded clock signal and re-time the data from a SMPTE 259M or SMPTE 344M compliant digital video signal.

The device removes the high frequency jitter components from the bit-serial stream. Input termination is on-chip for seamless matching to 50Ω transmission lines. An LVPECL compliant output interfaces seamlessly to the GS9068 Cable Driver

In Auto Mode, the GS9065 automatically detects and locks onto an incoming SMPTE SDI data signal from 143Mb/s to 540Mb/s. The GS9065 requires only one external crystal to set the VCO frequency.

The ASI/$\overline{177}$ input pin allows for manual selection of support of either 177Mb/s or DVB-ASI inputs.

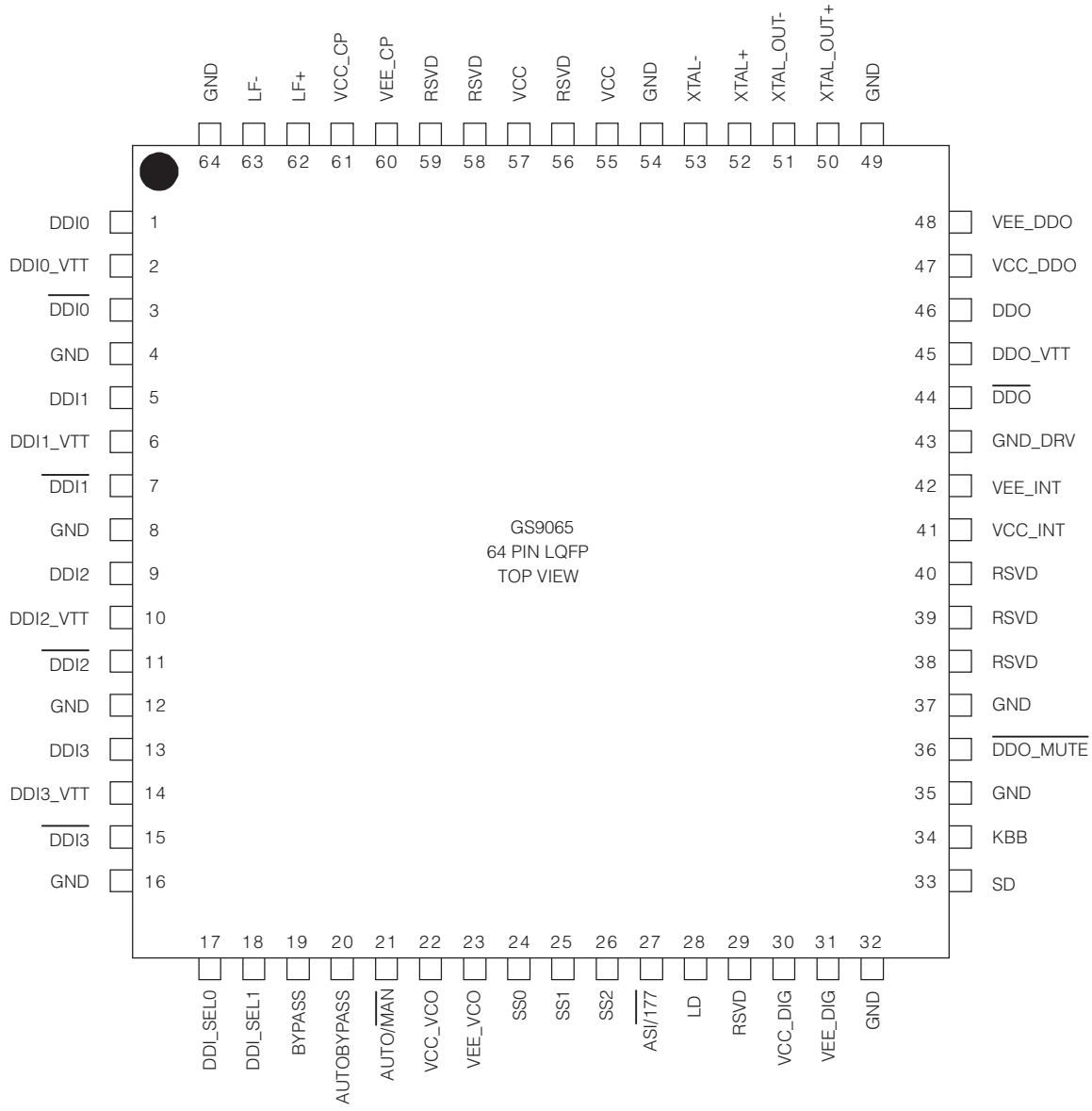


GS9065 Functional Block Diagram

Contents

1. Pin Out

1.1 Pin Assignment



1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Type	Description
1, 3	DDI0, $\overline{\text{DDI0}}$	INPUT	Serial digital differential input 0.
2	DDI0_VTT	PASSIVE	Center tap of two 50Ω on-chip termination resistors between DDI0 and $\overline{\text{DDI0}}$.
5, 7	DDI1,$\overline{\text{DDI1}}$	INPUT	Serial digital differential input 1.
6	DDI1_VTT	PASSIVE	Center tap of two 50Ω on-chip termination resistors between DDI1 and $\overline{\text{DDI1}}$.
9, 11	DDI2, $\overline{\text{DDI2}}$	INPUT	Serial digital differential input 2.
10	DDI2_VTT	PASSIVE	Center tap of two 50Ω on-chip termination resistors between DDI2 and $\overline{\text{DDI2}}$.
13, 15	DDI3, $\overline{\text{DDI3}}$	INPUT	Serial digital differential input 3 .
14	DDI3_VTT	PASSIVE	Center tap of two 50Ω on-chip termination resistors between DDI3 and $\overline{\text{DDI3}}$.
17, 18	DDI_SEL[1:0]	LOGIC INPUT	Serial digital input select.

DDI_SEL1	DDI_SEL0	INPUT SELECTED
0	0	DDI0
0	1	DDI1
1	0	DDI2
1	1	DDI3

19	BYPASS	LOGIC INPUT	Bypasses the reclocker stage (Active HIGH).
20	AUTOBYPASS	LOGIC INPUT	Automatically bypasses the reclocker stage when the PLL is not locked (active HIGH).
21	AUTO/$\overline{\text{MAN}}$	LOGIC INPUT	When set HIGH, the standard is automatically detected from the input data rate.
24, 25, 26	SS[2:0]	OUTPUTS	When AUTO/$\overline{\text{MAN}}$ is HIGH, SS[0:2] are outputs, displaying the data rate to which the PLL has locked. When AUTO/$\overline{\text{MAN}}$ is LOW, SS[0:2] are inputs, forcing the PLL to lock only to a selected data rate.

SS2	SS1	SS0	DATA RATE (Mb/s)
0	0	0	143
0	0	1	177
0	1	0	270
0	1	1	360
1	0	0	540

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
27	ASI/$\overline{177}$	LOGIC INPUT	When HIGH, disables 177Mb/s data rate in the AUTO data rate detection circuit. This prevents a FALSE LOCK to 177Mb/s when using DVB/ASI. When LOW, 177Mb/s LOCK is possible, however, if a 270Mb/s ASI signal is applied, the device could false lock to the 177MHz signal.
28	LD	OUTPUT	LOCK DETECT. HIGH when the PLL is locked.
29	RSVD	RESERVED	Do not connect.
33	SD	OUTPUT	Logic HIGH in SD Mode.
34	KBB	ANALOG INPUT	Controls the loop bandwidth of the PLL. Leave this pin floating for serial reclocking applications.
36	DDO_MUTE	LOGIC INPUT	Mutes the DDO/$\overline{DDO}$ outputs.
44, 46	$\overline{DDO}$, DDO	OUTPUT	Differential Serial Digital Outputs.
45	DDO_VTT	PASSIVE	Center tap of two 50Ω on-chip termination resistors between DDO and $\overline{DDO}$.
50, 51	XTAL_OUT+, XTAL_OUT-	OUTPUT	Differential buffered outputs of the reference oscillator.
52, 53	XTAL+, XTAL-	INPUT	Reference crystal input. Connect to the GO1535.
62, 63	LF+, LF-	PASSIVE	Loop filter capacitor connection. (C_{LF} = 47nF).
4, 8, 12,16, 32, 35, 37, 43, 49, 54, 64	GND	PASSIVE	Recommended connect to GND.
43	GND_DRV	PASSIVE	Recommended connect to GND.
55, 57	VCC	PASSIVE	Recommend connect to 3.3V.
22	VCC_VCO	POWER	Most positive power supply connection for the internal VCO section. Connect to 3.3V.
30	VCC_DIG	POWER	Most positive power supply connection for the internal glue logic. Connect to 3.3V.
41	VCC_INT	POWER	Most positive power supply connection. Connect to 3.3V.
47	VCC_DDO	POWER	Most positive power supply connection for the DDO/$\overline{DDO}$ output driver. Connect to 3.3V.
61	VCC_CP	POWER	Most positive power supply connection for the internal charge pump. Connect to 3.3V.
23	VEE_VCO	POWER	Most negative power supply connection for the internal VCO section. Connect to ground.
31	VEE_DIG	POWER	Most negative power supply connection for the internal glue logic. Connect to ground.
42	VEE_INT	POWER	Most negative power supply connection. Connect to ground.
48	VEE_DDO	POWER	Most negative power supply connection for the DDO/$\overline{DDO}$ output driver. Connect to ground.
60	VEE_CP	POWER	Most negative power supply connection for the internal charge pump. Connect to ground.
38, 39, 40, 56, 58, 59	RSVD	RESERVED	Do not Connect.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage	+3.6 V_{DC}
Input ESD Voltage	500V
Storage Temperature Range	-50°C< T_S < 125°C
Inputs	V_{CC} + 0.5V

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

V_{cc} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Test Levels
Supply Voltage	Operating Range	V_{CC}	3.135	3.3	3.465	V	3
Power Consumption	T_A=25°C		408	600	849	mW	5
Supply Current	T_A=25°C	I_{CC}	130	182	245	mA	1
Logic Inputs DDI_SEL[1:0], BYPASS, AUTOBYPASS, ASI/177, SDO_MUTE, AUTO/MAN	High	V_{IH}	2.0	-	-	V	3
	Low	V_{IL}	-	-	0.8	V	3
Logic Outputs LD		V_{OH}	3.2	-	-	V	1
		V_{OL}	-	-	0.6	V	1
Bi-Directional Pins SS[2:0], AUTO/MAN = 0 (Manual Mode)	High	V_{IH}	2.0	-	-	V	3
	Low	V_{IL}	-	-	0.8	V	3
Bi-Directional Pins SS[2:0], AUTO/MAN = 1 (AUTO Mode)	High	V_{OH}	2.6	-		V	1
	Low	V_{OL}	-	-	0.6	V	1
XTAL_OUT+, XTAL_OUT-	High	V_{OH}	-	V_{CC}	-	V	7
	Low	V_{OL}	-	V_{CC} - 0.285	-	V	7
Serial Input Voltage	Common mode	V_{DDI}	1.65 + (V_{SID}/2)	-	V_{CC} - (V_{SID}/2)	V	1

Table 2-2: DC Electrical Characteristics

V_{cc} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Test Levels
Output Voltage SDO, $\overline{SDO}$	Common mode	V_{SDO}	-	V_{CC} - $V_{OD}/2$	-	V	1

Test Levels

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

2.3 AC Electrical Characteristics

Table 2-3: 2.3 AC Electrical Characteristics

V_{cc} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Levels
Serial Input Data Rate			143	-	540	Mb/s	3
Serial Input Jitter Tolerance		Worst case modulation Eg. Square wave modulation 143, 270, 360 Mb/s	0.8	-	-	UI	1
PLL Lock Time - Asynchronous	t_{ALOCK}		-	5	10	ms	6,7
PLL Lock Time - Synchronous	t_{SLOCK}	C_{LF}=47nF	0.16	-	-	µs	6,7
Serial Output Rise/Fall Time (20% - 80%)	t_{rSDO}	50Ω load (on chip)	-	114	-	ps	6,7
	t_{fSDO}		-	106	-	ps	
Serial Input - Signal Swing	V_{SID}	50Ω load (on chip)	100	-	800	mV_{p-p}	1
Serial Output - Signal Swing	V_{OD}	Differential (across 100Ω).	1400	-	2000	mV_{p-p}	1

Table 2-3: 2.3 AC Electrical Characteristics

V_{cc} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Test Levels
Serial Output Jitter (additive)	t_{IJ}	KBB=Float, PRN, 2^{23}-1	143Mb/s	-	0.02	-	UI	1
			177Mbs	-	0.02	-	UI	1
			270Mb/s	-	0.02	0.09	UI	1
			360Mbs	-	0.03	-	UI	1
			540Mbs	-	0.03	0.09	UI	1
			BYPASS	-	0.06	0.13	UI	1
Loop Bandwidth	BW_{LOOP}	270 Mb/s KBB = FLOAT		-	520	-	KHz	6,7
		270 Mb/s KBB = GND		-	1000	-	KHz	6,7

Test Levels

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

2.4 Input/Output Circuits

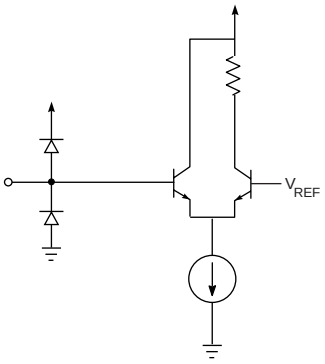


Figure 2-1: TTL Inputs

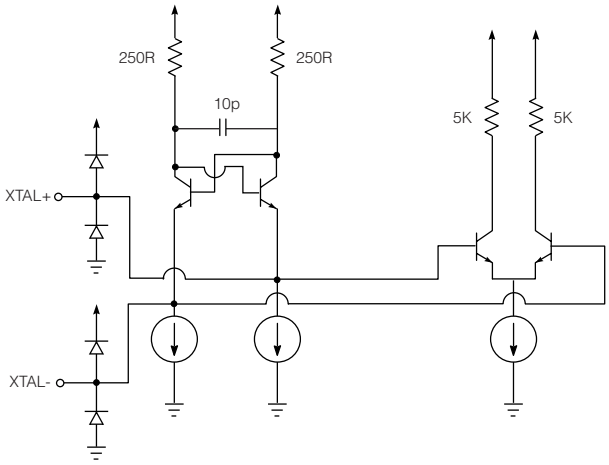


Figure 2-2: Crystal Input

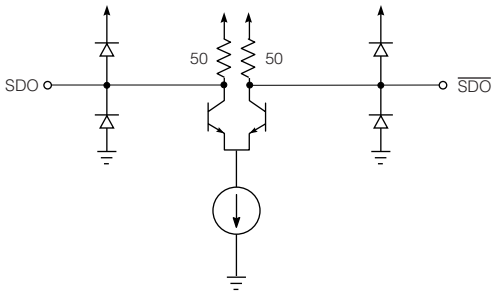


Figure 2-3: Serial Data Outputs

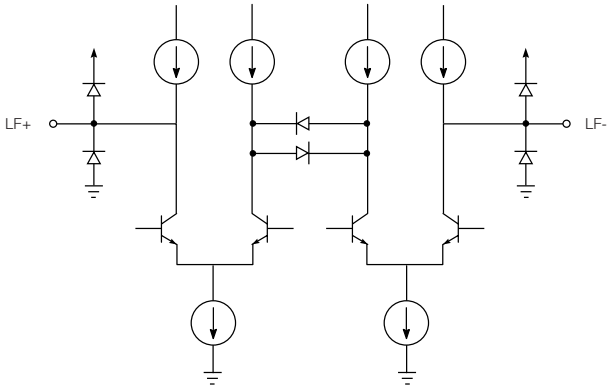


Figure 2-4: Loop Filter

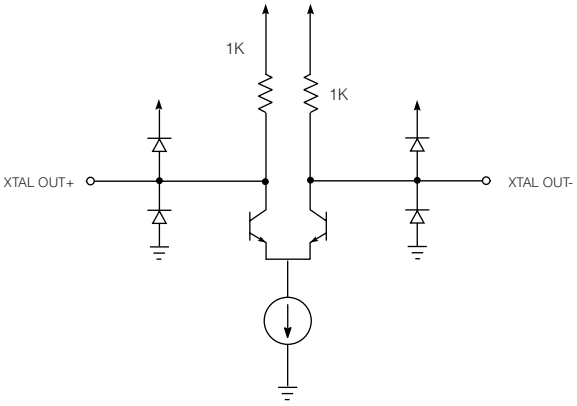


Figure 2-5: Crystal Ouput Buffer

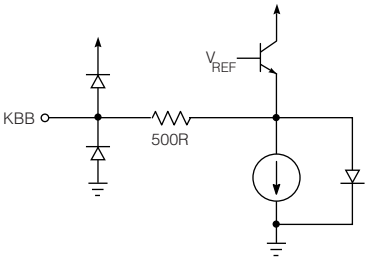


Figure 2-6: KBB

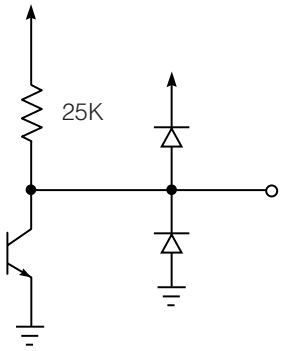


Figure 2-7: Outputs: LD, SD

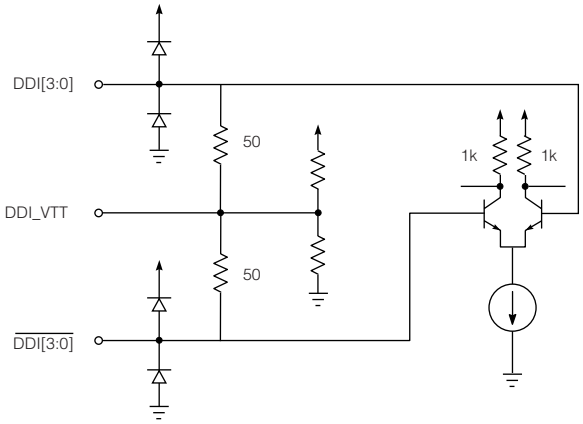


Figure 2-8: Serial Data Inputs

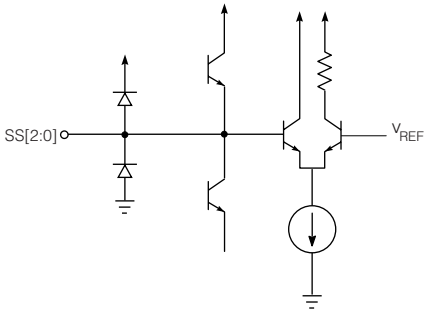


Figure 2-9: Standard Indication

3. Detailed Description

The GS9065 is a multi-standard retimer for serial digital SDTV signals at 143, 177, 270, 360 and 540 Mb/s.

3.1 Slew Rate Phase Lock Loop (S-PLL)

The term “slew” refers to the output phase of the PLL in response to a step change at the input. Linear PLLs have an output phase response characterized by an exponential response whereas an S-PLL’s output is a ramp response (See Figure 3-1). Because of this non-linear response characteristic, traditional small signal analysis is not possible with an S-PLL.

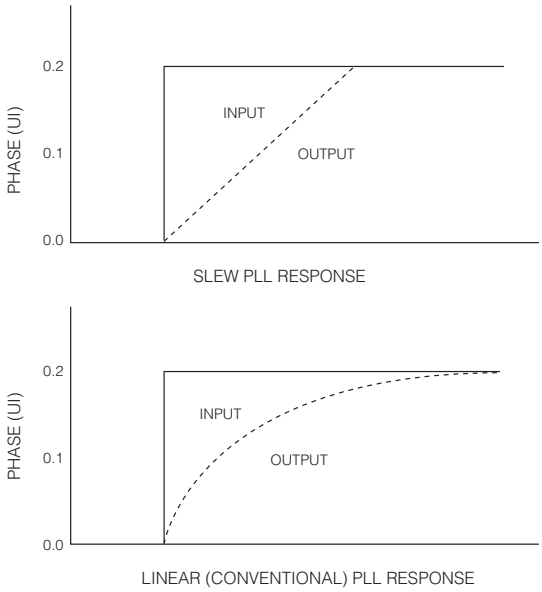


Figure 3-1: PLL Characteristics

The S-PLL offers several advantages over the linear PLL. The Loop Bandwidth of an S-PLL is independant of the transition density of the input data. Pseudo-random data has a transition density of 0.5 verses a pathological signal which has a transition density of 0.05. The loop bandwidth of a linear PLL will change proportionally with this change in transition density. With an S-PLL, the loop bandwidth is defined by the jitter at the data input. This translates to infinite loop bandwidth with a zero jitter input signal. This allows the loop to correct for small variations in the input jitter quickly, resulting in very low output jitter. The loop bandwidth of the GS9065’s PLL is defined at 0.2UI of input jitter.

The GS9065’s PLL consists of two acquisition loops. First is the Frequency Acquisiton (FA) loop. This loop is active when the device is not locked and is used to achieve lock to the supported data rates. Second is the phase acquisition (PA) loop. Once locked, the PA loop tracks the incomming data and makes phased corrections to produce a re-clocked output.

3.2 VCO

The internal VCO of the GS9065 is a ring oscillator. It is trimmed at the time of manufacture to capture all SD and HD data rates over temperature, and operation voltage ranges.

Integrated into the VCO is a series of programmable dividers, to achieve all serial data rates, as well as additional dividers for the frequency acquisition loop.

3.3 Charge Pump

A common charge pump is used for for the GS9065's PLL.

During frequency acquisition, the charge pump has two states, "pump-up" and "pump-down" which is produced by a leading or lagging phase difference between the input and the VCO frequency.

During phase acquisition, there are two levels of "pump-up" and two levels of "pump down" produced for leading and lagging phase difference between the input and VCO frequency. This is to allow for greater precision of VCO control.

The charge pump produces these signals by holding the integrated frequency information on the external loop-filter capacitor, C_{LF}. The instantaneous frequency information is the result of the current flowing through an internal resistor connected to the loop-filter capacitor.

3.4 Frequency Acquisition Loop — The Phase-Frequency Detector

An external crystal of 14.140 MHz is used as a reference to keep the VCO centered at the last known data rate. This allows the GS9065 to achieve a fast synchronous lock, especially in cases where a known data rate is interrupted. The crystal reference is also used to clock internal timers and counters. To keep the optimal performance of the reclocker over all operating conditions, the crystal frequency must be 14.140 MHz, +/-50ppm. The GO1535 meets this specification and is available from GENNUM.

The VCO is divided by a selected ratio which is dependant on the input data rate. The resultant is then compared to the crystal frequency. If the divided VCO frequency and the crystal frequency are within 1% of each other, the PLL is considered to be locked to the input data rate.

3.5 Phase Acquisition Loop — The Phase Detector

The phase detector is a digital quadrature phase detector. It indicates whether the input data is leading or lagging with respect to a clock that is in phase with the VCO (I-clk) and a quadrature clock (Q-clk). When the phase acquisition loop (PA loop) is locked, the input data transition is aligned to the falling edge of I-clk and the output data is re-timed on the rising edge of I-clk. During high input jitter conditions (>0.25UI), Q-clk will sample a different value than I-clk. In this condition, two extra phase correction signals will be generated which instructs the charge pump to create larger frequency corrections for the VCO.

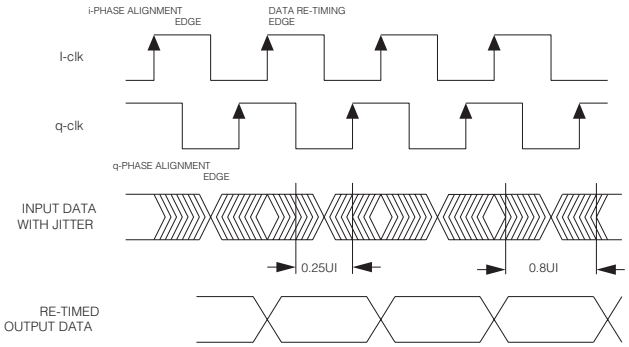


Figure 3-2: Phase Detector Characteristics.

When the PA loop is active, the crystal frequency and the incomming data rate are compared. If the resultant is more that 2%, the PLL is considered to be unlocked and the system jumps to the FA loop.

3.6 4:1 Input Mux

The 4:1 input mux allows the connection of four independent streams of video/data. These are differential inputs (DDI[3:0] and $\overline{\text{DDI[3:0]}}$). The active channel can be selected via the DDI_SEL[1:0] pins. Table 3-1 shows the input selected for a given state at DDI_SEL[1:0].

Table 3-1: Bit Pattern for Input Select

DDI_SEL1:0]	Selected Input
00	DDI0
01	DDI1
10	DDI2
11	DDI3

The DDI inputs are designed to be DC interfaced with the output of the GS1524 Cable Equalizer. There are on chip 50Ω termination resistors which come to a common point at the DDI_VT pins. Connect a 10nF capacitor to this pin and connect the other end of the capacitor to ground. This end-terminates the transmission line at the inputs for optimum performance.

If only one input pair is used, connect the unused positive inputs to +3.3V and leave the unused negative inputs floating. This helps to eliminate crosstalk from potential noise that would couple to the unused input pair.

3.7 Automatic And Manual Data Rate Selection

The GS9065 can be configured to manually lock to a specific data rate or automatically search for and lock to the incoming data rate. The AUTO/$\overline{\text{MAN}}$ pin selects Automatic data rate detection mode (AUTO mode) when HIGH and manual data rate selection mode (MANUAL mode) when LOW.

In AUTO mode, the SS[2:0] bi-directional pins become outputs and the bit pattern indicates the data rate that the PLL is locked to (or previously locked to). The "search algorithm" cycles through the data rates (see Figure 3-3) and starts over if that data rate is not found.

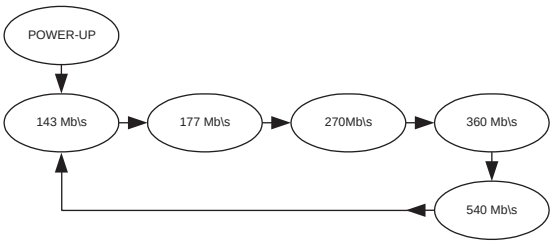


Figure 3-3: Data Rate Search Pattern

Table 3-2: Data Rate Indication Bit Pattern.

SS[2:0]	Data Rate (Mb/s)
000	143
001	177
010	270
011	360
100	540

In MANUAL mode, the SS[2:0] pins become inputs and the data rate can be programmed. In this mode, the search algorithm is disabled and the GS9065's PLL will only lock to this data rate.

3.8 Bypass Mode

In bypass mode, the GS9065 passes the data at the inputs, directly to the outputs.

The BYPASS pin is an active high signal which forces the GS9065 into bypass mode for as long as a HIGH is asserted at this pin.

The AUTOBYPASS pin is an active high signal which places the GS9065 into bypass mode only when the PLL has not locked to a data rate. Note that if BYPASS is HIGH, this will overwrite the AUTOBYPASS functionallity.

3.9 DVB/ASI Operation

The GS9065 is designed to re-clock DVB/ASI at 270 Mb/s. There is a harmonic present in idle patterns (K28.5) which is very close the 177 Mb/s data rate (EIC 1179). The ASI/$\overline{177}$ pin, when HIGH will disable the 177 Mb/s search in AUTO mode. In this mode, the GS9065 will not lock to 177 Mb/s.

3.10 Lock

The LOCK DETECT signal, LD, is an active high output which indicates when the PLL is locked.

The lock logic with the GS9065 includes a system which monitors the Frequency Acquisition Loop and the Phase Acquisition Loop as well as a monitor to detect harmonic lock.

3.11 Output Drivers

The GS9065's serial digital data outputs (DDO/$\overline{\text{DDO}}$) have a nominal voltage of 800mv single ended or 1600mV differential when terminated into 50Ω.

The DDO_VTT pin is the common point of two 50Ω termination resistors from the DDO and $\overline{\text{DDO}}$. This pin can be left open if the termination exists on the receiving device.

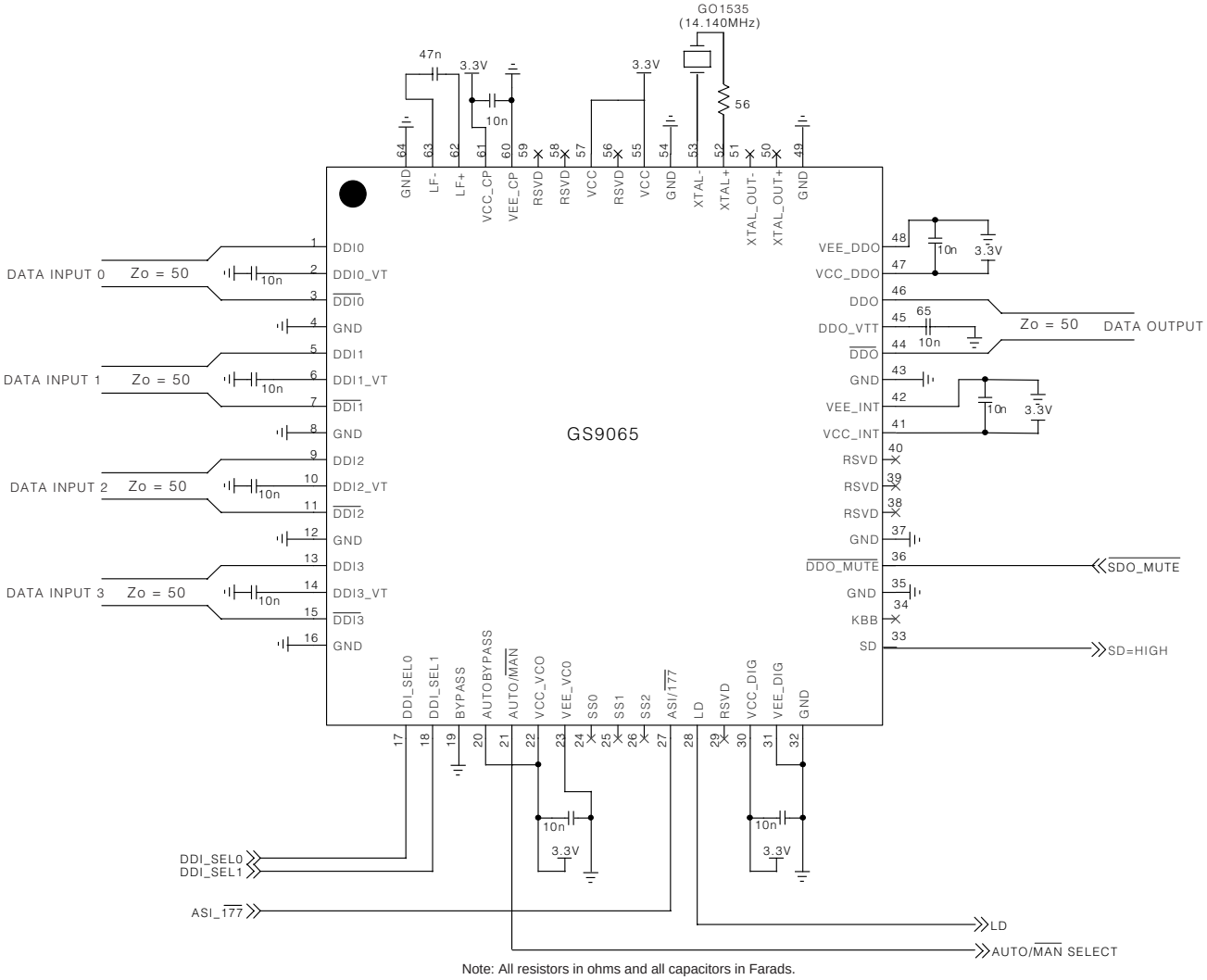
3.12 Output Mute

The $\overline{\text{DDO\_MUTE}}$ pin is provided to allow muting of the retimed output.

When the GS9065's PLL is locked and the device is reclocking, setting $\overline{\text{DDO\_MUTE}}$ = LOW will force the serial digital outputs DDO/$\overline{\text{DDO}}$ to mute. However, if the GS9065 is in bypass mode, (BYPASS = HIGH), $\overline{\text{DDO\_MUTE}}$ will have no effect on the output.

4. Application Reference Design

4.1 Typical Application Circuit



Note: All resistors in ohms and all capacitors in Farads.

5. References

Compliant with SMPTE 259M and SMPTE344M.

6. Package & Ordering Information

6.1 Package Dimensions

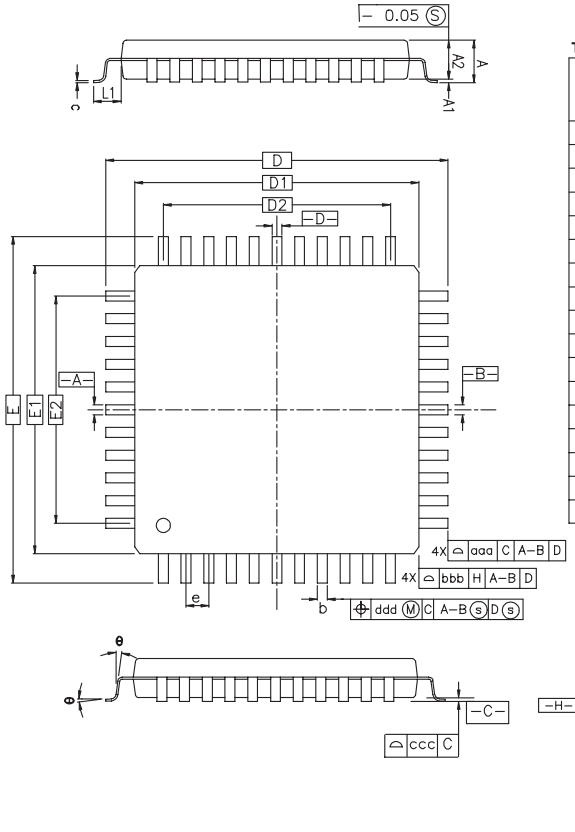


Table X

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D		12.00 BSC.			0.472 BSC.	
D_1		10.00 BSC.			0.393 BSC.	
E		12.00 BSC.			0.472 BSC.	
E_1		10.00 BSC.			0.393 BSC.	
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1		1.00 REF			0.039 REF	
S	0.20	—	—	0.008	—	—

CONTROL DIMENSIONS ARE IN MILLIMETERS.

NOTE:
Diagram shown is representative only.
Table X is fixed for all pin sizes, and
Table Y is specific to the 64-pin package.

Table Y

SYMBOL	64L					
	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.020 BSC		
D2	7.50			0.295		
E2	7.50			0.295		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		

6.2 Packaging Data

Parameter	Value
Package Type	10mm x 10mm 64-pin LQFP
Package Drawing Reference	JEDEC MS026
Moisture Saturation Level	3
Junction to Case Thermal Resistance, θ_{j-c}	14.9°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	45.4°C/W
Psi	0.9°C/W
Pb-free and Green	Yes

6.3 Ordering Information

Part Number	Packages	Temperature Ranges	Pb-Free and Green
GS9065-CFU	64 pin LQFP	0°C to 70°C	No
GS9065-CFUE3	64 pin LQFP	0°C to 70°C	Yes

7. Revision History

Version	ECR	Date	Changes and / or Modifications
6	134678	November 2004	Corrected TAC pins 50, 51 to conform with Pinout diagram. Added packaging data section. Converted to new document template.

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION
DATA SHEET
The product is in a development phase and specifications are subject to change without notice. Gennum reserves the right to remove the product at any time. Listing the product does not constitute an offer for sale.

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