

MAX14883E

CAN Transceiver with $\pm 60V$ Fault Protection and Selectable Polarity

General Description

The MAX14883E fault-protected, high-speed Control Area Network (CAN) transceiver is optimized for industrial network applications. This device features $\pm 60V$ fault protection, a $\pm 25V$ functional common mode input range, and high $\pm 10kV$ ESD protection (contact discharge) on the CANH and CANL bus. The device operates from a single 5V supply (V_{CC}) and includes a logic-level supply input (V_L) for interfacing with 1.8V to 5V logic.

The MAX14883E features a polarity selection input (POL) that swaps the CANH and CANL I/Os, allowing for software correction of cross-wired field cables.

The MAX14883E operates at the maximum CAN high-speed data rate, allowing up to 1Mbps on small networks. The maximum speed on large networks may be limited by capacitive loading and other factors.

The transceiver includes a transmitter dominant timeout (t_{DOM}) to prevent bus lockup caused by controller error or by a fault on the TXD input. When TXD remains in the dominant state (low) for longer than t_{DOM} , the driver is switched to the recessive state, releasing the bus.

The MAX14883E is available in a narrow, 8-pin SOIC package and operates over the $-40^{\circ}C$ to $+125^{\circ}C$ temperature range.

Benefits and Features

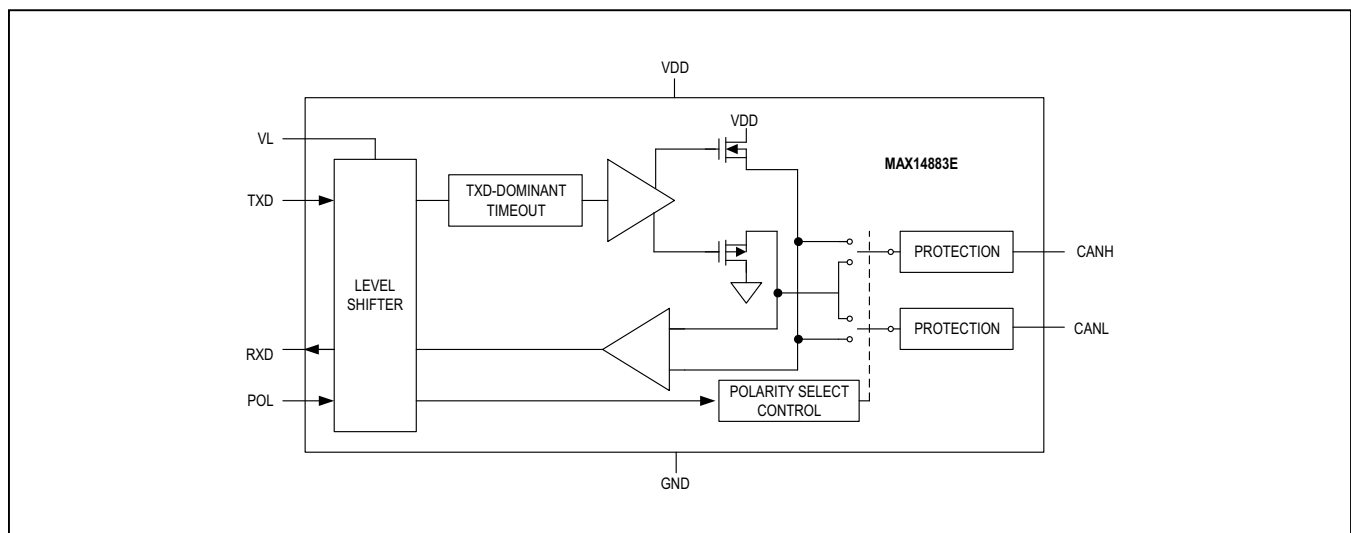
- Integrated Protection for Robust Communication
 - $\pm 60V$ Fault Tolerant CANH and CANL
 - High ESD Protection on CANH and CANL
 - $\pm 22kV$ Human Body Model
 - $\pm 15kV$ IEC 61000-4-2 Air Gap
 - $\pm 10kV$ IEC 61000-4-2 Contact Discharge
- Flexible Logic Interface Simplifies Designs
 - 1.71V to 5.5V Logic-Supply (V_L) Range
- High Integration Allows Simplified Network Configuration
 - Polarity Control
 - Dominant Timeout Protection
 - Capable of Data Rates Up to 1Mbps

Applications

- Industrial Controls
- Building Automation
- HVAC
- Switch Gear

Ordering Information appears at end of data sheet.

Simplified Block Diagram



Absolute Maximum Ratings

(All voltages referenced to GND, unless otherwise noted)

V _{DD}	-0.3V to +6V
CANH or CANL (Continuous).....	-63V to +63V
TXD, POL.....	-0.3V to 6V
V _L	-0.3V to (V _{DD} + 0.5V)
RXD.....	-0.3V to V _L + 0.3V

Continuous Power Dissipation

Single-Layer Board (T _A = +70°C, derate 5.9mW/°C above +70°C.)	470.6mW
Multilayer Board (T _A = +70°C, derate 7.6mW/°C above +70°C.)	606.1mW
Operating Temperature Range.....	-40°C to 125°C
Junction Temperature.....	+150°C
Storage Temperature Range.....	-60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow).....	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

8 SOIC

PACKAGE CODE	S8+4
Outline Number	21-0041
Land Pattern Number	90-0096
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ _{JA})	170
Junction to Case (θ _{JC})	40
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ _{JA})	132
Junction to Case (θ _{JC})	38

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

DC Electrical Characteristics

($V_{DD} = 4.5V$ to $5.5V$, $V_L = 1.71V$ to V_{DD} , $R_L = 60\Omega$, $C_L = 15pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{DD} = 5V$, $V_L = 3.3V$, and $T_A = +25^\circ C$, unless otherwise specified. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER							
Power Supply Input	V_{DD}			4.5		5.5	V
Logic-Level Voltage Supply Input	V_L			1.71		V_{DD}	V
Supply Current	I_{DD}	$V_{DD} = 5V$, TXD = low	No load		4.3	6.9	mA
			$R_L = 60\Omega$		47.6	66.8	
		$V_{DD} = 5V$, TXD = high	No load		3.2		
			CANH shorted to CANL		3.2		
Logic-Level Supply Current	I_L	No load on RXD	$V_L = 5V$		42	65	μA
			$V_L = 3.3V$		26		
			$V_L = 1.8V$		14		
V_{DD} UVLO Threshold	V_{UVLO_R}	V_{DD} rising				4.25	V
	V_{UVLO_F}	V_{DD} falling				3.45	
LOGIC INTERFACE (RXD, TXD, POL)							
Input High Voltage	V_{IH}			$0.7 \times V_L$			V
Input Low Voltage	V_{IL}	$2.25V \leq V_L \leq 5.5V$				0.8	V
		$1.71 \leq V_L < 2.25V$				0.6	
Output High Voltage	V_{OH}	$I_{SOURCE} = 4mA$		$V_L - 0.4$			V
Output Low Voltage	V_{OL}	$I_{SINK} = 4mA$				0.4	V
TXD Input Pullup Resistance	R_{PU_TXD}			100		250	k Ω
POL Input Pulldown Resistance	R_{PD_POL}			100		250	k Ω
Input Capacitance					5		pF
CAN BUS DRIVER							
Single-Ended Voltage Output (Dominant State)	V_{OD}	TXD = low, $R_L = 60\Omega$	CANH	2.75		4.5	V
			CANL	0.5		2.25	
Differential Voltage Output (Dominant State)	V_{DIFF}	TXD = low, $R_L = 60\Omega$	$R_{CM} = 156\Omega$, $-5V \leq V_{CM} \leq +10V$, Figure 1	1.5		3.0	V
			R_{CM} is open	1.5		3.0	
Single-Ended Voltage Output (Recessive State)	V_{OR}	TXD = high, no load	CANH	2		3	V
			CANL	2		3	
Differential Voltage Output (Recessive State)	V_{ODR}	TXD = high	$R_L = 60\Omega$	-120		12	mV
			No load	-500		+50	

DC Electrical Characteristics (continued)

($V_{DD} = 4.5V$ to $5.5V$, $V_L = 1.71V$ to V_{DD} , $R_L = 60\Omega$, $C_L = 15pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{DD} = 5V$, $V_L = 3.3V$, and $T_A = +25^\circ C$, unless otherwise specified. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
High-Side Short-Circuit Current	I_{SC_H}	TXD = low	POL = low, CANH is shorted to GND		178.5	245	mA
			POL = high, CANL is shorted to GND		178.5	245	
Low-Side Short-Circuit Current	I_{SC_L}	TXD = low	POL = low, CANL is shorted to V_{DD}		179.5	235	mA
			POL = high, CANH is shorted to V_{DD}		179.5	235	
RECEIVER (TXD = High, CANH and CANL Externally Driven)							
Common Mode Input Range		CANH or CANL to GND, RXD output valid		-25		+25	V
Differential Input Voltage Threshold (Recessive)	V_{DIFF_R}	TXD = high		0.5			V
Differential Input Voltage Threshold (Dominant)	V_{DIFF_D}	TXD = high				0.9	V
Differential Input Hysteresis	$V_{DIFF(HYST)}$				130		mV
CANH and CANL Input Resistance	R_{IN}	TXD = high		10		50	k Ω
Differential Input Resistance	R_{DIFF}	TXD = high		20		100	k Ω
Input Leakage Current	I_{LKG}	$V_{DD} = V_L = 0V$, $V_{CAN_} = 5V$				310	μA
Input Capacitance	C_{IN}	CANH or CANL to GND (Note 2)			62	110	pF
Differential Input Capacitance	C_{IN_DIFF}	CANH to CANL (Note 2)			31	55	pF
PROTECTION							
ESD Protection (CANH, CANL to GND)		IEC 61000-4-2 Air Gap Discharge			± 15		kV
		IEC 61000-4-2 Contact Discharge			± 10		
		Human Body Model			± 22		
ESD Protection (All Other Pins)		Human Body Model			± 4		kV
		Machine Model			± 400		V
Fault Protection Range	V_{FAULT}	CANH or CANL to GND		-60		+60	V
Thermal Shutdown	T_{SHDN}	Junction temperature rising			160		$^\circ C$
Thermal Shutdown Hysteresis	T_{HYST}				20		$^\circ C$

AC Electrical Characteristics—Switching

($V_{DD} = 4.5V$ to $5.5V$, $V_L = 1.71V$ to $5.5V$, $R_L = 60\Omega$, $C_L = 15pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise specified. Typical values are at $V_{DD} = 5V$, $V_L = 3.3V$, and $T_A = +25^\circ C$, unless otherwise specified. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Rise Time	t_R	$R_L = 60\Omega$, $C_L = 100pF$, R_{CM} is open, Figure 1			20	ns
Driver Fall Time	t_F	$R_L = 60\Omega$, $C_L = 100pF$, R_{CM} is open, Figure 1			33	ns
TXD to RXD Loop Delay	t_{LOOP}	$R_L = 60\Omega$, Dominant to Recessive and Recessive to Dominant, Figure 2			300	ns
TXD Propagation Delay (Recessive to Dominant)	t_{ONTXD}	$R_L = 60\Omega$, $C_L = 100pF$, R_{CM} is open, Figure 1			90	ns
TXD Propagation Delay (Dominant to Recessive)	t_{OFFTXD}	$R_L = 60\Omega$, $C_L = 100pF$, R_{CM} is open, Figure 1			90	ns
RXD Propagation Delay (Recessive to Dominant)	t_{ONRXD}	$C_L = 15pF$, Figure 3			210	ns
RXD Propagation Delay (Dominant to Recessive)	t_{OFFRXD}	$C_L = 15pF$, Figure 3			210	ns
TXD-Dominant TimeOut	t_{DOM}	Figure 4	1.3		4.3	ms

Note 1: All units are 100% production tested at $T_A = +25^\circ C$. Specifications over temperature are guaranteed by design.

Note 2: Not production tested. Guaranteed at $T_A = 25^\circ C$.

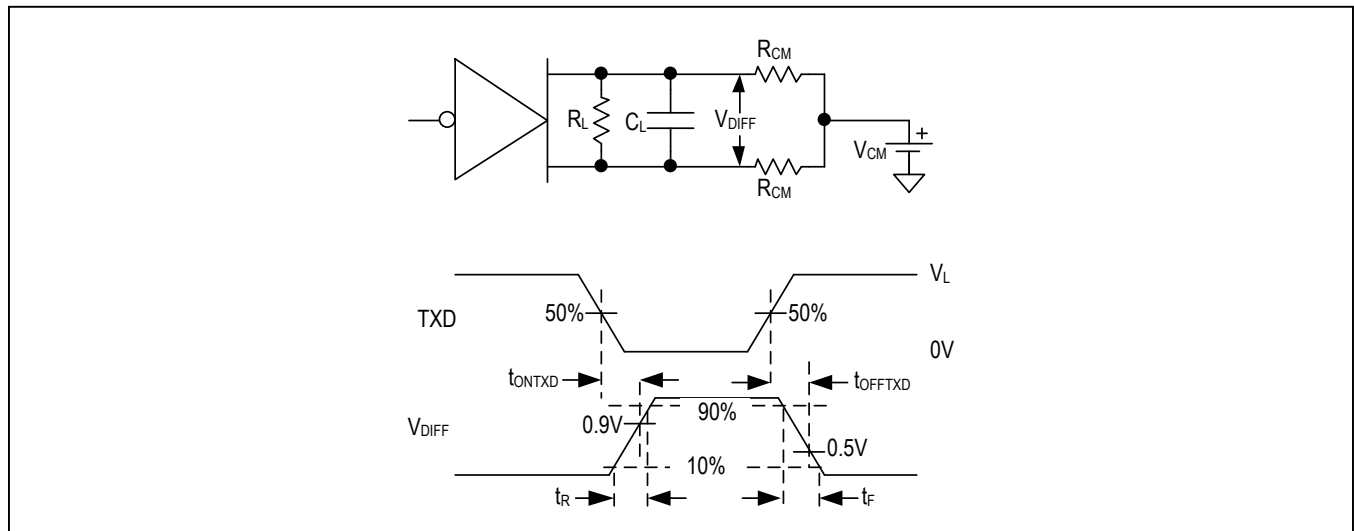


Figure 1. Transmitter Test Circuit and Timing Diagram

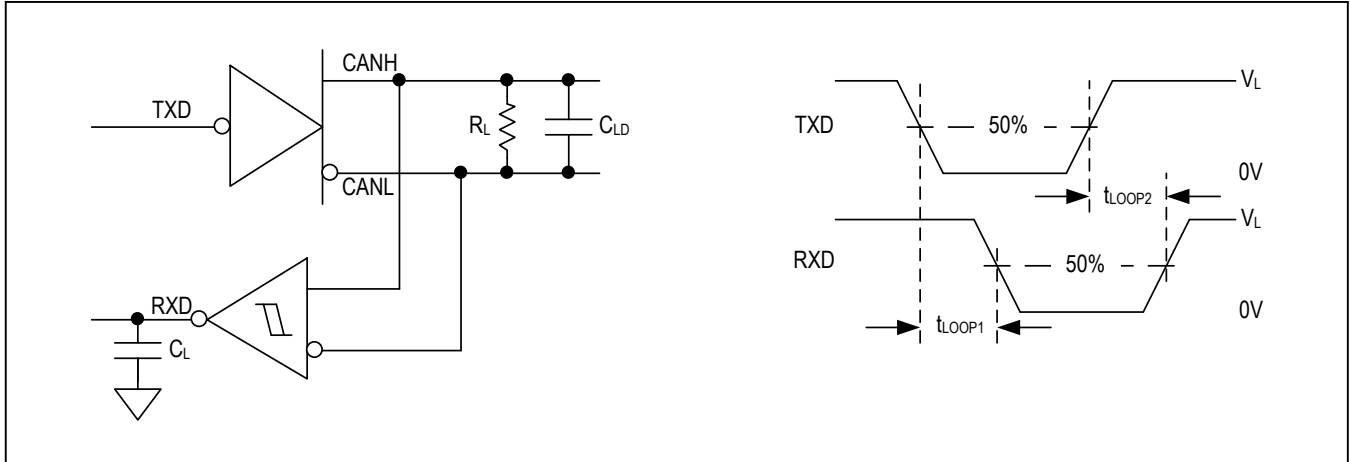


Figure 2. TXD to RXD Loop Delay

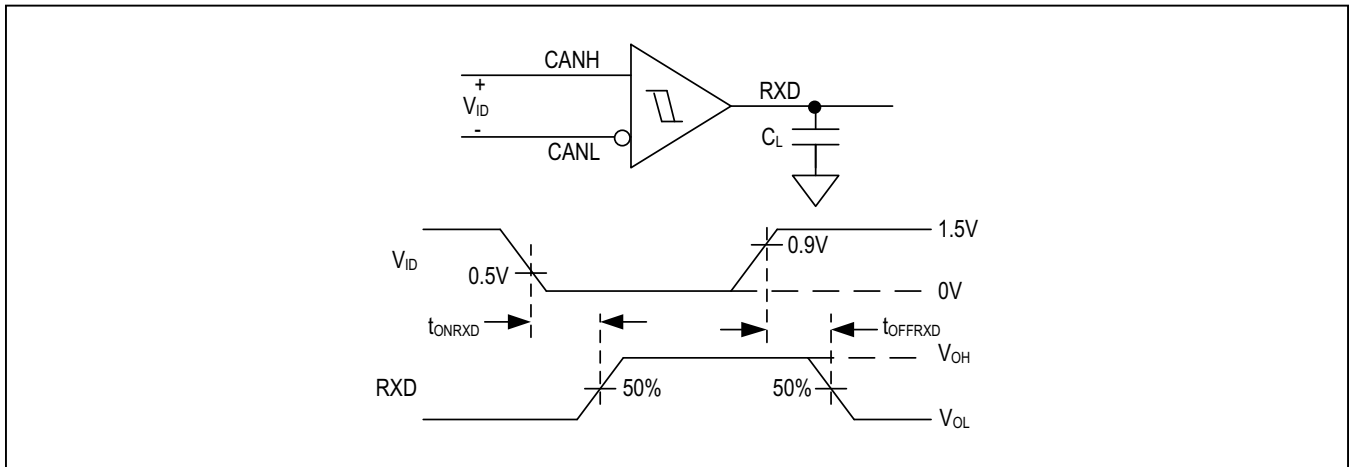


Figure 3. RXD Timing Diagram

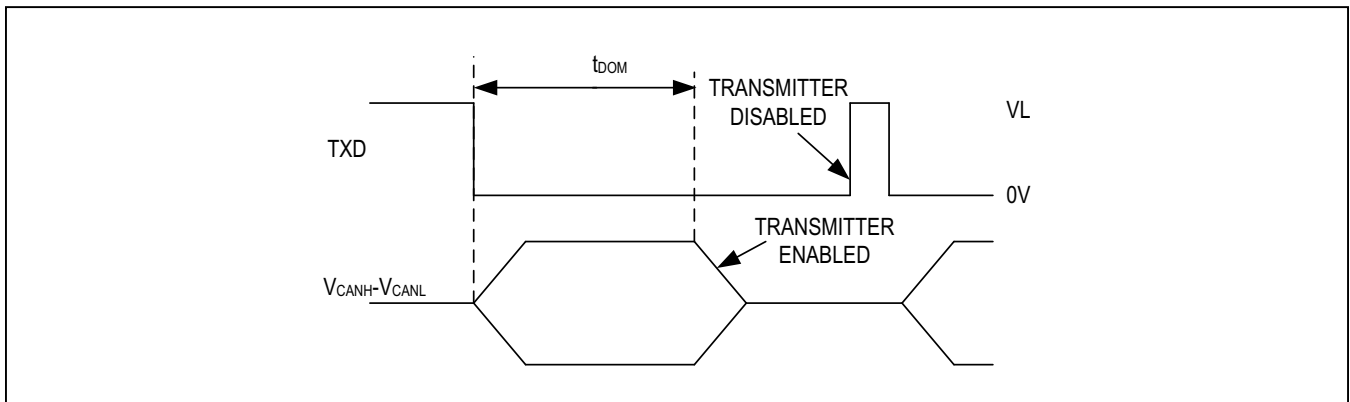
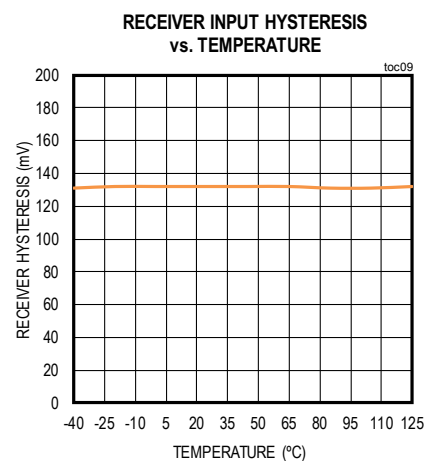
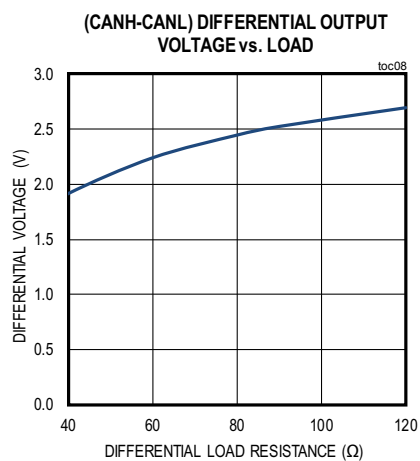
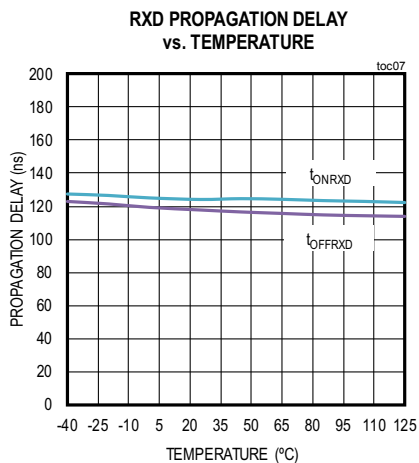
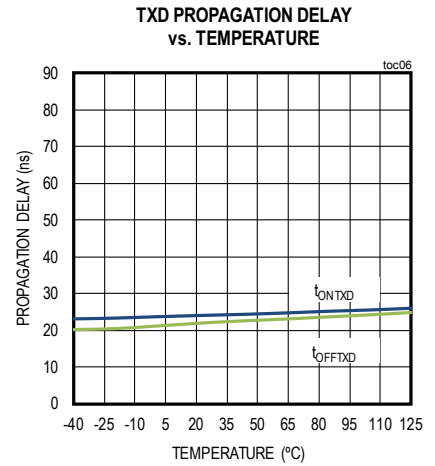
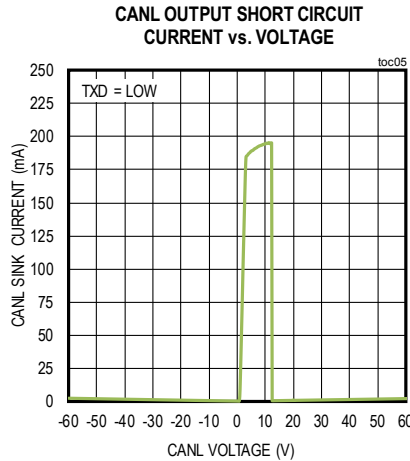
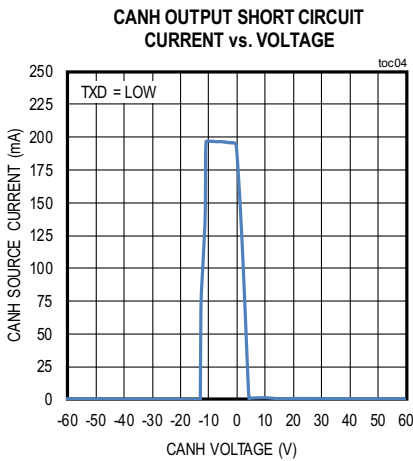
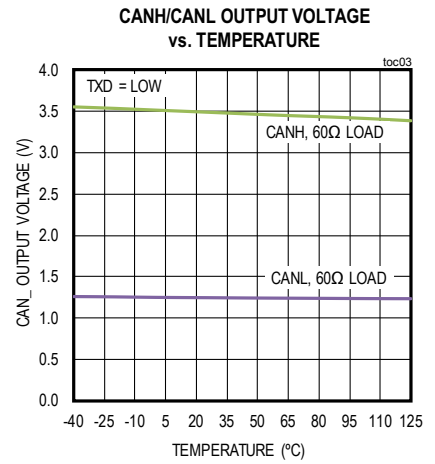
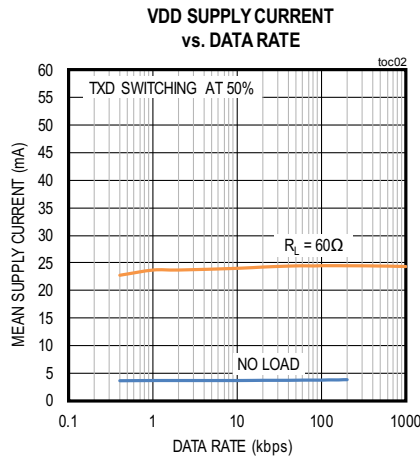
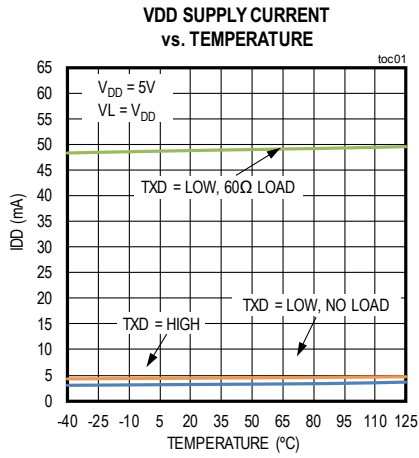


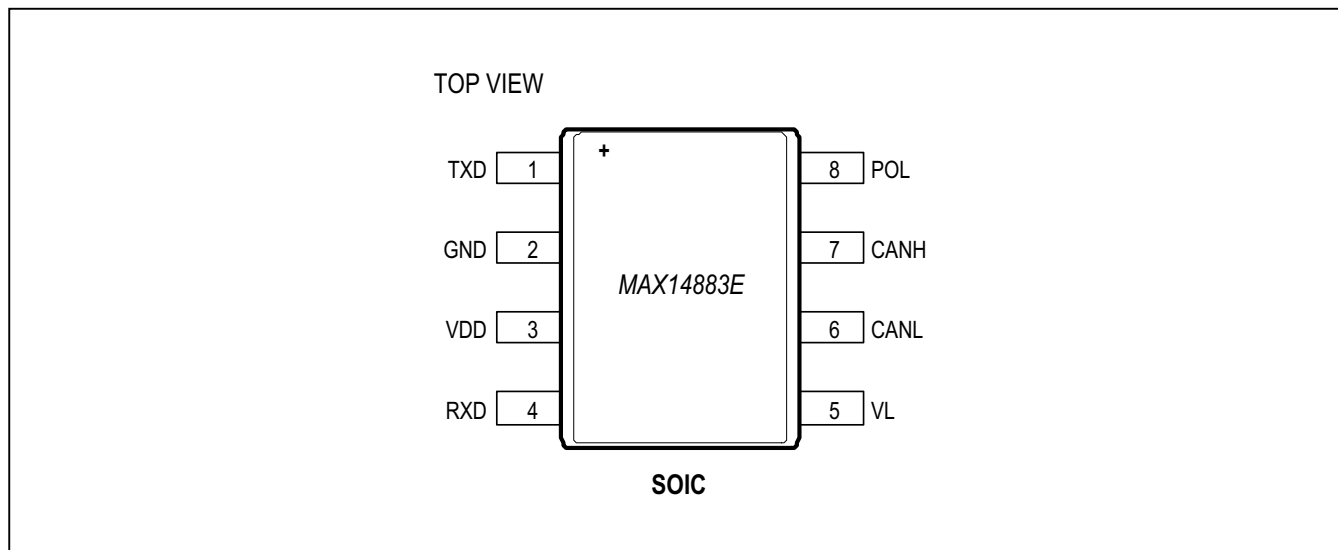
Figure 4. Transmitter-Dominant Timeout Timing Diagram

Typical Operating Characteristics

($V_{DD} = 5V$, $V_L = 3.3V$, 60Ω load between CANH and CANL, $T_A = 25^\circ C$, unless otherwise noted.)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	TXD	Transmit Data Input. Drive TXD high to set the driver in the recessive state. Drive TXD low to set the driver in the dominant state. TXD has an internal pullup to V_L .
2	GND	Ground.
3	V_{DD}	Power Supply Input. Bypass V_{DD} to GND with a $0.1\mu F$ capacitor as close to the device as possible.
4	RXD	Receive Data Output. RXD is high when CANH and CANL are in the recessive state. RXD is low when CANH and CANL are in the dominant state. RXD is referenced to V_L .
5	V_L	Logic-Level Voltage Supply Input. Bypass V_L to GND with a $0.1\mu F$ capacitor as close to the device as possible.
6	CANL	CAN Bus Line Low. CANL is the low-side input/output of the receiver/driver. Drive POL high to set CANL as the high-side input/output of the receiver/driver.
7	CANH	CAN Bus Line High. CANH is the high-side input/output of the differential receiver/driver. Drive POL high to set CANH as the low-side input/output.
8	POL	Polarity Select Input. Drive POL low for normal CANH/CANL operation. Drive POL high to switch CANH/CANL operation. POL does not change the dominant and recessive states of TXD and RXD. POL has an internal $100k\Omega$ (min) pulldown to GND.

Detailed Description

The MAX14883E fault-protected CAN transceiver is optimized for industrial network applications and operates from a 5V supply. The MAX14883E features a $\pm 25V$ common mode input range and is protected against shorts up to $\pm 60V$ on the CAN bus (CANH, CANL), making it ideal for operating in harsh industrial environments.

The MAX14883E operates at the maximum high-speed CAN data rate, allowing up to 1Mbps on small networks. The maximum speed on large networks may be limited by capacitive loading and other factors. Networks of up to 17 MAX14883E transceivers can operate up to 1Mbps. Larger networks of up to 120 MAX14883E transceivers can operate up to data rates of 125kbps.

CANH and CANL outputs are short-circuit current-limited and are protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs in a high-impedance state.

Transmitter

The transmitter converts a single-ended input signal (TXD) from the CAN controller to differential outputs for the bus lines (CANH, CANL). The truth table for the transmitter and receiver is given in [Table 1](#).

Transmitter-Dominant Timeout

The MAX14883E features a transmitter dominant timeout (t_{DOM}) that prevents erroneous CAN controllers from clamping the bus to a dominant level by maintaining a continuous low TXD signal. When TXD remains in the dominant state (low) for greater than t_{DOM} , the transmitter is disabled, releasing the bus to a recessive state ([Figure 4](#)). After a dominant timeout fault, the transmitter is re-enabled when receiving a rising edge at TXD. The transmitter dominant timeout limits the minimum possible data rate to 9kbps for standard CAN protocol.

Driver Output Protection

The MAX14883E protects the transmitter output stage against a short-circuit to a positive or negative voltage by limiting the driver current. Thermal shutdown further protects the MAX14883E from excessive temperatures that may result from a short. The transmitter returns to normal operation once the short is removed.

Receiver

The receiver reads the differential input from the bus (CANH, CANL) and transfers this data as a single-ended output (RXD) to the CAN controller. It consists of a comparator that senses the difference $V_{DIFF} = (CANH - CANL)$, with respect to an internal threshold of 0.7V. If $V_{DIFF} > 0.9V$, a logic-low is present on RXD. If $V_{DIFF} < 0.5V$, a logic-high is present.

The CANH and CANL common-mode range is $\pm 25V$. RXD is logic-high when CANH and CANL are shorted or terminated and undriven.

Polarity Selection

A polarity select input (POL) switches the state of the CANH and CANL drivers. Polarity selection allows for software correction of cross-wired field cables, ensuring that the transmitter continues to operate correctly in the field. See [Table 1](#) for detailed operation.

Thermal Shutdown

If the junction exceeds $+160^{\circ}C$ (typ), the device is switched off. During thermal shutdown, CANH and CANL are high-impedance and all IC functions are disabled. The transmitter outputs are re-enabled and the device resumes normal operation when the junction temperature drops below $145^{\circ}C$ (typ).

Table 1. Transmitter and Receiver Truth Table (When Not Connected to the Bus)

POL	TXD	TXD LOW TIME	CANH	CANL	BUS STATE	RXD
LOW	LOW	$< t_{DOM}$	HIGH	LOW	DOMINANT	LOW
LOW	LOW	$> t_{DOM}$	$V_{DD}/2$	$V_{DD}/2$	RECESSIVE	HIGH
LOW	HIGH	X	$V_{DD}/2$	$V_{DD}/2$	RECESSIVE	HIGH
HIGH	LOW	$< t_{DOM}$	LOW	HIGH	DOMINANT	LOW
HIGH	LOW	$> t_{DOM}$	$V_{DD}/2$	$V_{DD}/2$	RECESSIVE	HIGH
HIGH	HIGH	X	$V_{DD}/2$	$V_{DD}/2$	RECESSIVE	HIGH

Applications Information

Reduced EMI and Reflections

In multidrop CAN applications, it is important to maintain a single linear bus of uniform impedance that is properly terminated at each end. See [Figure 5](#) for an example network. A star configuration should never be used. Any

deviation from the end-to-end wiring scheme creates a stub. High-speed data edges on a stub can create reflections back down the bus. These reflections can cause data errors by eroding the noise margin of the system.

Although stubs are unavoidable in a multidrop system, care should be taken to keep these stubs as small as possible, especially when operating with high data rates.

Typical Application Circuits

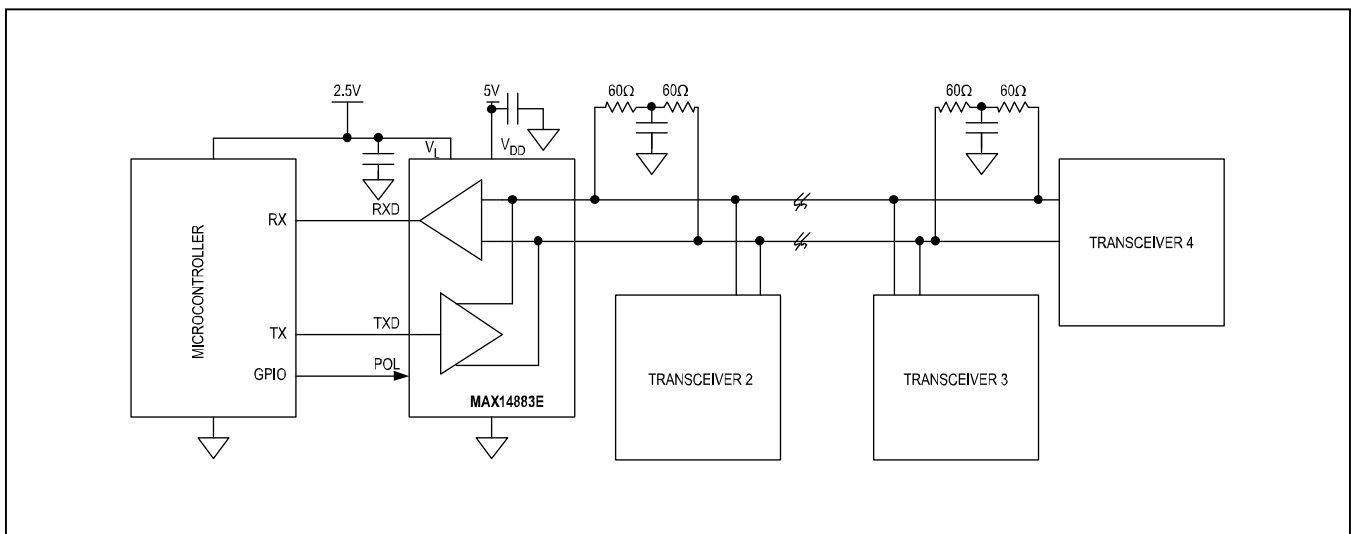


Figure 5. Multidrop CAN Bus

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14883EASA+	-40°C to +125°C	8 SOIC
MAX14883EASA+T	-40°C to +125°C	8 SOIC

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/16	Initial release	—

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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