To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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R1LP0408C-I Series

Wide Temperature Range Version
4M SRAM (512-kword × 8-bit)

REJ03C0067-0200Z
Rev. 2.00
May.26.2004

Description

The R1LP0408C-I is a 4-Mbit static RAM organized 512-kword × 8-bit. R1LP0408C-I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). The R1LP0408C-I Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has packaged in 32-pin SOP, 32-pin TSOP II.

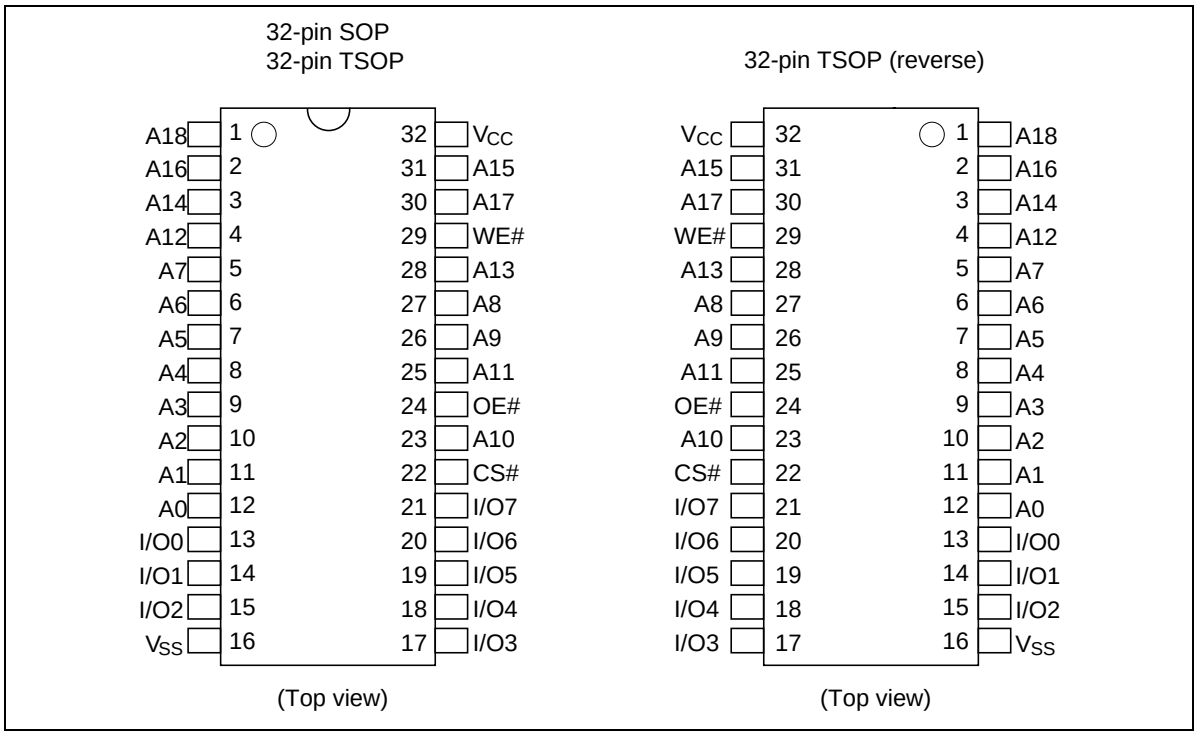
Features

- Single 5 V supply: 5 V ± 10%
- Access time: 55/70 ns (max)
- Power dissipation:
  - Active: 10 mW/MHz (typ)
  - Standby: 4 µW (typ)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Directly TTL compatible.
  - All inputs and outputs
- Battery backup operation.
- Operating temperature: –40 to +85°C

Ordering Information

Type No.	Access time	Package
R1LP0408CSP-5SI	55 ns	525-mil 32-pin plastic SOP (32P2M-A)
R1LP0408CSP-7LI	70 ns	
R1LP0408CSB-5SI	55 ns	400-mil 32-pin plastic TSOP II (32P3Y-H)
R1LP0408CSB-7LI	70 ns	
R1LP0408CSC-5SI	55 ns	400-mil 32-pin plastic TSOP II reverse (32P3Y-J)
R1LP0408CSC-7LI	70 ns	

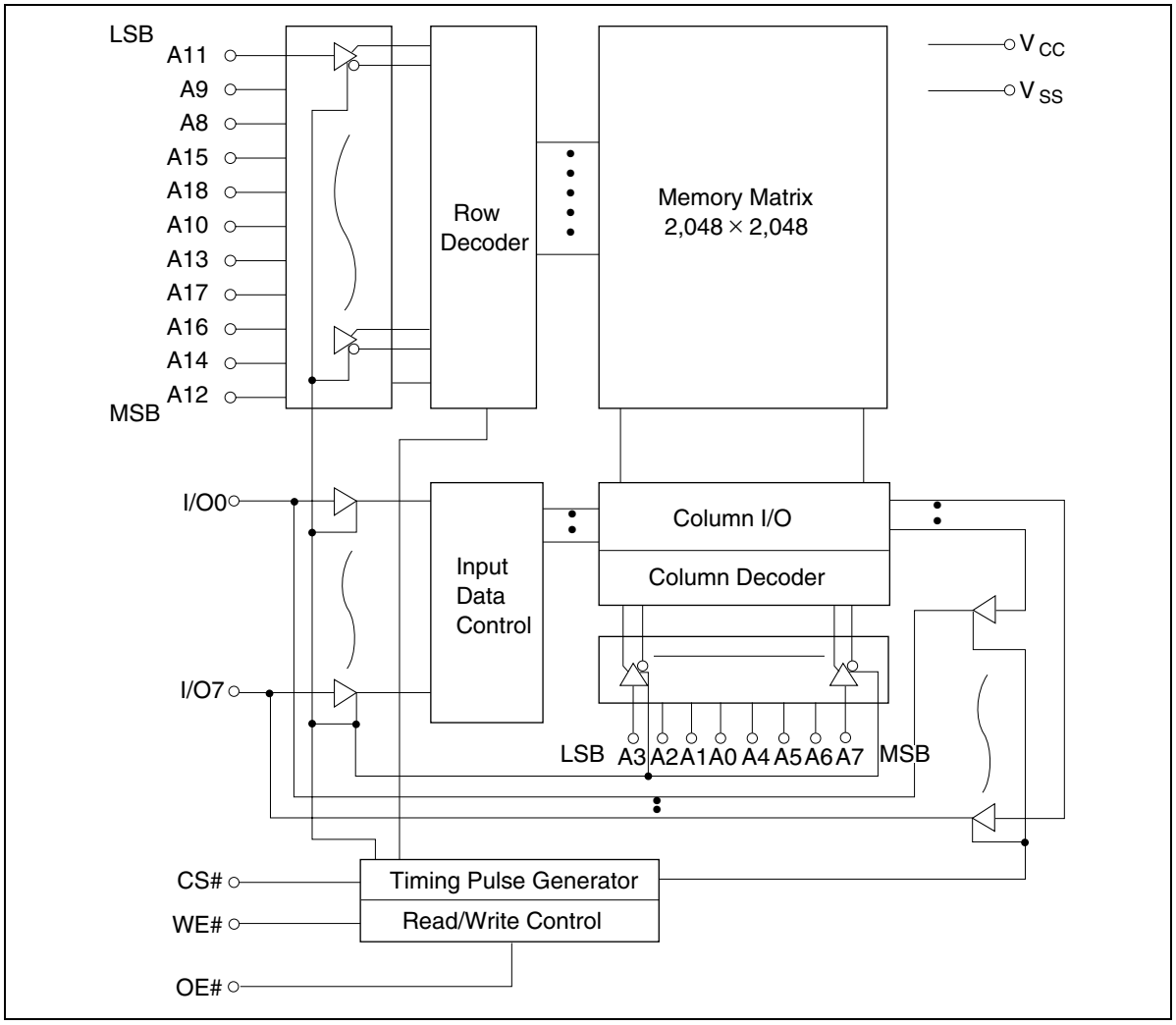
Pin Arrangement



Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
CS# ($\overline{CS}$)	Chip select
OE# ($\overline{OE}$)	Output enable
WE# ($\overline{WE}$)	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Operation Table

WE#	CS#	OE#	Mode	V_{CC} current	I/O0 to I/O7	Ref. cycle
×	H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Terminal voltage on any pin relative to V_{SS}	V_T	–0.5*[1] to V_{CC} + 0.3*[2]	V
Power dissipation	P_T	0.7	W
Operating temperature	Topr	–40 to +85	°C
Storage temperature range	Tstg	–65 to +150	°C
Storage temperature range under bias	Tbias	–40 to +85	°C

Notes: 1. V_T min: –3.0 V for pulse half-width ≤ 30 ns.
2. Maximum voltage is +7.0 V.

DC Operating Conditions

(Ta = –40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	–0.3*[1]	—	0.8	V

Note: 1. V_{IL} min: –3.0 V for pulse half-width ≤ 30 ns.

DC Characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current			$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current			$\|I_{LO}\|$	—	—	1	µA	CS# = V_{IH} or OE# = V_{IH} or WE# = V_{IL} or $V_{I/O}$ = V_{SS} to V_{CC}
Operating current			I_{CC}	—	1.5*[1]	3	mA	CS# = V_{IL}, Others = V_{IH}/ V_{IL}, $I_{I/O}$ = 0 mA
Average operating current			I_{CC1}	—	8*[1]	25	mA	Min. cycle, duty = 100%, CS# = V_{IL}, Others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
			I_{CC2}	—	2*[1]	5	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, CS# ≤ 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby current			I_{SB}	—	0.1*[1]	0.5	mA	CS# = V_{IH}
Standby current	–5SI	to +85°C	I_{SB1}	—	—	10	µA	Vin ≥ 0 V, CS# ≥ V_{CC} – 0.2 V
		to +70°C	I_{SB1}	—	—	8	µA	
		to +40°C	I_{SB1}	—	1.0*[2]	3	µA	
		to +25°C	I_{SB1}	—	0.8*[1]	3	µA	
	–7LI	to +85°C	I_{SB1}	—	—	20	µA	
		to +70°C	I_{SB1}	—	—	16	µA	
		to +40°C	I_{SB1}	—	1.0*[2]	10	µA	
		to +25°C	I_{SB1}	—	0.8*[1]	10	µA	
Output low voltage			V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage			V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA
			V_{OH2}	2.6	—	—	V	I_{OH} = –0.1 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading, and not guaranteed.
2. Typical values are at V_{CC} = 5.0 V, Ta = +40°C and specified loading, and not guaranteed.

Capacitance

(Ta = +25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	Cin	—	—	8	pF	Vin = 0 V	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics

(Ta = –40 to +85°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{IL} = 0.4 V, V_{IH} = 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate + C_L (50 pF) (R1LP0408C-5SI)
  1 TTL Gate + C_L (100 pF) (R1LP0408C-7LI)
  (Including scope and jig)

Read Cycle

		R1LP0408C-I					
		-5SI		-7LI			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	55	—	70	—	ns	
Address access time	t_{AA}	—	55	—	70	ns	
Chip select access time	t_{CO}	—	55	—	70	ns	
Output enable to output valid	t_{OE}	—	25	—	35	ns	
Chip select to output in low-Z	t_{LZ}	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2
Chip deselect to output in high-Z	t_{HZ}	0	20	0	25	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1, 2
Output hold from address change	t_{OH}	10	—	10	—	ns	

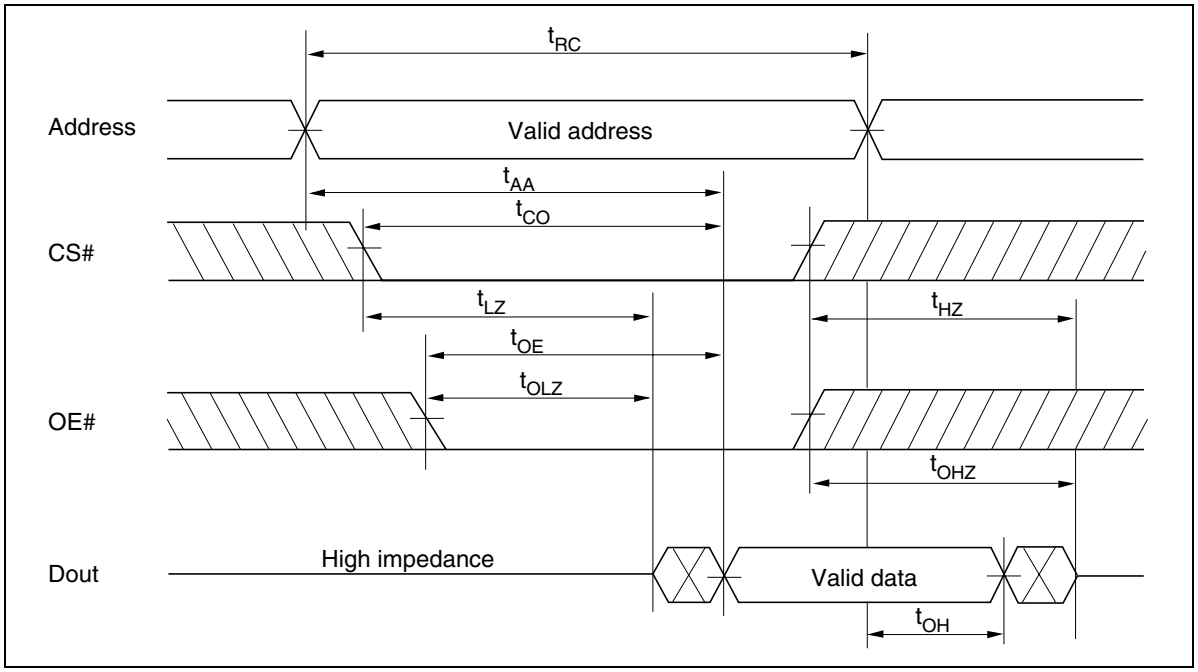
Write Cycle

		R1LP0408C-I					
		-5SI		-7LI			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	55	—	70	—	ns	
Chip selection to end of write	t_{CW}	50	—	60	—	ns	4
Address setup time	t_{AS}	0	—	0	—	ns	5
Address valid to end of write	t_{AW}	50	—	60	—	ns	
Write pulse width	t_{WP}	40	—	50	—	ns	3, 12
Write recovery time	t_{WR}	0	—	0	—	ns	6
Write to output in high-Z	t_{WHZ}	0	20	0	25	ns	1, 2, 7
Data to write time overlap	t_{DW}	25	—	30	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1, 2, 7

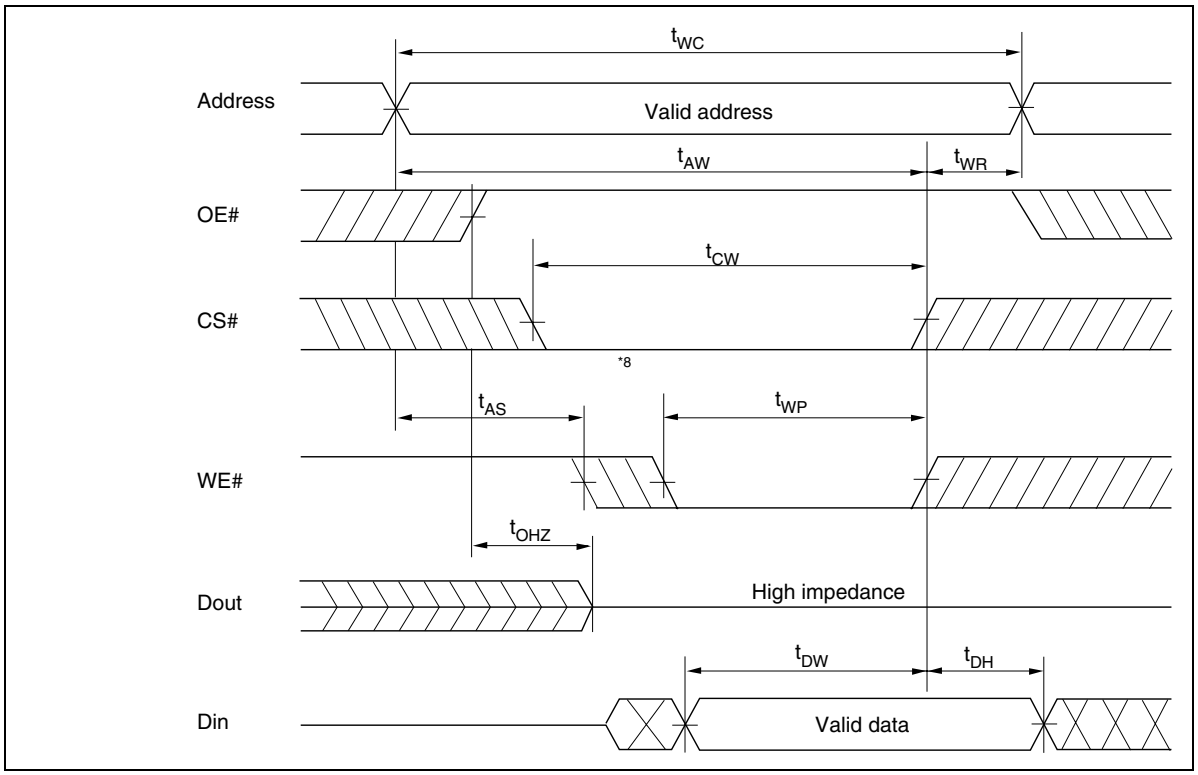
Notes:
1. t_{HZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. A write occurs during the overlap (t_{WP}) of a low CS# and a low WE#. A write begins at the later transition of CS# going low or WE# going low. A write ends at the earlier transition of CS# going high or WE# going high. t_{WP} is measured from the beginning of write to the end of write.
4. t_{CW} is measured from CS# going low to the end of write.
5. t_{AS} is measured from the address valid to the beginning of write.
6. t_{WR} is measured from the earlier of WE# or CS# going high to the end of write cycle.
7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
8. If the CS# low transition occurs simultaneously with the WE# low transition or after the WE# transition, the output remain in a high impedance state.
9. Dout is the same phase of the write data of this write cycle.
10. Dout is the read data of next address.
11. If CS# is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
12. In the write cycle with OE# low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention. $t_{WP} \geq t_{DW}$ min + t_{WHZ} max

Timing Waveform

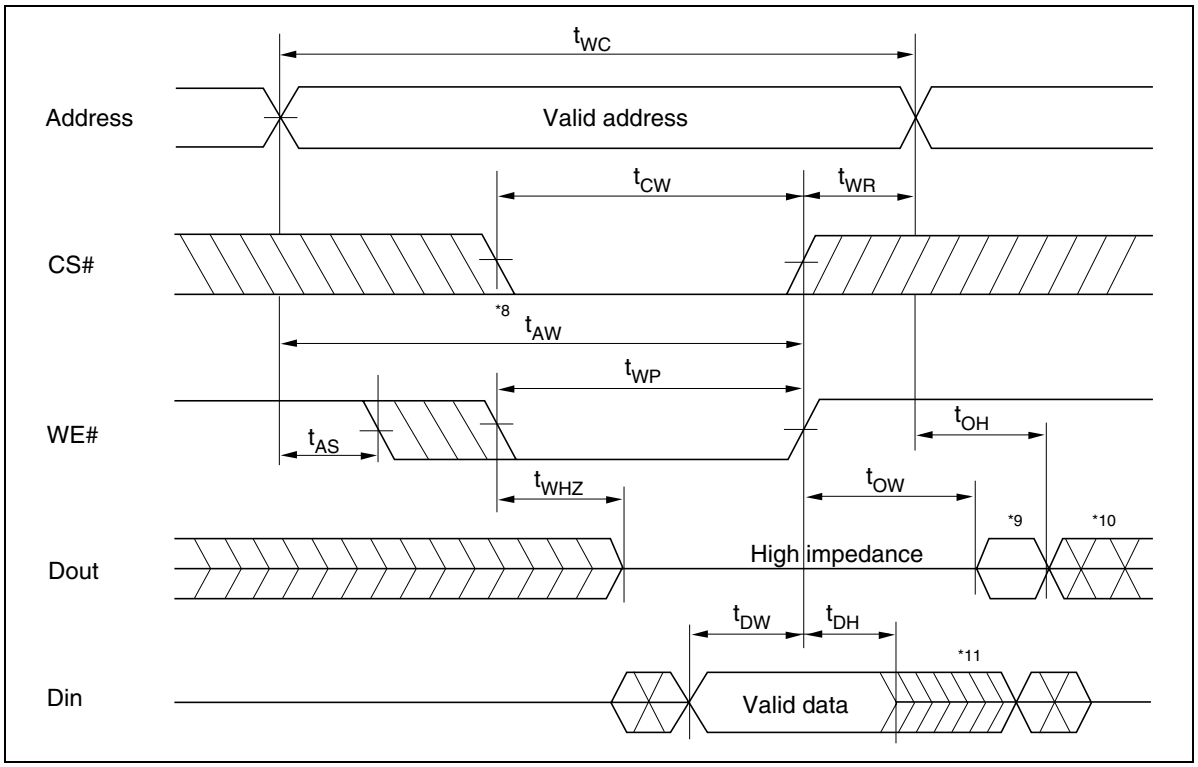
Read Timing Waveform (WE# = V_{IH})



Write Timing Waveform (1) (OE# Clock)



Write Timing Waveform (2) (OE# Low Fixed)



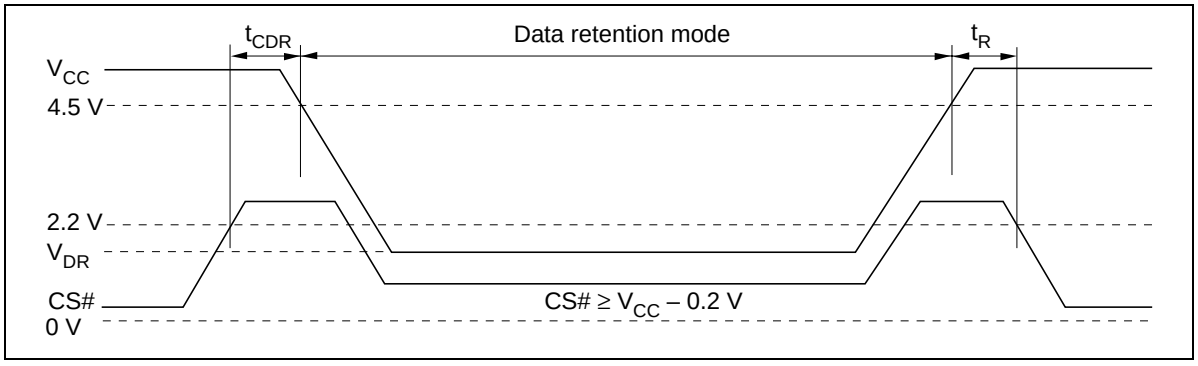
Low V_{CC} Data Retention Characteristics

(Ta = –40 to +85°C)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions*[3]
V_{CC} for data retention			V_{DR}	2	—	—	V	CS# ≥ V_{CC} – 0.2 V, Vin ≥ 0 V
Data retention current	–5SI	to +85°C	I_{CCDR}	—	—	10	µA	V_{CC} = 3.0 V, Vin ≥ 0 V
		to +70°C	I_{CCDR}	—	—	8	µA	CS# ≥ V_{CC} – 0.2 V
		to +40°C	I_{CCDR}	—	1.0*[2]	3	µA	
		to +25°C	I_{CCDR}		0.8*[1]	3	µA	
	–7LI	to +85°C	I_{CCDR}	—	—	20	µA	
		to +70°C	I_{CCDR}	—	—	16	µA	
		to +40°C	I_{CCDR}	—	1.0*[2]	10	µA	
		to +25°C	I_{CCDR}	—	0.8*[1]	10	µA	
Chip deselect to data retention time			t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time			t_R	t_{RC}*[4]	—	—	ns	

Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and specified loading, and not guaranteed.
2. Typical values are at V_{CC} = 3.0 V, Ta = +40°C and specified loading, and not guaranteed.
3. CS# controls address buffer, WE# buffer, OE# buffer, and Din buffer. In data retention mode, Vin levels (address, WE#, OE#, I/O) can be in the high impedance state.
4. t_{RC} = read cycle time.

Low V_{CC} Data Retention Timing Waveform (CS# Controlled)



Rev.	Date	Contents of Modification	
		Page	Description
1.00	Aug.01.2003	—	Initial issue
2.00	May.26.2004	6	DC characteristics –5SI and –7LI items' description are divided.
		12	Low V_{CC} Data Retention Characteristics –5SI and –7LI items' description are divided.
		12	Low V_{CC} Data Retention Timing Waveform 2.4 V to 2.2 V

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Colophon .1.0

Selection Guide

Low Power SRAM

Renesas Electronics
www.renesas.eu

2010.11

About Renesas Electronics Corporation

Renesas Electronics Corporation (TSE: 6723), the world's number one supplier of microcontrollers, is a premier supplier of advanced semiconductor solutions including microcontrollers, SoC solutions and a broad range of analog and power devices as well as memory products. Business operations began as Renesas Electronics in April 2010 through the integration of NEC Electronics Corporation (TSE:6723) and Renesas Technology Corp., with operations spanning research, development, design and manufacturing for a wide range of applications. Headquartered in Japan, Renesas Electronics has subsidiaries in 20 countries worldwide. More information can be found at www.renesas.com.

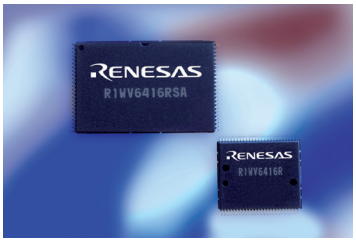
Welcome to the Low Power SRAM product lineup

Renesas memory delivers superior reliability achieved through exclusive advanced technology. An extensive line-up of memory products is available to meet the diverse functional requirements of our customers, covering not only Low Power SRAM, but also QDRII, QDRII+, DDRII & DDRII+ High Speed SRAM and a wide range of serial/parallel EEPROM.

Roadmap

Low Power SRAM		2010	2011	2012	2013	2014	2015	Status
Low	256 kbit	3 V/5 V x8 0.6 µm		0.15 µm Advanced				in MP MP Advanced Version from Q2'11
	1 Mbit	3 V x8 0.25 µm		0.15 µm Advanced				in MP MP Advanced Version from Q1'11
		5 V x8 0.25 µm		0.15 µm Advanced				in MP
	2 Mbit	3 V x8/x16 0.25 µm		0.15 µm Advanced				in MP MP Advanced Version from Q2'11
Middle	4 Mbit	3 V x8/x16		0.15 µm Advanced				in MP
		5 V x8		0.18 µm				in MP
	8 Mbit	3 V x8/x16		0.15 µm Advanced				in MP
		5 V x8/x16		0.18 µm				in MP
High	16 Mbit	3 V x8/x16		0.13 µm CMOS				in MP
	16 Mbit	3 V x8/x16		0.15 µm Advanced				in MP
	32 Mbit	3 V x8/x16		0.15 µm Advanced				in MP
	64 Mbit	3 V x8/x16		0.15 µm Advanced				in MP

- Widest product line-up from 256 kbit – 64 Mbit
- Long term and stable support
- Highest quality due to Renesas core advanced technology
- Easy switch to higher density in the same package
- In house R&D and Fabs



Renesas offers the best quality – our biggest strength

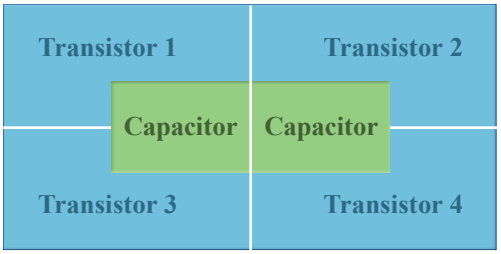
Our advanced technology achieves outstanding results:
- High reliability
- Smaller die size
- Latch-up free
- Soft-error free

SRAM = 6 Transistors

90 nm process:

Process itself is smaller but Transistors are bigger, as they need to store a big amount of charge.

Renesas 150 nm process:



Cell of Renesas core advanced technology, about half the size of full CMOS.

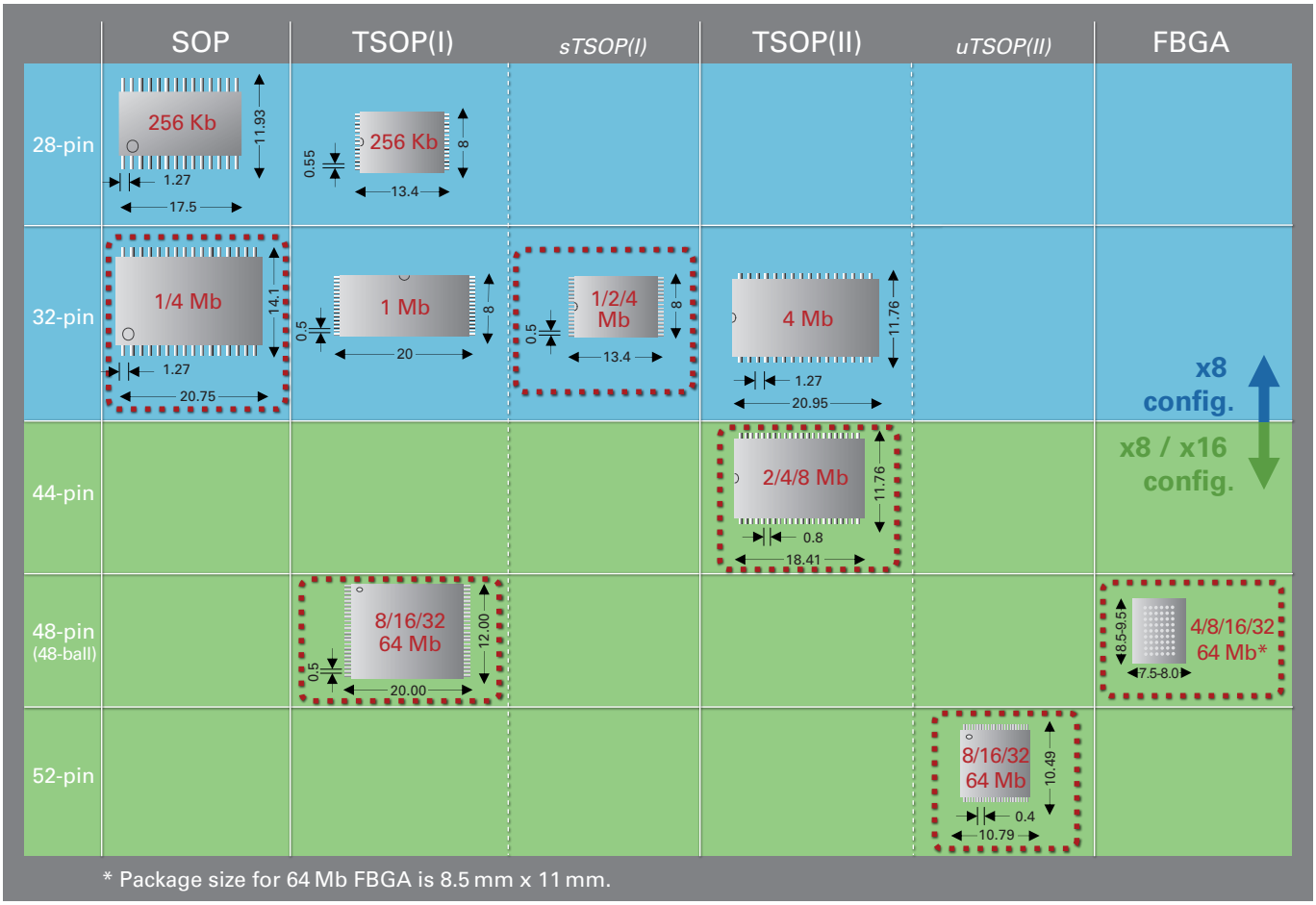
How did we achieve such high quality?

Renesas uses TFT MOSFETs instead of planar MOSFETs. Additionally in the devices, a large amount of charge is stored in two capacitors which subsequently increases the capacitance of the TFTs. These capacitors are positioned above the TFTs, in turn shielding the transistors from alpha and neutron radiation. Together this makes Renesas' SRAM cells latch-up free and enables the lowest soft-error rate in the industry.

We are proud to confirm...

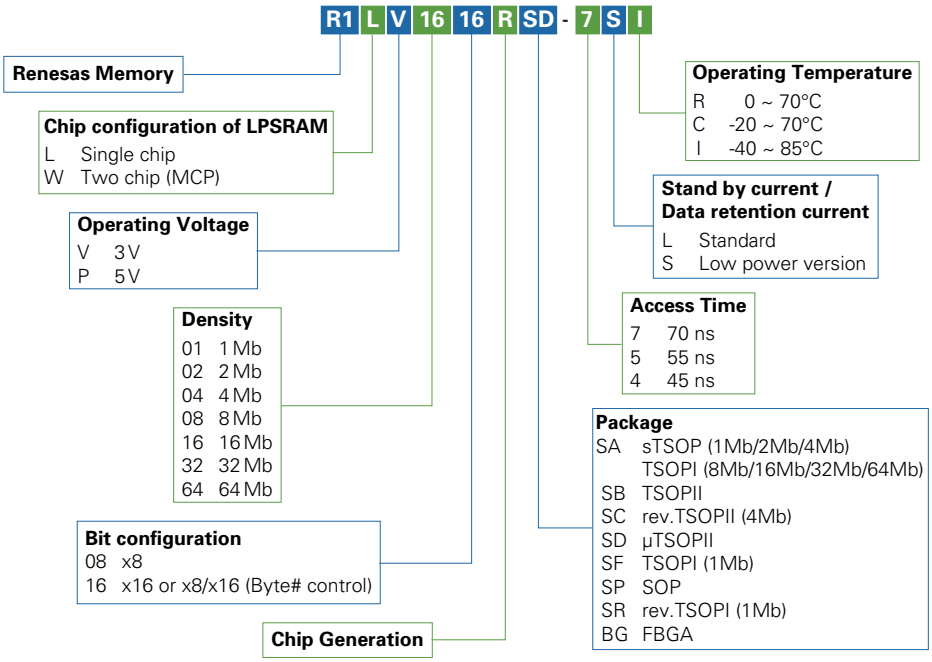
Soft Error Rate of our advanced technology has been tested and confirmed to be less than 100FIT/device.

Package Lineup for Renesas Low Power SRAM



Renesas provides six kinds of packages, which are upwards compatible, making it easy to expand density without changing the PCB.

Low Power SRAM Part Numbering System



Useful Links

Datasheet
http://www.renesas.eu/products/memory/low_power_sram/lpsram_root.jsp

Advanced 0.15 µm Technology
http://www.renesas.eu/products/memory/low_power_sram/child_folder/lpsram_supersram.jsp

Technical update
http://www.renesas.eu/products/memory/low_power_sram/Technical_Update.jsp

Franchised distributors
http://www.renesas.eu/support/purchasing_info/purchasing_info.jsp?title=European%2520Distributors

Product List

Capacity	Configuration	Part Name	Suffix	Package	Access Time (ns)	Process	Voltage	Temperature	Comments
256 kbit	32 k x 8	R1LP5256ESP-5SR R1LP5256ESP-7SR R1LP5256ESA-5SR R1LP5256ESA-7SR	#B0 #S0	SOP(28) SOP(28) TSOP(28) TSOP(28)	55 70	0.15 µm	4.5 V to 5.5 V	0 to 70 °C	Mass production from Q2'11
	32 k x 8	R1LP5256ESP-5SI R1LP5256ESP-7SI R1LP5256ESA-5SI R1LP5256ESA-7SI	#B0 #S0	SOP(28) SOP(28) TSOP(28) TSOP(28)	55 70	0.15 µm	4.5 V to 5.5 V	-40 to 85 °C	Mass production from Q2'11
	32 k x 8	R1LV5256ESP-5SR R1LV5256ESP-7SR R1LV5256ESA-5SR R1LV5256ESA-7SR	#B0 #S0	SOP(28) SOP(28) TSOP(28) TSOP(28)	55 70	0.15 µm	2.7 V to 3.6 V	0 to 70 °C	Mass production from Q2'11
	32 k x 8	R1LV5256ESP-5SI R1LV5256ESP-7SI R1LV5256ESA-5SI R1LV5256ESA-7SI	#B0 #S0	SOP(28) SOP(28) TSOP(28) TSOP(28)	55 70	0.15 µm	2.7 V to 3.6 V	-40 to 85 °C	Mass production from Q2'11
1 Mbit	128 k x 8	R1LP0108ESP-5SR R1LP0108ESP-7SR R1LP0108ESF-5SR R1LP0108ESF-7SR R1LP0108ESR-5SR R1LP0108ESR-7SR R1LP0108ESA-5SR R1LP0108ESA-7SR	#B0 #S0	SOP(32) SOP(32) TSOP(32) TSOP(32) rev.TSOP(32) rev.TSOP(32) sTSOP(32) sTSOP(32)	55 70	0.15 µm	4.5 V to 5.5 V	0 to 70 °C	
	128 k x 8	R1LP0108ESP-5SI R1LP0108ESP-7SI R1LP0108ESF-5SI R1LP0108ESF-7SI R1LP0108ESR-5SI R1LP0108ESR-7SI R1LP0108ESA-5SI R1LP0108ESA-7SI	#B0 #S0	SOP(32) SOP(32) TSOP(32) TSOP(32) rev.TSOP(32) rev.TSOP(32) sTSOP(32) sTSOP(32)	55 70	0.15 µm	4.5 V to 5.5 V	-40 to 85 °C	
	128 k x 8	R1LV0108ESP-5SR R1LV0108ESP-7SR R1LV0108ESF-5SR R1LV0108ESF-7SR R1LV0108ESA-5SR R1LV0108ESA-7SR	#B0 #S0	SOP(32) SOP(32) TSOP(32) TSOP(32) sTSOP(32) sTSOP(32)	55 70	0.15 µm	2.7 V to 3.6 V	0 to 70 °C	Mass production from Q1'11
	128 k x 8	R1LV0108ESP-5SI R1LV0108ESP-7SI R1LV0108ESF-5SI R1LV0108ESF-7SI R1LV0108ESA-5SI R1LV0108ESA-7SI	#B0 #S0	SOP(32) SOP(32) TSOP(32) TSOP(32) sTSOP(32) sTSOP(32)	55 70	0.15 µm	2.7 V to 3.6 V	-40 to 85 °C	Mass production from Q1'11
2 Mbit	256 k x 8	R1LV0208BSA-5SI R1LV0208BSA-7SI	#B0 #S0	sTSOP(32)	55 70	0.15 µm	2.7 V to 3.6 V	-40 to 85 °C	Mass production from Q2'11
	128 k x 16	R1LV0216BSB-5SI R1LV0216BSB-7SI	#B0 #S0	TSOP(44)	55 70	0.15 µm	2.7 V to 3.6 V	-40 to 85 °C	Mass production from Q2'11
4 Mbit	512 k x 8	R1LP0408CSP-5SC R1LP0408CSP-7LC R1LP0408CSB-5SC R1LP0408CSB-7LC R1LP0408CSC-5SC R1LP0408CSC-7LC	#B0 #S0 #D0 #S0 #D0 #S0	SOP(32) SOP(32) TSOP(32) TSOP(32) rev.TSOP(32) rev.TSOP(32)	55 70	0.18 µm	4.5 V to 5.5 V	-20 to 70 °C	
	512 k x 8	R1LP0408CSP-5SI R1LP0408CSP-7LI R1LP0408CSB-5SI R1LP0408CSB-7LI R1LP0408CSC-5SI R1LP0408CSC-7LI	#B0 #S0 #D0 #S0 #D0 #S0	SOP(32) SOP(32) TSOP(32) TSOP(32) rev.TSOP(32) rev.TSOP(32)	55 70	0.18 µm	4.5 V to 5.5 V	-40 to 85 °C	
	512 k x 8	R1LV0408DSP-5SR R1LV0408DSP-7LR R1LV0408DSA-5SR R1LV0408DSA-7LR R1LV0408DSB-5SR R1LV0408DSB-7LR	#B0 #S0 #B0 #S0 #B0 #S0	SOP(32) SOP(32) sTSOP(32) sTSOP(32) TSOP(32) TSOP(32)	55 70	0.15 µm	2.7 V to 3.6 V	0 to 70 °C	
	512 k x 8	R1LV0408DSP-5SI R1LV0408DSP-7LI R1LV0408DSA-5SI R1LV0408DSA-7LI R1LV0408DSB-5SI R1LV0408DSB-7LI	#B0 #S0 #B0 #S0 #B0 #S0	SOP(32) SOP(32) sTSOP(32) sTSOP(32) TSOP(32) TSOP(32)	55 70	0.15 µm	2.7 V to 3.6 V	-40 to 85 °C	

Capacity	Configuration	Part Name	Suffix	Package	Access Time (ns)	Process	Voltage	Temperature	Comments
4 Mbit	256 k x 16	R1LV0416DSB-5SR R1LV0416DSB-7LR	#B0 #S0	TSOP(44)	55 70	0.15 µm	2.7 V to 3.6 V	0 to 70 °C	2-chip select
	256 k x 16	R1LV0416DSB-5SI R1LV0416DSB-7LI	#B0 #S0	TSOP(44)	55 70	0.15 µm	2.7 V to 3.6 V	-40 to 85 °C	2-chip select
	256 k x 16	R1LV0416DBG-5SR R1LV0416DBG-7LR	#B0 #S0	FBGA(48)	55 70	0.15 µm	2.7 V to 3.6 V	0 to 70 °C	2-chip select
	256 k x 16	R1LV0416DBG-5SI R1LV0416DBG-7LI	#B0 #S0	FBGA(48)	55 70	0.15 µm	2.7 V to 3.6 V	-40 to 85 °C	2-chip select
	256 k x 16	R1LV0414DSB-5SR R1LV0414DSB-7LR	#B0 #S0	TSOP(44)	55 70	0.15 µm	2.7 V to 3.6 V	0 to 70 °C	1-chip select
	256 k x 16	R1LV0414DSB-5SI R1LV0414DSB-7LI	#B0 #S0	TSOP(44)	55 70	0.15 µm	2.7 V to 3.6 V	-40 to 85 °C	1-chip select
8 Mbit	1 M x 8	HM28100TTI5SE		TSOP(44)	55	0.18 µm	5.0 V ± 10%	-40 to 85 °C	former HM628100LTTI-5SL
	1 M x 8	R1LV0808ASB-5SI R1LV0808ASB-7SI	#B0 #S0	TSOP(44)	55 70	0.15 µm	2.4 V to 3.6 V	-40 to 85 °C	
	1 M x 8/ 512 k x 16	R1LV0816ASD-5SI R1LV0816ASD-7SI	#B0 #S0	µTSOP(52)	55 70	0.15 µm	2.4 V to 3.6 V	-40 to 85 °C	
	512 k x 16	HM216514TTI5SE		TSOP(44)	55	0.18 µm	4.5 V to 5.5 V	-40 to 85 °C	former HM6216514LTTI-5SL
	1 M x 8/ 512 k x 16	R1LV0816ASA-5SI R1LV0816ASA-7SI	#B0 #S0	TSOP(48) NEW	55 70	0.15 µm	2.4 V to 3.6 V	-40 to 85 °C	
	512 k x 16	R1LV0816ASB-5SI R1LV0816ASB-7SI	#B0 #S0	TSOP(44)	55 70	0.15 µm	2.4 V to 3.6 V	-40 to 85 °C	
	512 k x 16	R1LV0816ABG-5SI R1LV0816ABG-7SI	#B0 #S0	FBGA(48) FBGA(48)	55 70	0.15 µm	2.4 V to 3.6 V	-40 to 85 °C	
16 Mbit	2 M x 8/ 1 M x 16	R1LV1616RSD-7SR R1LV1616RSD-7SI	#B0 #S0	µTSOP(52)	70 85	0.15 µm	2.7 V to 3.6 V	0 to 70 °C -40 to 85 °C	
	2 M x 8/ 1 M x 16	R1LV1616RSD-5SR R1LV1616RSD-5SI	#B0 #S0	µTSOP(52)	55	0.15 µm	2.7 V to 3.6 V	0 to 70 °C -40 to 85 °C	
	2 M x 8/ 1 M x 16	R1LV1616RSA-5SR R1LV1616RSA-7SR R1LV1616RSA-5SI R1LV1616RSA-7SI	#B0 #S0	TSOP(48)	55 70 85	0.15 µm	2.7 V to 3.6 V	0 to 70 °C 0 to 70 °C -40 to 85 °C -40 to 85 °C	
	2 M x 8/ 1 M x 16	R1LV1616HSA-4SI R1LV1616HSA-5SI	#B0 #S0	TSOP(48)	45 55	0.13 µm	2.7 V to 3.6 V	-40 to 85 °C	
	1 M x 16	R1LV1616RBG-7SR R1LV1616RBG-7SI	#B0 #S0	FBGA(48)	70 85	0.15 µm	2.7 V to 3.6 V	0 to 70 °C -40 to 85 °C	
	1 M x 16	R1LV1616RBG-5SR R1LV1616RBG-5SI	#B0 #S0	FBGA(48)	55	0.15 µm	2.7 V to 3.6 V	0 to 70 °C -40 to 85 °C	
	1 M x 16	R1LV1616HBG-4SI R1LV1616HBG-5SI	#B0 #S0	FBGA(48)	45 55	0.13 µm	2.7 V to 3.6 V	-40 to 85 °C	
32 Mbit (MCP)	2 M x 16	R1WV3216RBG-7SR R1WV3216RBG-7SI	#B0 #S0	FBGA(48)	70 85	0.15 µm	2.7 V to 3.6 V	0 to 70 °C -40 to 85 °C	
32 Mbit	4 M x 8/ 2 M x 16	R1LV3216RSA-5SR R1LV3216RSA-7SR R1LV3216RSA-5SI R1LV3216RSA-7SI	#B0 #S0	TSOP(48)	55 70	0.15 µm	2.7 V to 3.6 V	0 to 70 °C 0 to 70 °C -40 to 85 °C -40 to 85 °C	
	4 M x 8/ 2 M x 16	R1LV3216RSD-5SR R1LV3216RSD-7SR R1LV3216RSD-5SI R1LV3216RSD-7SI	#B0 #S0	µTSOP(52)	55 70	0.15 µm	2.7 V to 3.6 V	0 to 70 °C 0 to 70 °C -40 to 85 °C -40 to 85 °C	
64 Mbit (MCP)	4 M x 16	R1WV6416RBG-5SR R1WV6416RBG-7SR R1WV6416RBG-5SI R1WV6416RBG-7SI	#B0 #S0	FBGA(48)	55 70	0.15 µm	2.7 V to 3.6 V	0 to 70 °C 0 to 70 °C -40 to 85 °C -40 to 85 °C	
	8 M x 8/ 4 M x 16	R1WV6416RSA-5SR R1WV6416RSA-7SR R1WV6416RSA-5SI R1WV6416RSA-7SI	#B0 #S0	TSOP(48)	55 70	0.15 µm	2.7 V to 3.6 V	0 to 70 °C 0 to 70 °C -40 to 85 °C -40 to 85 °C	
	8 M x 8/ 4 M x 16	R1WV6416RSD-5SR R1WV6416RSD-7SR R1WV6416RSD-5SI R1WV6416RSD-7SI	#B0 #S0	µTSOP(52)	55 70	0.15 µm	2.7 V to 3.6 V	0 to 70 °C 0 to 70 °C -40 to 85 °C -40 to 85 °C	

All our parts are RoHS compliant. Suffix: #B0 is indicating loose parts. Suffix #S0 is indicating Tape + Reel (1,000 pcs. per reel). MCP: Multi Chip Package

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