

BLP05H635XR; BLP05H635XRG

Power LDMOS transistor

AMPLEON

Rev. 4 — 21 September 2016

Product data sheet

1. Product profile

1.1 General description

A 35 W extremely rugged LDMOS power transistor for broadcast and industrial applications in the HF to 600 MHz band.

Table 1. Application information

| Test signal | f | V _{DS} | P _L | G _p | η _D |
|-------------|--------|-----------------|----------------|----------------|----------------|
| | (MHz) | (V) | (W) | (dB) | (%) |
| pulsed RF | 108 | 50 | 35 | 27 | 75 |
| CW | 63.86 | 50 | 35 | 29.4 | 75.6 |
| | 127.72 | 50 | 35 | 26.8 | 75.7 |

1.2 Features and benefits

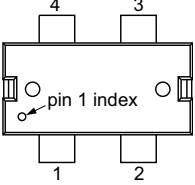
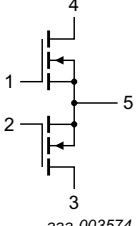
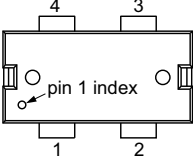
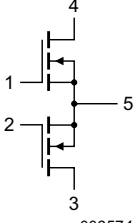
- Easy power control
- Integrated double sided ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 600 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

2. Pinning information

Table 2. Pinning

| Pin | Description | Simplified outline | Graphic symbol |
|---------------------------------|-----------------------|---|--|
| BLP05H635XR (SOT1223-2) | | | |
| 1 | gate 2 |  |  aaa-003574 |
| 2 | gate 1 | | |
| 3 | drain 1 | | |
| 4 | drain 2 | | |
| 5 | source ^[1] | | |
| BLP05H635XRG (SOT1224-2) | | | |
| 1 | gate 2 |  |  aaa-003574 |
| 2 | gate 1 | | |
| 3 | drain 1 | | |
| 4 | drain 2 | | |
| 5 | source ^[1] | | |

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|--------------|---------|---|-----------|
| | Name | Description | Version |
| BLP05H635XR | HSOP4F | plastic, heatsink small outline package; 4 leads (flat) | SOT1223-2 |
| BLP05H635XRG | HSOP4F | plastic, heatsink small outline package; 4 leads | SOT1224-2 |

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|----------------------|----------------|-----|------|------|
| V_{DS} | drain-source voltage | | - | 135 | V |
| V_{GS} | gate-source voltage | | -6 | +11 | V |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| T_j | junction temperature | ^[1] | - | 225 | °C |

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

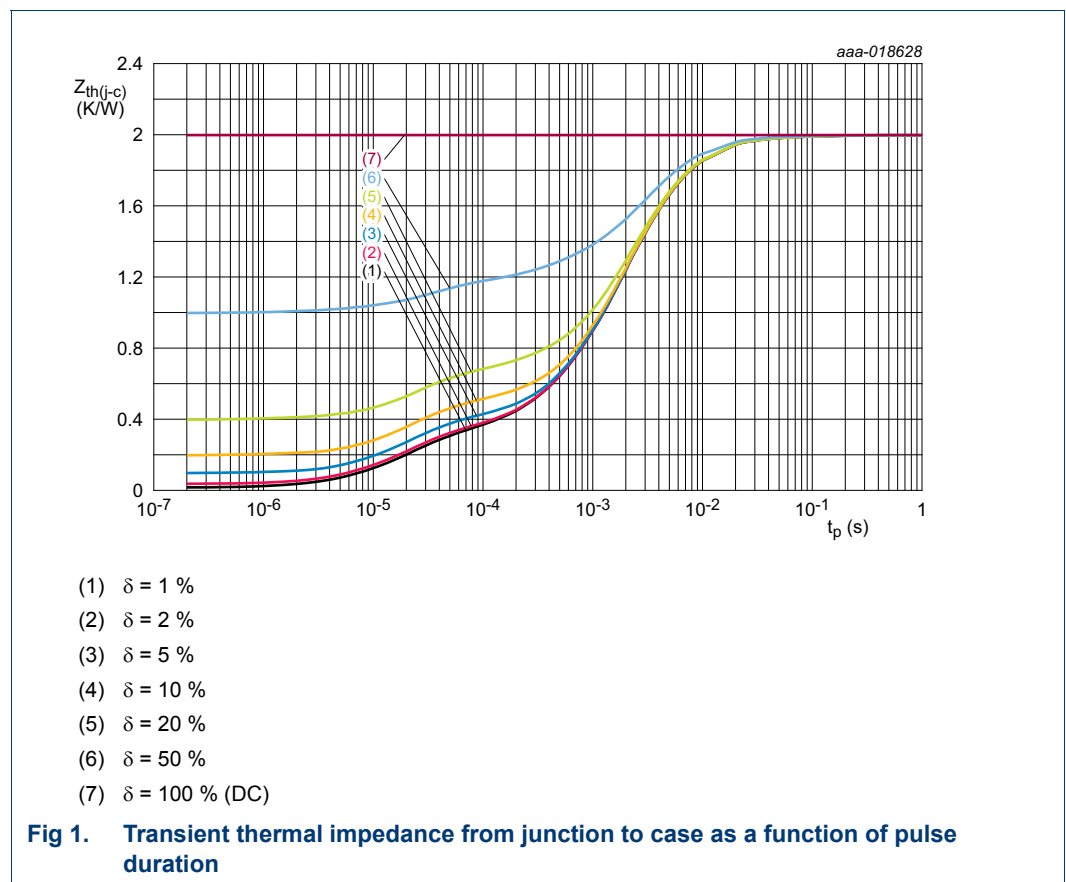
Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|---------------|---|---|------|------|
| $R_{th(j-c)}$ | thermal resistance from junction to case | $T_j = 115\text{ °C}$ [1][2] | 2.0 | K/W |
| $Z_{th(j-c)}$ | transient thermal impedance from junction to case | $T_j = 150\text{ °C}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\text{ %}$ [3] | 0.68 | K/W |

[1] T_j is the junction temperature.

[2] $R_{th(j-c)}$ is measured under RF conditions.

[3] See Figure 1.



6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$; per section unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|--------------------------------|---|------|-----|------|---------------|
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $V_{GS} = 0\text{ V}$; $I_D = 0.125\text{ mA}$ | 135 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $V_{DS} = 10\text{ V}$; $I_D = 12.5\text{ mA}$ | 1.25 | 1.8 | 2.25 | V |
| V_{GSq} | gate-source quiescent voltage | $V_{DS} = 50\text{ V}$; $I_D = 10\text{ mA}$ | - | 1.7 | - | V |
| I_{DSS} | drain leakage current | $V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$ | - | - | 1.4 | μA |

Table 6. DC characteristics ...continued
 $T_j = 25\text{ }^\circ\text{C}$; per section unless otherwise specified.

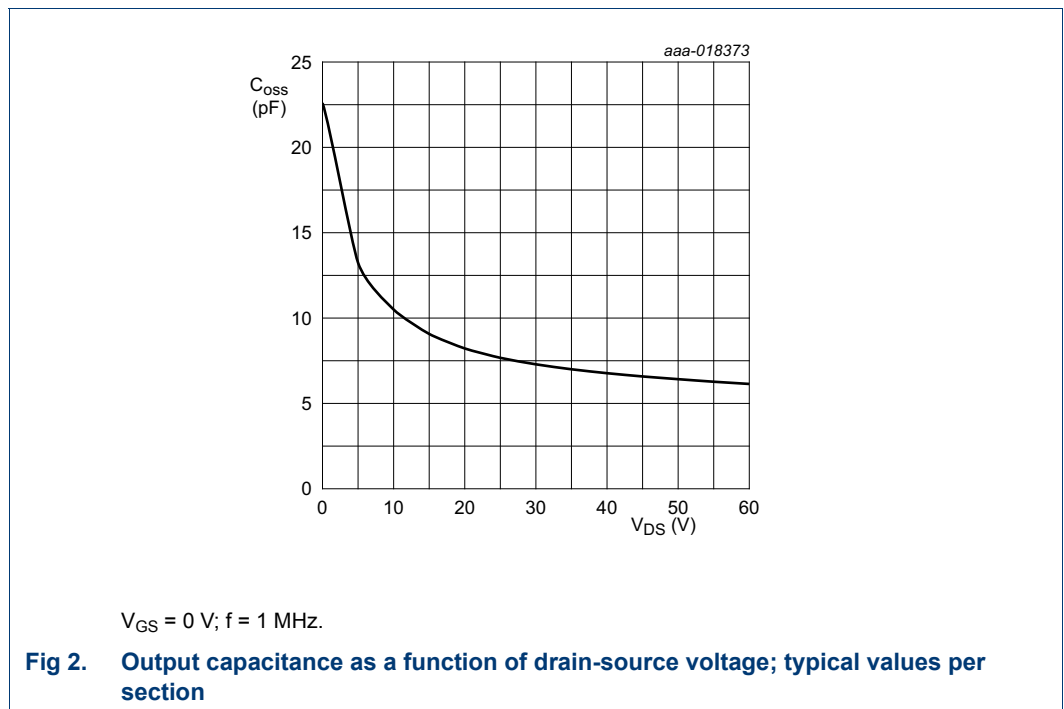
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|----------------------------------|--|-----|-----|-----|----------|
| I_{DSX} | drain cut-off current | $V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$ | - | 1.8 | - | A |
| I_{GSS} | gate leakage current | $V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$ | - | - | 140 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 437.5\text{ mA}$ | - | 3.2 | - | Ω |

Table 7. AC characteristics
 $T_j = 25\text{ }^\circ\text{C}$; per section unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|----------------------|---|-----|------|-----|------|
| C_{rs} | feedback capacitance | $V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$ | - | 0.12 | - | pF |
| C_{iss} | input capacitance | $V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$ | - | 16.2 | - | pF |
| C_{oss} | output capacitance | $V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$ | - | 6.4 | - | pF |

Table 8. RF characteristics
 Test signal: pulsed RF; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\%$; $f = 108\text{ MHz}$; RF performance at $V_{DS} = 50\text{ V}$;
 $I_{Dq} = 10\text{ mA}$; $T_{case} = 25\text{ }^\circ\text{C}$; unless otherwise specified; in a class-AB production test circuit.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|-------------------|---------------------|------|-----|-----|------|
| G_p | power gain | $P_L = 35\text{ W}$ | 25.5 | 27 | - | dB |
| RL_{in} | input return loss | $P_L = 35\text{ W}$ | - | -25 | - | dB |
| η_D | drain efficiency | $P_L = 35\text{ W}$ | 71 | 75 | - | % |



7. Test information

7.1 Ruggedness in class-AB operation

The BLP05H635XR and BLP05H635XRG are capable of withstanding a load mismatch corresponding to VSWR > 65 : 1 through all phases under the following conditions: $V_{DS} = 50\text{ V}$; $I_{DQ} = 20\text{ mA}$; $P_L = 35\text{ W}$ pulsed; $f = 108\text{ MHz}$.

7.2 Impedance information

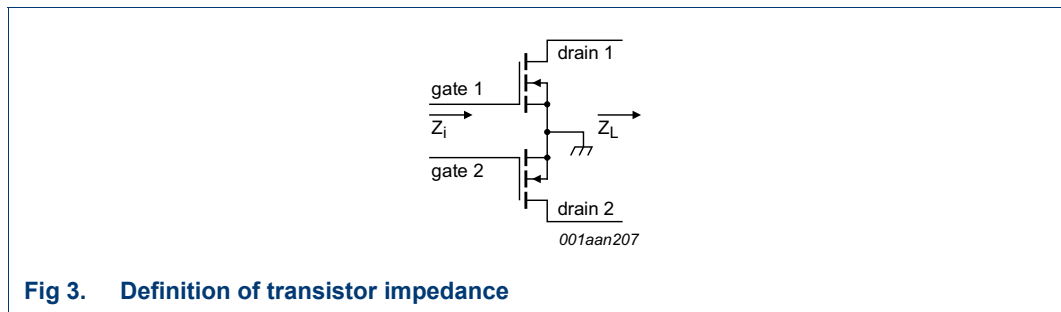


Fig 3. Definition of transistor impedance

Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at $V_{DS} = 50\text{ V}$ and $P_L = 35\text{ W}$.

| f | Z_i | Z_L |
|-------|---------------|---------------|
| (MHz) | (Ω) | (Ω) |
| 108 | 46.6 – j282.0 | 100.6 + j26.9 |

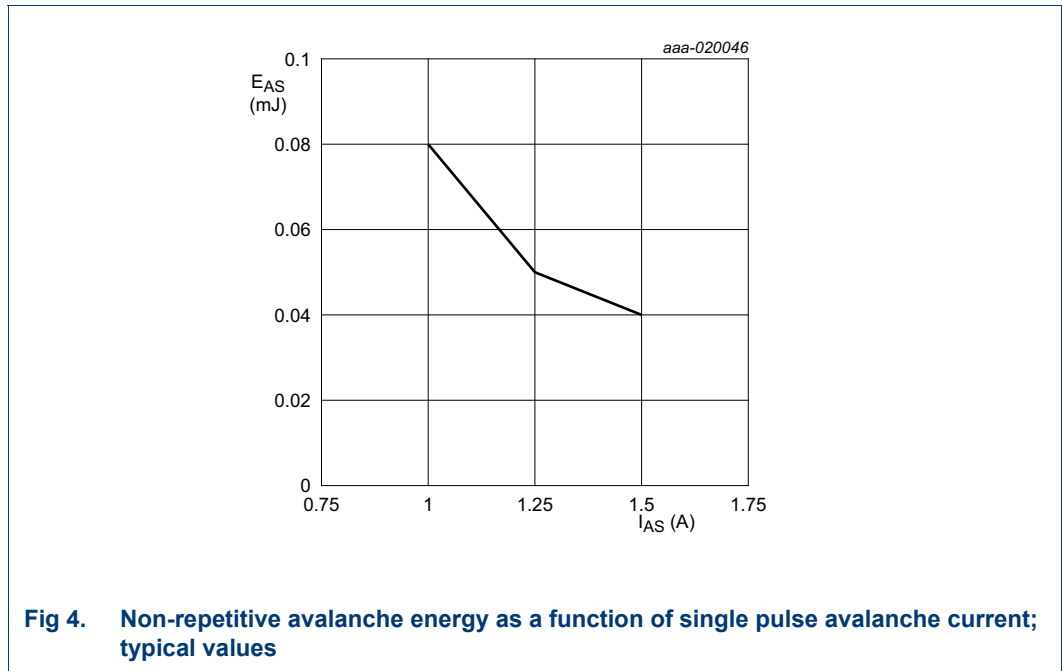
7.3 UIS avalanche energy

Table 10. Typical avalanche data per section

$T_{amb} = 25\text{ }^\circ\text{C}$; typical test data; test jig without water cooling.

| I_{AS} | E_{AS} |
|----------|----------|
| (A) | (J) |
| 1.0 | 0.08 |
| 1.25 | 0.05 |
| 1.5 | 0.04 |

For information see application note AN10273.



7.4 Test circuit

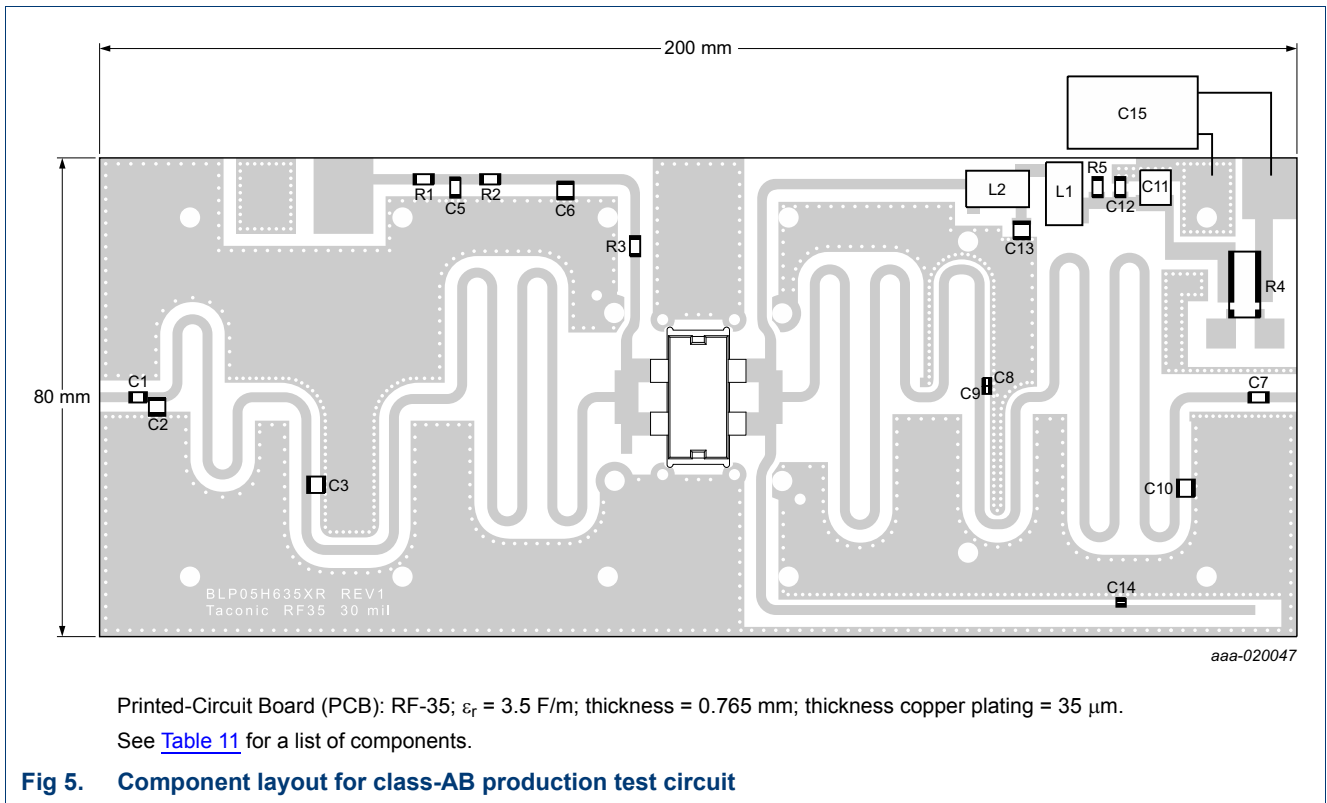


Table 11. List of components

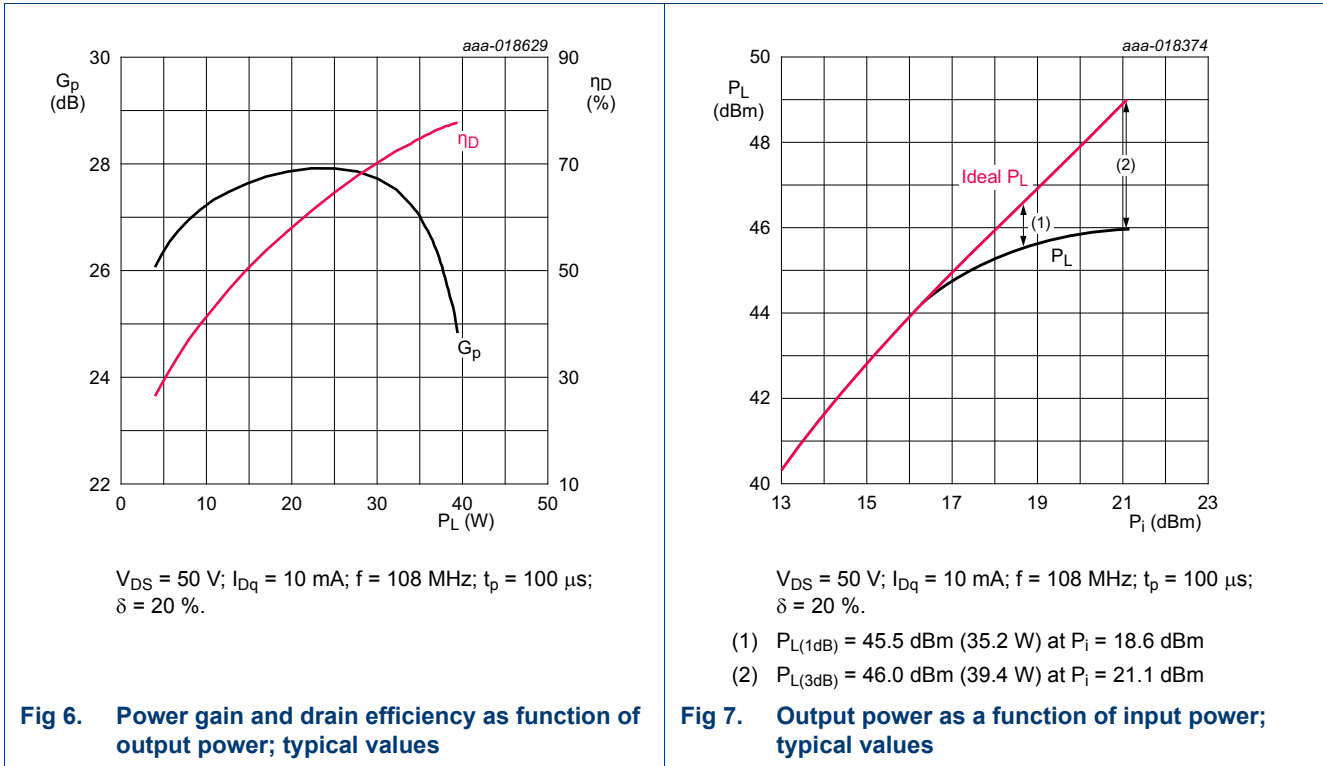
For test circuit see [Figure 5](#).

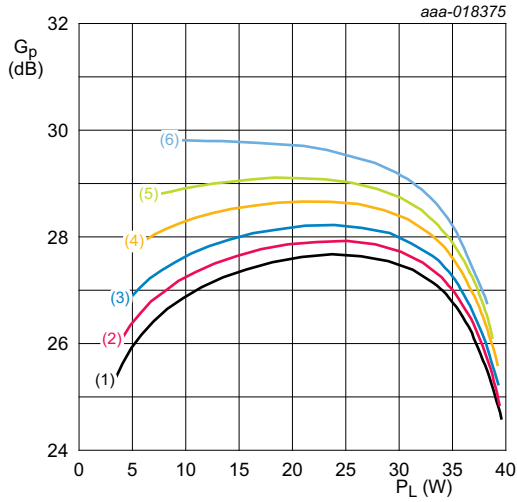
| Component | Description | Value | Remarks |
|-----------|-----------------------------------|----------------------|------------------------|
| C1, C7 | multilayer ceramic chip capacitor | 470 pF | ATC 800B |
| C2 | multilayer ceramic chip capacitor | 120 pF | ATC 800B |
| C3 | multilayer ceramic chip capacitor | 390 pF | ATC 800B |
| C5 | multilayer ceramic chip capacitor | 1 μ F, 50 V | GRM32RR71H105KA01L |
| C6, C13 | multilayer ceramic chip capacitor | 820 pF | ATC 800B |
| C8, C9 | multilayer ceramic chip capacitor | 39 pF | ATC 100A |
| C10 | multilayer ceramic chip capacitor | 27 pF | ATC 800B |
| C11 | multilayer ceramic chip capacitor | 4.7 μ F, 100 V | C5750X7RA475KT/A |
| C12 | multilayer ceramic chip capacitor | 100 nF | GRM188R72A104KA35D |
| C14 | multilayer ceramic chip capacitor | 15 pF | ATC 800B |
| C15 | electrolytic capacitor | 2200 μ F, 63 V | Vishay |
| L1 | wire inductor | 169 nH | Coilcraft:132-12SMG |
| L2 | wire inductor | 90 nH | Coilcraft:132-9SMG |
| R1, R2 | resistor | 10 Ω | SMD 1206 |
| R3 | resistor | 4.64 k Ω | SMD 0805 |
| R4 | shunt resistor | 50 m Ω | Ohmite: FC4L110R050FER |
| R5 | resistor | 7.5 Ω , 0.6 W | SMD 1206 |

7.5 Graphical data

The following figures are measured in a class-AB production test circuit.

7.5.1 1-Tone CW pulsed

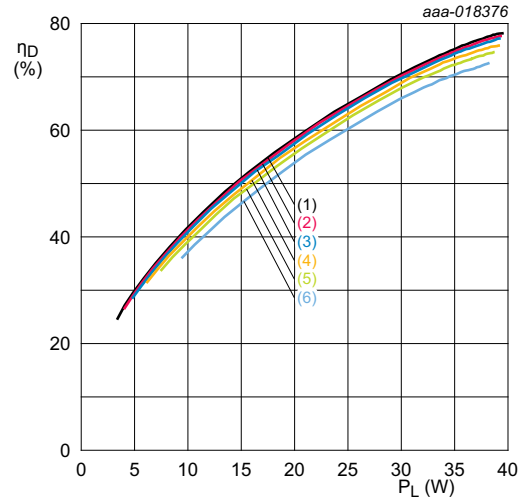




$V_{DS} = 50 \text{ V}; f = 108 \text{ MHz}; t_p = 100 \text{ } \mu\text{s}; \delta = 20 \text{ } \%$.

- (1) $I_{Dq} = 5 \text{ mA}$
- (2) $I_{Dq} = 10 \text{ mA}$
- (3) $I_{Dq} = 20 \text{ mA}$
- (4) $I_{Dq} = 50 \text{ mA}$
- (5) $I_{Dq} = 100 \text{ mA}$
- (6) $I_{Dq} = 200 \text{ mA}$

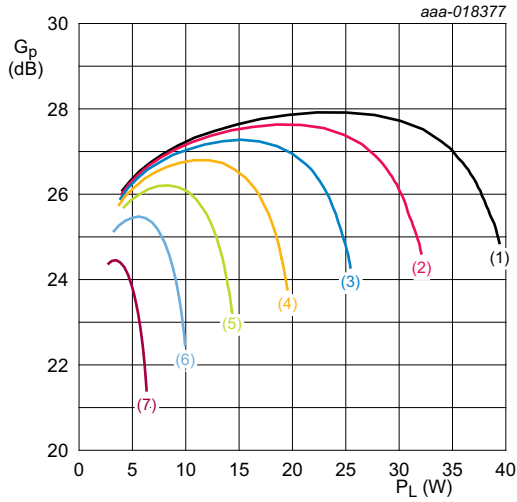
Fig 8. Power gain as a function of output power; typical values



$V_{DS} = 50 \text{ V}; f = 108 \text{ MHz}; t_p = 100 \text{ } \mu\text{s}; \delta = 20 \text{ } \%$.

- (1) $I_{Dq} = 5 \text{ mA}$
- (2) $I_{Dq} = 10 \text{ mA}$
- (3) $I_{Dq} = 20 \text{ mA}$
- (4) $I_{Dq} = 50 \text{ mA}$
- (5) $I_{Dq} = 100 \text{ mA}$
- (6) $I_{Dq} = 200 \text{ mA}$

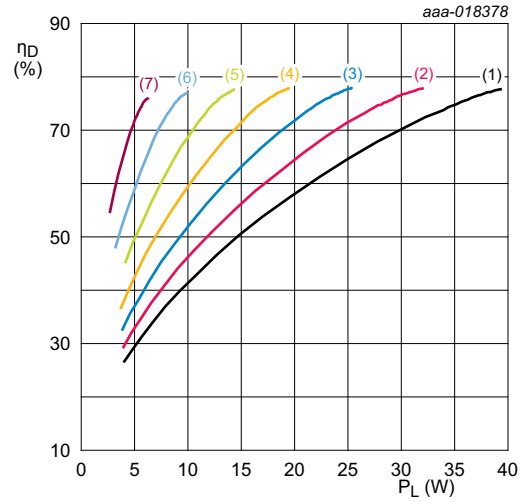
Fig 9. Drain efficiency as a function of output power; typical values



$I_{Dq} = 10$ mA; $f = 108$ MHz; $t_p = 100$ μ s; $\delta = 20$ %.

- (1) $V_{DS} = 50$ V
- (2) $V_{DS} = 45$ V
- (3) $V_{DS} = 40$ V
- (4) $V_{DS} = 35$ V
- (5) $V_{DS} = 30$ V
- (6) $V_{DS} = 25$ V
- (7) $V_{DS} = 20$ V

Fig 10. Power gain as a function of output power; typical values



$I_{Dq} = 10$ mA; $f = 108$ MHz; $t_p = 100$ μ s; $\delta = 20$ %.

- (1) $V_{DS} = 50$ V
- (2) $V_{DS} = 45$ V
- (3) $V_{DS} = 40$ V
- (4) $V_{DS} = 35$ V
- (5) $V_{DS} = 30$ V
- (6) $V_{DS} = 25$ V
- (7) $V_{DS} = 20$ V

Fig 11. Drain efficiency as a function of output power; typical values

8. Package outline

HSOP4F: plastic, heatsink small outline package; 4 leads(flat)

SOT1223-2

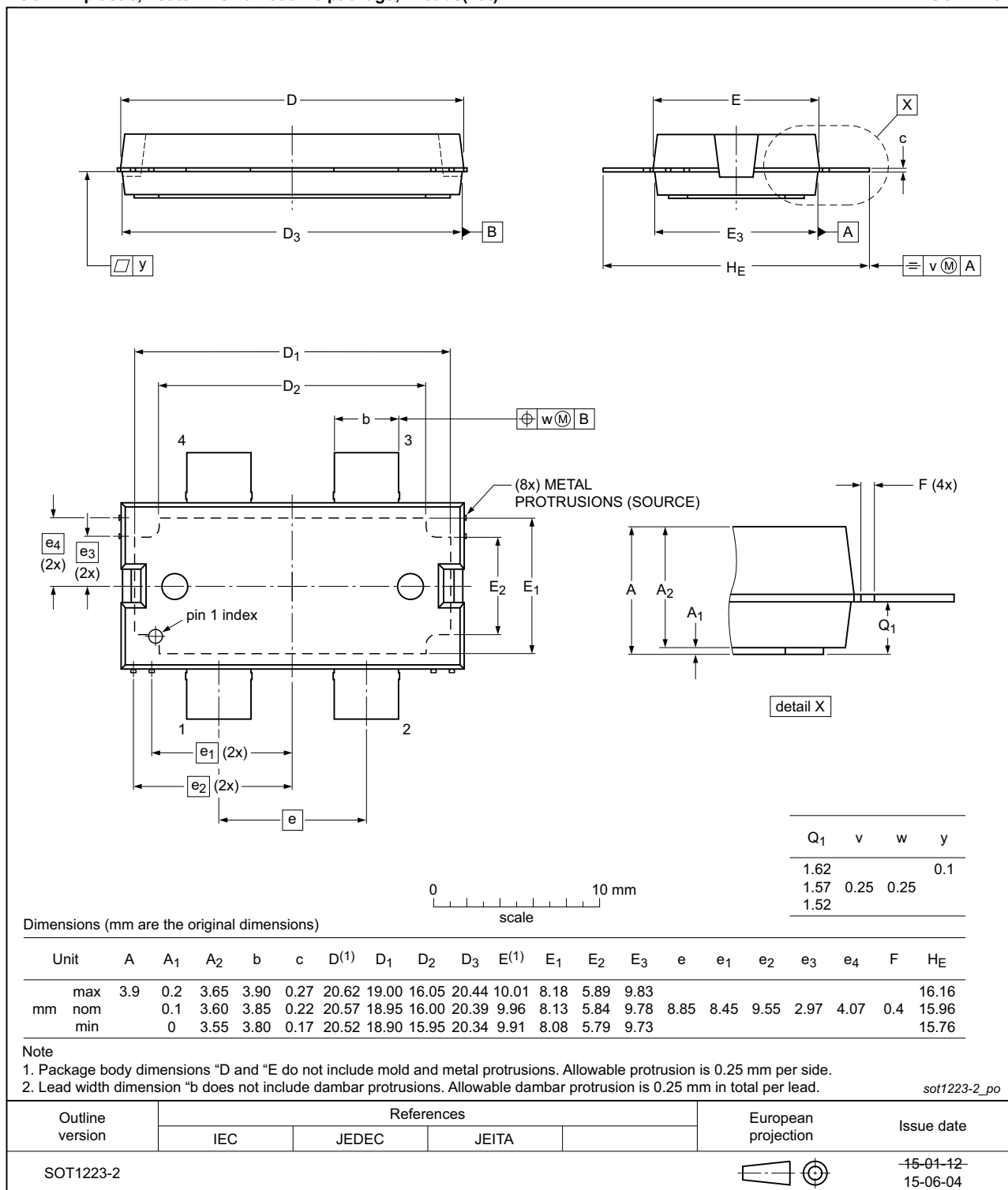


Fig 12. Package outline SOT1223-2 (HSOP4F)

HSOP4: plastic, heatsink small outline package; 4 leads

SOT1224-2

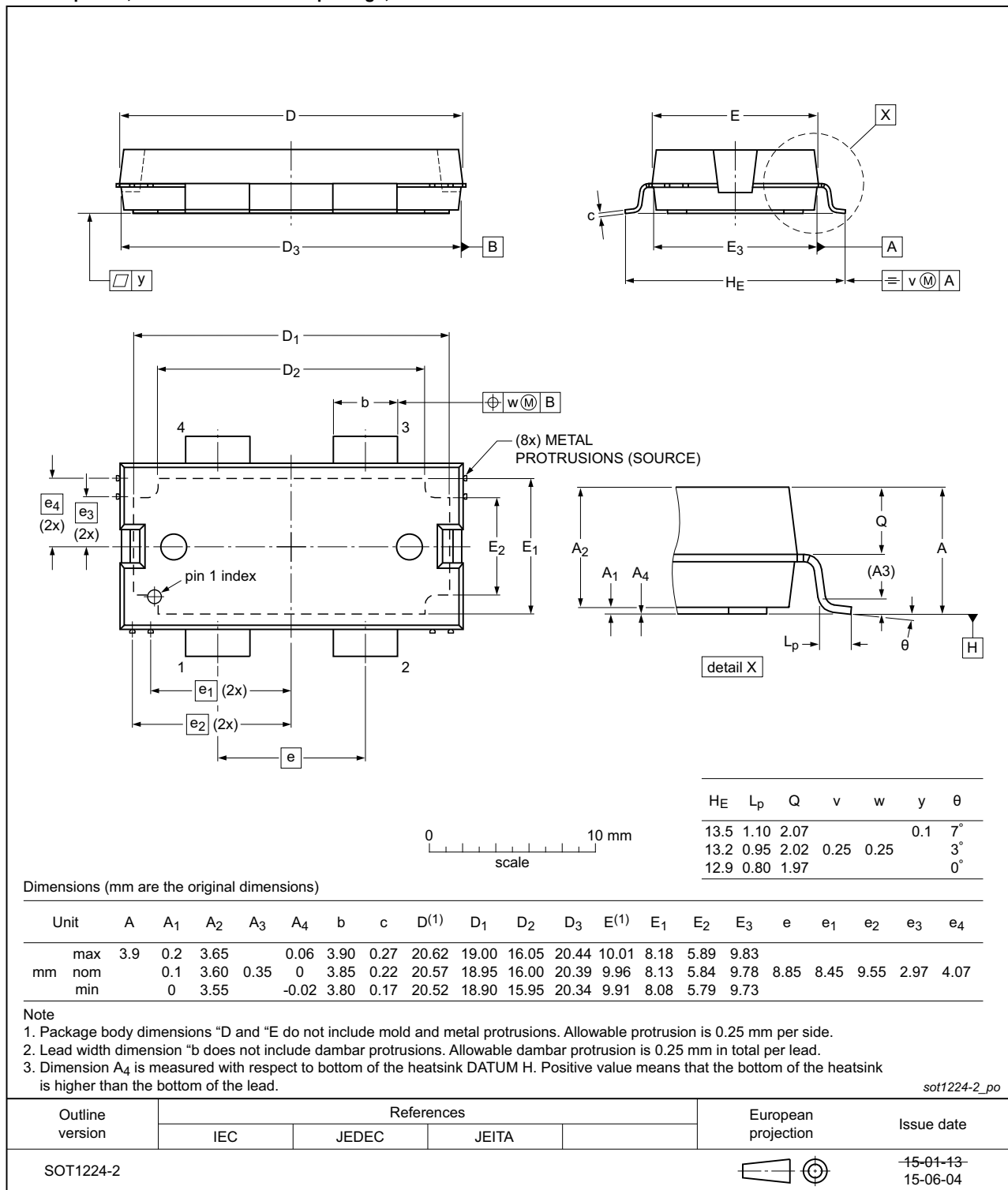


Fig 13. Package outline SOT1224-2 (HSOP4F)

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 12. Abbreviations

| Acronym | Description |
|---------|--|
| CW | Continuous Wave |
| ESD | ElectroStatic Discharge |
| HF | High Frequency |
| LDMOS | Laterally Diffused Metal-Oxide Semiconductor |
| MTF | Median Time to Failure |
| SMD | Surface Mounted Device |
| UIS | Unclamped Inductive Switching |
| VSWR | Voltage Standing-Wave Ratio |

11. Revision history

Table 13. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------------|--|----------------------|---------------|-----------------|
| BLP05H635XR_H635XRG v.4 | 20160921 | Product data sheet | - | BLP05H635XR v.3 |
| Modifications: | <ul style="list-style-type: none"> The document now describes both the straight lead and gull-wing versions of this product: BLP05H635XR and BLP05H635XRG respectively Table 2 on page 2: added BLP05H635XRG data Table 3 on page 2: added BLP05H635XRG data Section 7.1 on page 5: added BLP05H635XRG Figure 13 on page 12: added figure SOT1224-2 | | | |
| BLP05H635XR v.3 | 20160108 | Product data sheet | - | BLP05H635XR#2 |
| BLP05H635XR#2 | 20150901 | Objective data sheet | - | BLP05H635XR v.1 |
| BLP05H635XR v.1 | 20150518 | Objective data sheet | - | - |

12. Legal information

12.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
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| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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