National Semiconductor

54F/74F385
Quad Serial Adder/Subtractor

General Description

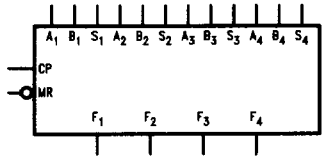
The 'F385 contains four serial adder/subtractors with common clock and clear inputs, but independent operand and mode select inputs. Each adder/subtractor contains a sum flip-flop and a carry-save flip-flop for synchronous operations. Each circuit performs either A plus B or A minus B in twos complement notation, but can also be used for magnitude-only or ones complement operation. The 'F385 is designed for use with the 'F384 and 'F784 serial multipliers in implementing digital filters or butterfly networks in fast Fourier transforms.

Features

- Four independent adder/subtractors
- Twos complement arithmetic
- Synchronous operation
- Common clear and clock
- Ones complement or magnitude-only capability

Ordering Code: See Section 5

Logic Symbols



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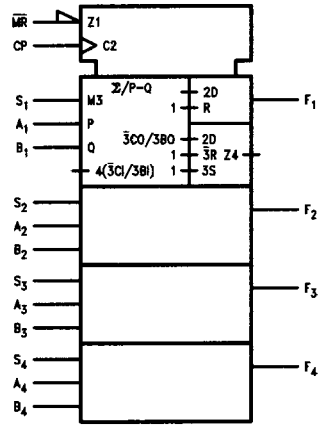
IEEE/IEC



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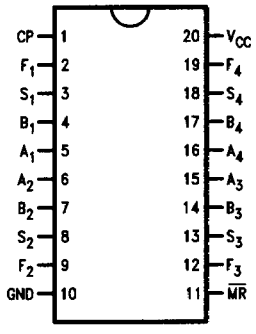
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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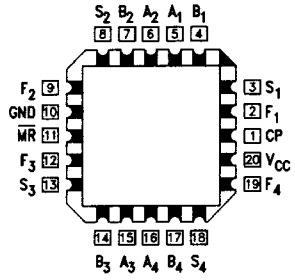
Pin Assignment for LCC



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_1–A_4	A Operand Inputs	1.0/1.0	20 μA/−0.6 mA
B_1–B_4	B Operand Inputs	1.0/1.0	20 μA/−0.6 mA
S_1–S_4	Function Select Inputs	1.0/1.0	20 μA/−0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/−0.6 mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
F_1–F_4	Sum or Difference Outputs	50/33.3	−1 mA/20 mA

Functional Description

Each adder contains two edge-triggered flip-flops to store the sum and carry, as shown in the Logic Diagram. Flip-flop state changes occur on the rising edge of the Clock Pulse (CP) input signal. The Select (S) input should be LOW for the Add (A plus B) mode and HIGH for the Subtract (A minus B) mode. A LOW signal on the asynchronous Master Reset ($\overline{MR}$) input clears the sum flip-flop and resets the carry flip-flop to zero in the Add mode or presets it to one in the Subtract mode.

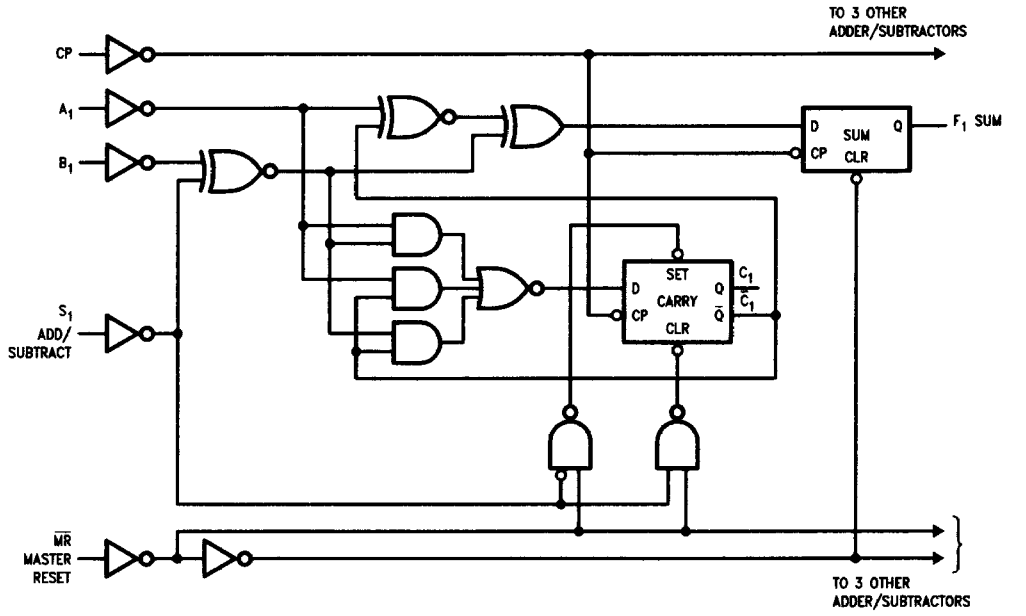
In the Subtract mode, the B operand is internally complemented. Presetting the carry flip-flop to one completes the twos complement transformation by adding one to "A plus $\overline{B}$" during the first (LSB) operation after $\overline{MR}$ is released. For ones complement subtraction, the carry flip-flop can be set to zero by making S LOW during the reset, then making S HIGH after the reset but before the next clock.

Truth Table

Inputs*				Internal Carry		Output*	Function
$\overline{MR}$	S	A	B	C	C_1	F	
L	L	X	X	L	L	L	Clear
L	H	X	X	H	H	L	
H	L	L	L	L	L	L	Add
H	L	L	L	H	L	H	
H	L	L	H	L	L	H	
H	L	L	H	H	H	L	
H	L	H	L	L	L	H	
H	L	H	L	H	H	L	
H	L	H	H	L	H	L	
H	L	H	H	H	H	H	
H	H	L	L	L	L	H	Subtract
H	H	L	L	H	H	L	
H	H	L	H	L	L	L	
H	H	L	H	H	L	H	
H	H	H	L	L	H	L	
H	H	H	L	H	H	H	
H	H	H	H	L	L	H	
H	H	H	H	H	H	L	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
* = Inputs before CP transition, output after C
C_1 = Carry flip-flop state before (C) and after (C_1) clock transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 20 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCH}	Power Supply Current			68	92*	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			68	92*	mA	Max	V_O = LOW

*95 mA for 54F

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			54F $T_A, V_{CC} = Mil$ $C_L = 50\ pF$		74F $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	70	100		65		70		MHz	2-1
t_{PLH} t_{PHL}	Propagation Delay CP to F_n	3.5 4.0	6.0 7.0	8.0 9.0	3.0 3.5	10.0 11.0	3.5 4.0	9.0 10.0	ns	2-3
t_{PHL}	Propagation Delay $\overline{MR}$ to F_n	5.5	9.0	12.0	5.0	14.0	5.5	13.0	ns	2-3

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} = Mil$		74F $T_A, V_{CC} = Com$		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n to CP	15.0 15.0		17.5 17.5		15.0 15.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n to CP	0 0		0 0		0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW B_n or S_n to CP	15.0 15.0		17.5 17.5		15.0 15.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW B_n or S_n to CP	0 0		0 0		0 0			
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	6.0 6.0		7.0 7.0		6.0 6.0		ns	2-4
$t_w(L)$	$\overline{MR}$ Width, LOW	6.0		6.5		6.0		ns	2-4
t_{rec}	Recovery Time, $\overline{MR}$ to CP	8.5		10.0		9.5		ns	2-6