MC1066

ACPI–Compliant SMBus Temperature Sensor with Internal and External Diode Input

The MC1066 is a serially programmable temperature sensor optimized for monitoring modern high performance CPUs with on–board integrated temperature sensing diodes. Temperature data is converted from the CPU's diode outputs and made available as an 8–bit digital word.

Communication with the MC1066 is accomplished via the standard System Management Bus (SMBus) commonly used in modern computer systems. This permits reading the current internal/external temperature, programming the threshold setpoints, and configuring the device. Additionally, an interrupt is generated on the ALERT/COMP pin when temperature moves outside the preset threshold windows in either direction. A separate CRITICAL setpoint is provided through external hardwiring for "fail safe" operation per ACPI guidelines.

A Standby command may be sent via the SMBus or by signaling the STBY input pin to activate the low–power Standby mode. Registers can be accessed while in Standby mode. Address selection inputs allow up to nine MC1066s to share the same 2–wire SMBus for multi–zone monitoring.

All registers can be read by the host, and both polled and interrupt driven systems are easily accommodated. Small size, low installed cost, and ease of use make the MC1066 an ideal choice for implementing sophisticated system management schemes, such as ACPI.

Features

- Specifically ACPI–Compliant
- Backward Compliant to Older APM Systems
- Includes Internal *and* External Sensing Capability
- Outputs Temperature As 8–Bit Digital Word
- Solid State Temperature Sensing; 1°C Resolution
- 3.0–5.5 V Operating Range
- Independent Internal and External Threshold Set–Points With ALERT/COMP Interrupt Output
- SMBus 2–Wire Serial Interface
- Optional CRITICAL Set–Point for Full ACPI Compliant Implementation
- Up To Nine MC1066s May Share the Same Bus
- Low Standby Power Mode
- Low Power: 70 μA (max) Operating, 10 μA (max) Standby Mode
- 16–Pin Plastic QSOP Package

Typical Applications

- Thermal Protection For Intel "Deschutes" Pentium™ II and Other High Performance CPUs with Integrated On–Board Diode - No Sensor Mounting Problems!
- Accurate Temperature Sensing From Any Silicon Junction Diode
- Thermal Management in Electronic Systems: Computers, Network Equipment, Power Supplies

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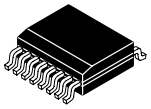
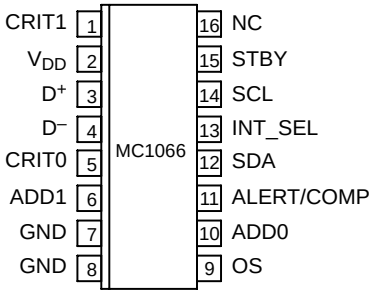


16–Pin QSOP
DB SUFFIX
CASE TBD
PRELIMINARY INFORMATION

PIN CONFIGURATION

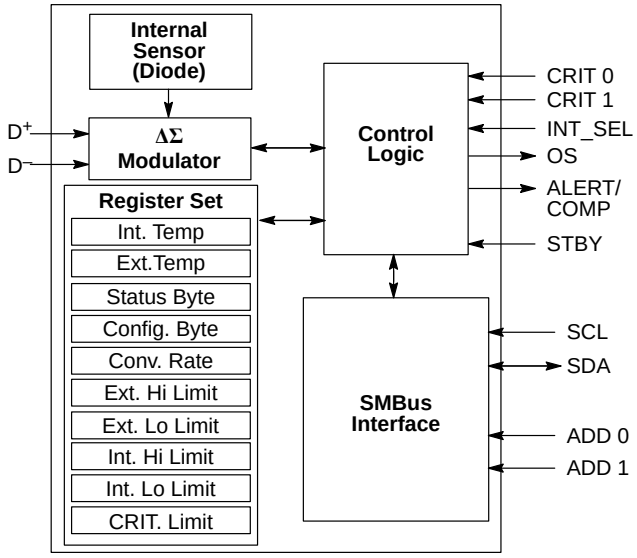


(Top View)

ORDERING INFORMATION

Device	Package	Shipping
MC1066DBR2	16–Pin QSOP	2500 Tape/Reel

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Type	Description
2	V_{DD}	Power	Power Supply Input
3	D^+	Bi–Directional	Current Source and A/D Positive Input
4	D^-	Bi–Directional	Current Sink and A/D Negative Input
6, 10	ADD[1:0]	Input	Address Select Pins (See Address Decode Table)
7, 8	GND	Power	System Ground
11	ALERT/COMP	Output	SMBus Interrupt (SMBALERT) or Comparator Output
12	SDA	Bi–Directional	SMBus Serial Data
14	SCL	Input	SMBus Serial Clock
15	STBY	Input	Standby Enable
1, 5	CRIT[1:0]	Input	CRITICAL Setpoint Bits (See CRITICAL Setpoint Decode Table)
9	OS	Output	Open Collector, Low–True “Over–Temperature” Warning Output
13	INT_SEL	Input	Selects ALERT or COMP Output on Pin 11
16	NC	–	Not Connected

PIN DESCRIPTION

SCL

Input. SMBus serial clock. Clocks data into and out of the MC1066.

SDA

Bidirectional. Serial data is transferred on the SMBus in both directions using this pin.

ADD1, ADD0

Inputs. Sets the 7–bit SMBus address. These pins are “tri–state,” and the SMBus addresses are specified in the Address Decode Table.

(**NOTE:** The tri–state scheme allows up to nine MC1066s on a single bus. A match between the MC1066’s address and the address specified in the serial bit stream must be made to initiate communication. Many SMBus–compatible devices with other addresses may share the same 2–wire bus. These pins are only active at power–on reset, and will latch into the appropriate states.

ALERT/COMP*

Output, Open Collector, Active Low. The ALERT output corresponds to the general SMBALERT signal and indicates an interrupt event. The MC1066 will respond to the standard SMBus Alert Response Address when ALERT is asserted. Normally, the ALERT output will be asserted and latched when any of the following occurs:

1. INT_TEMP equal to or exceeds INT_HLIM
2. INT_TEMP below INT_LLIM
3. EXT_TEMP equal to or exceeds EXT_HLIM
4. EXT_TEMP below EXT_LLIM
5. External Diode “Open”

The operation of the ALERT output is controlled by the MASK1 bit in the CONFIG register. If the MASK1 bit is set to “1,” no interrupts will be generated on ALERT. The ALERT output is cleared and re–armed by the Alert Response Address (ARA). This output may be WIRE–ORed with similar outputs from other SMBus devices. If the alarm condition persists after the ARA, the ALERT output will be immediately re–asserted.

(**NOTE:** A pull–up resistor is necessary on ALERT since it is an open–drain output. Current sourced from the pull–up resistor causes power dissipation and may cause internal heating of the MC1066. To avoid affecting the accuracy of internal temperature readings, the pull–up resistors should be made as large as possible.)

Normally the COMP output will be asserted upon the following events:

1. EXT_TEMP equal to or exceeds EXT_HLIM
2. External Diode “Open”

COMP will be de–asserted upon the following event: EXT_TEMP below EXT_HLIM.

The operation of the COMP output is controlled by the MASK1 bit in the CONFIG register. If the MASK1 bit is set to “1,” no interrupts will be generated on COMP. This output may be WIRE–ORed with similar outputs from other SMBus devices. Note: A pull–up resistor is necessary on COMP since it is an open–drain output. Current sourced from the pull–up resistor causes power dissipation and may cause internal heating of the MC1066. To avoid affecting the accuracy of internal temperature readings, the pull–up resistors should be made as large as possible.

INT_SEL

Input. The operation of Pin 11 is defined by the state of this pin. There is an internal pull–up to V_{DD}. If INT_SEL is high, Pin 11 will function as ALERT. If INT_SEL is grounded, Pin 11 will function as COMP.

STBY

Input. The activation of Standby mode may be achieved using either the STBY pin or the CHIP STOP bit (CONFIG register). If STBY is pulled low, the MC1066 unconditionally enters its low–power Standby mode (I_{DD} = 10 μA, max). The temperature–to–digital conversion process is halted, but ALERT and OS remain functional. The MC1066’s bus interface remains active, and all registers may be read from and written to normally. The INT_TEMP and EXT_TEMP registers will contain whatever data was valid at the time of Standby. (Transitions on SDA or SCL due to external bus activity may increase the Standby power consumption.)

CRIT [1:0]

Inputs. These digital pins determine the temperature threshold for the CRITICAL setpoint when the 1066 is first powered up. They must be tied either to Ground or to V_{DD}, or they must be left floating. See the CRITICAL setpoint decode table for details.

OS

Output. Open Collector, low–true digital output which asserts when *either* INT_TEMP or EXT_TEMP trips the CRITICAL setpoint. This interrupt *cannot be masked.*

D^+

Bi–directional. This pin connects to the anode of the external diode and is the positive A/D input. Current is injected into the external diode from the MC1066, and the temperature proportional V_{BE} is measured and converted to digital temperature data.

D^-

Bi–directional. This pin connects to the cathode of the external diode. Current is sunk from the external diode into the MC1066 through this pin. It also is the negative input terminal to the MC1066’s A/D converter. This node is kept at approximately 0.7V above GROUND.

V_{DD}

Input. Power supply input. See electrical specifications.

GND

Input. Ground return for all MC1066 functions.

ABSOLUTE MAXIMUM RATINGS*

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	6.0	V
Voltage on Any Pin (GND to V_{DD})		(GND – 0.3 V) to (V_{DD} + 0.3 V)	V
Operating Temperature Range	T_A	–55 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
SMBus Input/Output Current		–1.0 to +50	mA
D^- Input Current		±1.0	mA
Maximum Power Dissipation	P_D	330	mW

* Maximum Ratings are those values beyond which damage to the device may occur.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3 V, –55°C ≤ T_A ≤ 125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply					
Power Supply Voltage	V_{DD}	3.0	–	5.5	V
V_{DD} Undervoltage Lockout Threshold	$V_{UV–LOCK}$	2.4	2.80	2.95	V
Power–On Reset Threshold (V_{DD} Falling Edge)	V_{POR}	1.0	1.7	2.3	V
Operating Current 0.25 Conv./Sec Rate SMBus Inactive (1)	I_{DD}	–	–	70	μA
Operating Current 2 Conv./Sec Rate SMBus Inactive (1)	I_{DD}	–	–	180	μA
Standby Supply Current (SMBus Active)	$I_{DD–STANDBY}$	–	–	100	μA
Standby Supply Current (SMBus Inactive)	$I_{DD–STANDBY}$	–	–	10	μA
CRIT[1:0] Bias Current (Power–Up Only)	$I_{CRIT–BIAS}$	–	160	–	μA
ADD[1:0] Bias Current (Power–Up Only)	$I_{ADD–BIAS}$	–	160	–	μA
ALERT/COMP Output					
Output Low Voltage I_{OL} = 1.0 mA (3)	V_{OL}	–	–	0.4	V
OS Output					
Output Low Voltage I_{OL} = 1.0 mA (3)	V_{OL}	–	–	0.4	V
ADD[1:0], CRIT [1:0] Inputs					
Logic Input Low	V_{IL}	–	–	V_{DD} x 0.3	V
Logic Input High	V_{IH}	V_{DD} x 0.7	–	–	V
STBY Input					
Logic Input Low	V_{IL}	–	–	V_{DD} x 0.3	V
Logic Input High	V_{IH}	V_{DD} x 0.7	–	–	V
INT_SEL					
Logic Input Low	V_{IL}	–	–	V_{DD} x 0.3	V
Logic Input High	V_{IH}	V_{DD} x 0.7	–	–	V
Internal Pull–Up Resistance	R_P	–	500	–	kΩ
Temp–to–Bits Converter					
Basic Temperature Resolution	T_{RES}	–	1.0	–	°C
Internal Diode Temperature +60°C ≤ T_A ≤ +100°C 0°C ≤ T_A ≤ +125°C –55°C ≤ T_A ≤ 0°C	T_{IERR}	 –2.0 –3.0 –	 – – ±3.0	 +2.0 +3.0 –	°C

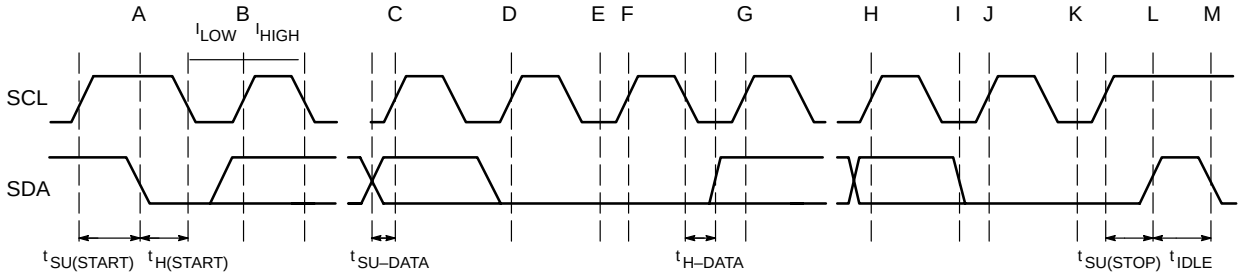
Characteristic	Symbol	Min	Typ	Max	Unit
Temp–to–Bits Converter					
External Diode Temperature +60°C ≤ T_A ≤ +100°C 0°C ≤ T_A ≤ +125°C –55°C ≤ T_A ≤ 0°C	T_{EERR}	 –3.0 –5.0 –	 – – ±5.0	 +3.0 +5.0 –	°C
External Diode High Source Current (D^+) – (D^-) ~ 0.65 V	$I_{DIODE–HIGH}$	–	100	–	μA
External Diode Low Source Current (D^+) – (D^-) ~ 0.65 V	$I_{DIODE–LOW}$	–	10	–	μA
D^- Source Voltage	$V_{D–SOURCE}$	–	0.7	–	V
Conversion Time From CHIP STOP to Conv. Complete (2)	t_{CONV}	54	83	112	msec
Conversion Rate Accuracy (See Conversion Rate Register Desc.)	ΔCR	–35	–	+35	%
2–Wire SMBus Interface					
Logic Input High	V_{IH}	2.2	–	–	V
Logic Input Low	V_{IL}	–	–	0.8	V
SDA Output Low I_{OL} = 2 mA (3) I_{OL} = 4 mA (3)	V_{OL}	 – –	 – –	 0.4 0.6	V
Input Capacitance SDA, SCL	C_{IN}	–	5.0	–	pF
I/O Leakage	I_{LEAK}	–1.0	0.1	1.0	μA

1. Operating current is an average value (including external diode injection pulse current) integrated over multiple conversion cycles. Transient current may exceed this specification.
2. For true recurring conversion time see Conversion Rate register description.
3. Output current should be minimized for best temperature accuracy. Power dissipation within the MC1066 will cause self–heating and temperature drift error.

SMBus PORT AC TIMING (V_{DD} = 3.3 V, –55°C ≤ (T_A = T_J) ≤ 125°C; C_L = 80 pF, unless otherwise noted.)

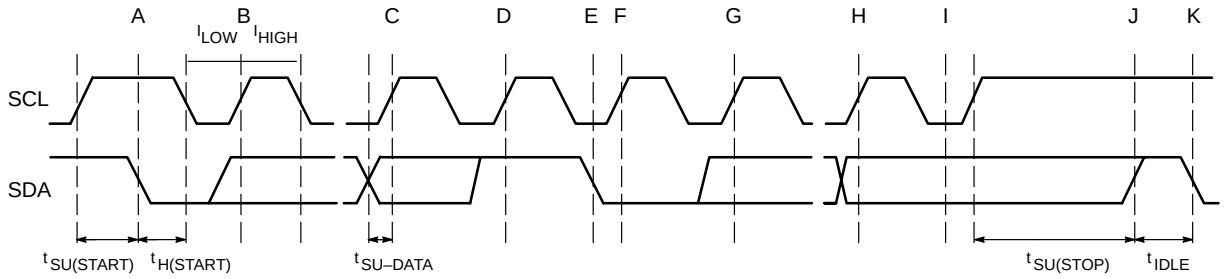
Characteristic	Symbol	Min	Typ	Max	Unit
SMBus Clock Frequency	f_{SMB}	10	–	100	kHz
Low Clock Period (10% to 10%)	t_{LOW}	4.7	–	–	μsec
High Clock Period (90% to 90%)	t_{HIGH}	4.0	–	–	μsec
SMBus Rise Time (10% to 90%)	t_R	–	–	1,000	nsec
SMBus Fall Time (90% to 10%)	t_F	–	–	300	nsec
Start Condition Setup Time (90% SCL to 10% SDA) (for Repeated Start Condition)	$t_{SU(START)}$	4.0	–	–	μsec
Start Condition Hold Time	$t_{H(START)}$	4.0	–	–	μsec
Data in Setup Time	$t_{SU–DATA}$	1,000	–	–	nsec
Data in Hold Time	$t_{H–DATA}$	1,250	–	–	nsec
Stop Condition Setup Time	$t_{SU(STOP)}$	4.0	–	–	μsec
Bus Free Time Prior to New Transition	t_{IDLE}	4.7	–	–	μsec

SMBUS Write Timing Diagram



A = Start Condition
B = MSB of Address Clocked into Slave
C = LSB of Address Clocked into Slave
D = R/$\overline{W}$ Bit Clocked into Slave
E = Slave Pulls SDA Line Low
F = Acknowledge Bit Clocked into Master
G = MSB of Data Clocked into Slave
H = LSB of Data Clocked into Slave
I = Slave Pulls SDA Line Low
J = Acknowledge Clocked into Master
K = Acknowledge Clock Pulse
L = Stop Condition, Data Executed by Slave
M = New Start Condition

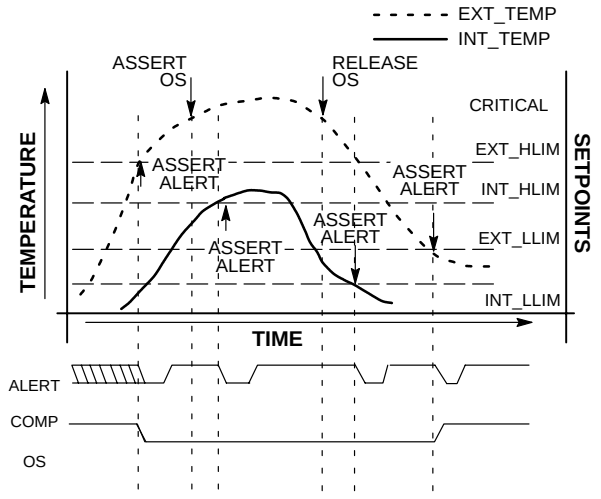
SMBUS Read Timing Diagram



A = Start Condition
B = MSB of Address Clocked into Slave
C = LSB of Address Clocked into Slave
D = R/$\overline{W}$ Bit Clocked into Slave
E = Slave Pulls SDA Line Low
F = Acknowledge Bit Clocked into Master
G = MSB of Data Clocked into Master
H = LSB of Data Clocked into Master
I = Acknowledge Clock Pulse
J = Stop Condition
K = New Start Condition

DETAILED OPERATING DESCRIPTION

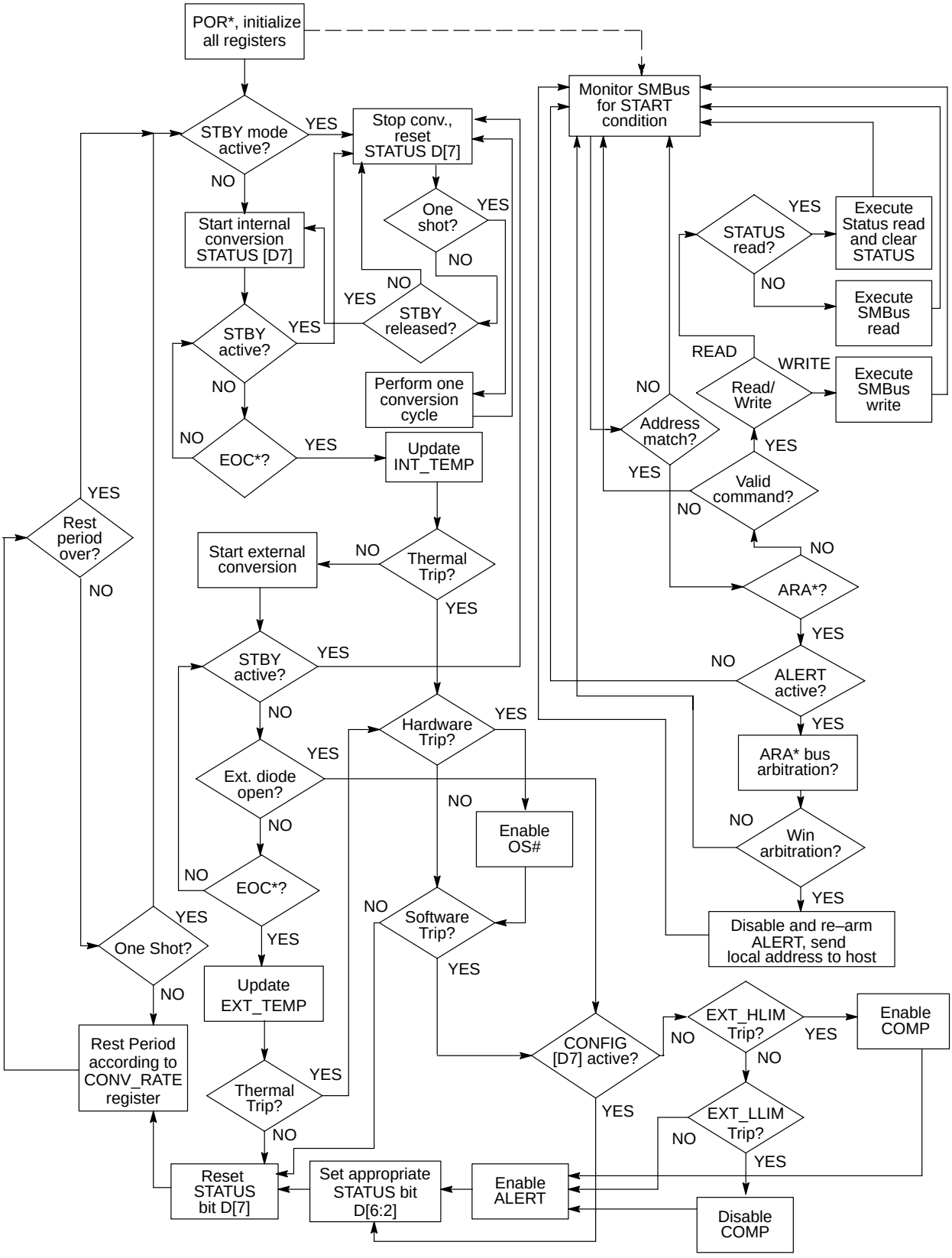
The MC1066 acquires and converts temperature information from two separate sources, both silicon junction diodes, with a basic accuracy of ±1°C. One is located on the MC1066 die; the other is connected externally. This external diode may be located on another IC die. The analog–to–digital converter on the MC1066 alternately converts temperature data from the two sensors and stores them separately in internal registers.



Note: This diagram implies that the appropriate setpoint is moved, temporarily, after each ALERT event to suppress re–assertion of ALERT immediately after the ARA/de–assertion.

Figure 1. Temperature vs. Setpoint Event Generation

The system interface is a slave SMBus port with an ALERT (SMBALERT) and COMP interrupt outputs. The ALERT interrupt is triggered when one or more of four preset temperature thresholds are tripped (see Figure 1). These four thresholds are user–programmable via the SMBus port. The COMP interrupt is triggered when EXT_TEMP equals or exceeds EXT_HLIM. Also, there is a fifth independent, hardware programmable threshold (CRITICAL) that trips its own interrupt (OS) for an unconditional warning. Additionally, the temperature data can be read at any time through the SMBus port. Nine SMBus addresses are programmable for the MC1066, which allows for a multi–sensor configuration. Also, there is low–power Standby mode where temperature acquisition is suspended.



* POR = Power On Reset; ARA = Alert Response Address; EOC = End Of Conversion

Figure 2. MC1066 Functional Description Flowchart

STANDBY MODE

The MC1066 allows the host to put it into a low power (I_{DD} = 10 μA, max) Standby mode. In this mode, the A/D converter is halted, and the temperature data registers are frozen. The SMBus port operates normally. Standby mode can be enabled with either the STBY input pin or the CHIP STOP bit in the CONFIG register. The following table summarizes this operation.

Standby Mode Operation

STBY	Chip Stop Bit	One Shot?	Operating Mode
0	Don't Care	Don't Care	Standby
1	0	Don't Care	Normal
1	1	No	Standby
1	1	Yes	Normal (1 Conversion Only, then Standby)

SMBus SLAVE ADDRESS

The two pins ADD1 and ADD0 are tri–state input pins which determine the 7–bit SMBus slave address of the MC1066. The address is latched during POR. The allowable addresses are summarized in the table below.

Address Decode Table

ADD0	ADD1	SMBus Address
0	0	0011 000
0	open (3–state)	0011 001
0	1	0011 010
open (3–state)	0	0101 001
open (3–state)	open (3–state)	0101 010
open (3–state)	1	0101 011
1	0	1001 100
1	open (3–state)	1001 101
1	1	1001 110

SERIAL PORT OPERATION

The Serial Clock input (SCL) and bi–directional data port (SDA) form a 2–wire bi–directional serial port for programming and interrogating the MC1066. The following conventions are used in the bus architecture in the following table. (See SMBus Write/Read Timing Diagram.)

All transfers take place under control of a host, usually a CPU or microcontroller, acting as the Master, which provides the clock signal for all transfers. The MC1066 *always* operates as a slave. The serial protocol is illustrated in Figure 3. All data transfers have two phases; all bytes are transferred MSB first. Accesses are initiated by a start condition (START), followed by a device address byte and one or more data bytes. The device address byte includes a Read/Write selection bit. Each access must be terminated by a Stop Condition (STOP). A convention called *Acknowledge* (ACK) confirms receipt of each byte. Note that SDA can change only during periods when SCL is LOW (SDA changes while SCL is High are reserved for Start and Stop conditions.)

MC1066 Serial Bus Conventions

Term	Explanation
Transmitter	The device sending data to the bus.
Receiver	The device receiving data from the bus.
Master	The device which controls the bus: initiating transfers (START), generating the clock, and terminating transfers (STOP).
Slave	The device addressed by the master.
Start	A unique condition signaling the beginning of a transfer indicated by SDA falling (High – Low) while SCL is high.
Stop	A unique condition signaling the end of a transfer indicated by SDA rising (Low – High) while SCL is high.
ACK	A receiver acknowledges the receipt of each byte with this unique condition. The receiver drives SDA low during SCL high of the ACK clock–pulse. The Master provides the clock pulse for the ACK cycle.
Busy	Communication is not possible because the bus is in use.
NOT Busy	When the bus is idle, both SDA and SCL will remain high.
Data Valid	The state of SDA must remain stable during the High period of SCL in order for a data bit to be considered valid. SDA only changes state while SCL is low during normal data transfers (see Start and Stop conditions).

Start Condition (START)

The MC1066 continuously monitors the SDA and SCL lines for a start condition (a High to Low transition of SDA while SCL is High), and will not respond until this condition is met. (See SMBus Write/Read Timing Diagram.)

Address Byte

Immediately following the Start Condition, the host must transmit the address byte to the MC1066. The states of ADD1 and ADD0 during power–up determine the 7–bit SMBus address for the MC1066. The 7–bit address transmitted in the serial bit stream must match for the MC1066 to respond with an Acknowledge (indicating the MC1066 is on the bus and ready to accept data). The eighth bit in the Address Byte is a Read–Write Bit. This bit is 1 for a read operation or 0 for a write operation.

Write Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	DATA	ACK	P
	7 Bits			8 Bits		8 Bits		

Slave Address

Command Byte: selects which register you writing to.

Data Byte: data goes into the register set by the command byte.

Read Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	S	ADDRESS	RD	ACK	DATA	NACK	P
	7 Bits			8 Bits			7 Bits			8 Bits		

Slave Address

Command Byte: selects which register you reading from.

Slave Address: repeated due to change in data–flow direction.

Data Byte: reads from the register set by the command byte.

Send Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	P
	7 Bits			8 Bits		

Command Byte: sends command with no data, usually used for one–shot command.

Receive Byte Format

S	ADDRESS	RD	ACK	DATA	NACK	P
	7 Bits			8 Bits		

Data Byte: reads data from the register commanded by the last Read Byte.

S = Start Condition
P = Stop Condition
Shaded = Slave Transmission

Figure 3. SMBus Protocols

Acknowledge (ACK)

Acknowledge (ACK) provides a positive handshake between the host and the MC1066. The host releases SDA after transmitting eight bits, then generates a ninth clock cycle to allow the MC1066 to pull the SDA line Low to acknowledge that it successfully received the previous eight bits of data or address.

Data Byte

After a successful ACK of the address byte, the host must transmit the data byte to be written or clock out the data to be read. (See the appropriate timing diagrams.) ACK will be generated after a successful write of a data byte into the MC1066.

Stop Condition (STOP)

Communications must be terminated by a stop condition (a Low to High transition of SDA while SCL is High). The Stop Condition must be communicated by the transmitter to the MC1066. (See SMBus Write/Read Timing Diagram.)

Command Byte Description

Command	Code	Function
RIT	00h	Read Internal Temp (INT_TEMP)
RET	01h	Read External Temp (EXT_TEMP)
RS	02h	Read Status Byte (STATUS)
RC	03h	Read Configuration Byte (CONFIG)
RCR	04h	Read Conversion Rate Byte (CONV_RATE)
RIHL	05h	Read Internal High Limit (INT_HLIM)
RILL	06h	Read Internal Low Limit (INT_LLIM)
REHL	07h	Read External High Limit (EXT_HLIM)
RELL	08h	Read External Low Limit (EXT_LLIM)
WC	09h	Write Configuration Byte (CONFIG)
WCR	0Ah	Write Conversion Rate Byt3 (CONV_RATE)
WIHL	0Bh	Write Internal High Limit (INT_HLIM)
WILL	0Ch	Write Internal Low Limit (INT_LLIM)
WEHL	0Dh	Write External High Limit (EXT_HLIM)
WELL	0Eh	Write External Low Limit (EXT_LLIM)
OSHT	0Fh	One Shot Temp Measurement
RMID	FEh	Read Manufacturer ID (MFR_ID)
RMREV	FFh	Read Manufacturer Revision Number (MFR_REV)

NOTE: Proper device operation is NOT guaranteed if undefined locations (10h to FDh) are addressed. In case of erroneous SMBus operation (RECEIVE_BYTE command issued immediately after WRITE_BYTE command) the MC1066 will ACKnowledge the address and return 1111 1111b to signify an error. Under no condition will it implement an SMBus “timeout.”

REGISTER SET AND PROGRAMMER'S MODEL

MC1066 Command Set

The MC1066 supports four SMBus command protocols. These are READ_BYTE, WRITE_BYTE, SEND_BYTE, and RECEIVE_BYTE. See System Management Bus Specification Rev. 1.0 for details.

Configuration Register (Config), 8–Bits, Read/Write

Configuration Register (Config)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Mask1	Chip Stop	Reserved					

Bit	POR State	Function	Operation
D[7]	0	Interrupt Mask (see text)	1 = mask ALERT/ COMP 0 = don't mask ALERT/COMP
D[6]	0	Standby switch	1 = standby, 0 = normal
D[5]–D[0]	0	Reserved – Always returns zero when read.	N/A

A/D Conversion Rate Register (CONV_RATE), 8–Bits, Read/Write

A/D Conversion Rate Register (CONV_RATE)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Reserved					MSB	X	LSB

Bit	POR State	Function	Operation
D[7:3]	0	Reserved – Always returns zero when read.	N/A
D[2:0]	010b	Conversion rate bits.	See below.

A/D Conversion Rate Selection

D2	D1	D0	Conversion Rate Samples/sec
0	0	0	0.0625
0	0	1	0.125
0	1	0	0.25
0	1	1	0.5
1	0	0	1.0
1	0	1	2.0
1	1	0	4.0
1	1	1	8.0

NOTE: Conversion rate denotes actual sampling of both internal *and* external sensors.

Temperature Registers, 8–Bits, Read–Only (INT_TEMP, EXT_TEMP)

The binary value (2's complement format) in these two registers represents temperature of the internal and external sensors following a conversion cycle. The registers are automatically updated in an alternating manner.

Internal Temperature Register (INT_TEMP)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	x	x	x	x	x	x	LSB

External Temperature Register (EXT_TEMP)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	x	x	x	x	x	x	LSB

Temperature Threshold Setpoint Registers, 8–Bits, Read–Write (INT_HLIM, INT_LLIM, EXT_HLIM, EXT_LLIM)

These registers store the values of the upper and lower temperature setpoints for event detection. The value is in 2's–complement binary. INT_HLIM and INT_LLIM are compared with the INT_TEMP value, and EXT_HLIM and EXT_LLIM are compared with EXT_TEMP. These registers may be written at any time.

Internal High Limit Setpoint Register (INT_HLIM)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	x	x	x	x	x	x	LSB

Internal Low Limit Setpoint Register (INT_LLIM)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	x	x	x	x	x	x	LS

External High Limit Setpoint Register (EXT_HLIM)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	x	x	x	x	x	x	LSB

External Low Limit Setpoint Register (EXT_LLIM)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	x	x	x	x	x	x	LSB

NOTE: POR states:

INT_HLIM	01111111b	+127°C
INT_LLIM	11001001b	–55°C
EXT_HLIM	01111111b	+127°C
EXT_LLIM	11001001b	–55°C

Critical Setpoint Register, 8–Bits (Reserved)

This register stores the value of the CRITICAL setpoint. It is not accessible through the SMBus port and only can be set with the CRIT[1:0] pins. The value in this register determines the OS event threshold.

Critical Limit Setpoint Register (Critical)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	x	x	x	x	x	x	LSB

Critical Setpoint Decode Table

CRIT1	CRIT0	Binary	Critical Setpoint°C
0	0	01010101	85
0	open	01011010	90
0	1	01011111	95
open	0	01100100	100
open	open	01101001	105
open	1	01101110	110
1	0	01110011	115
1	open	01111000	120
1	1	01111101	125

In the two temperature data and four threshold setpoint registers, each unit value represents one degree (Celsius). The value is in 2's–complement binary format such that a reading of 00000000b corresponds to 0°C. Examples of this temperature–to–binary value relationship are shown in the following table.

Temperature–to–Digital Value Conversion (INT_TEMP, EXT_TEMP, INT_HLIM, INT_LLIM,EXT_HLIM, EXT_LLIM)

Actual Temperature	Rounded Temperature	Binary Value	Hex Value
+130.00°C	+127°C	01111111	7F
+127.00°C	+127°C	01111111	7F
+126.50°C	+127°C	01111111	7F
+25.25°C	+25°C	00011001	19
+0.50°C	+1°C	00000001	01
+0.25°C	0°C	00000000	00
0.00°C	0°C	00000000	00
–0.25°C	0°C	00000000	00
–0.50°C	0°C	00000000	00
–0.75°C	–1°C	11111111	FF
–1.00°C	–1°C	11111111	FF
–25.00°C	–25°C	11100111	E7
–25.25°C	–25°C	11100110	E7
–54.75°C	–55°C	11001001	C9
–55.00°C	–55°C	11001001	C9
–65.00°C	–65°C	10111111	BF

Status Register (Status)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Busy	Flag1	Flag2	Flag3	Flag4	Flag5	Flag6	Re-served

Bit(s)	POR State	Function	Operation*
D[7]	0	Signal A/D converter is busy.	1 = A/D busy, 0 = A/D idle
D[6]	0	Interrupt flag for INT_HLIM event	1 = interrupt occurred, 0 = none
D[5]	0	Interrupt flag for INT_LLIM event	1 = interrupt occurred, 0 = none
D[4]	0	Interrupt flag for EXT_HLIM event	1 = interrupt occurred, 0 = none
D[3]	0	Interrupt flag for EXT_LLIM event	1 = interrupt occurred, 0 = none
D[2]	0	External diode "fault" flag	1 = external diode fault 0 = external diode OK
D[1:0]	0	Reserved – Always returns zero.	N/A

NOTE: All status bits are cleared after a read operation is performed on STATUS. The EXT_TEMP register will read +127°C if an external diode "open" is detected.

Manufacturer's Identification Register (MFR_ID), 8–Bits, Read Only:

Manufacturer's Identification Register (MFR_ID)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	X	X	X	X	X	X	LSB

Manufacturer's Revision Register (MFR_REV), 8–Bits, Read Only:

Manufacturer's Revision Register (MFR_REV)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	X	X	X	X	X	X	LSB

Register Set Summary:

The MC1066's register set is summarized in the following table. All registers are 8–bits wide.

Name	Description	POR State	Read	Write
INT_TEMP	Internal sensor temperature (2's complement)	0000 0000b*	√	
EXT_TEMP	External sensor temperature (2's complement)	0000 0000b*	√	
STATUS	STATUS register	0000 0000b	√	
CONFIG	CONFIG register	0000 0000b	√	√
CONV_RATE	A/D conversion rate register	0000 0010b	√	√
INT_HLIM	Internal high limit (2's complement)	0111 1111b	√	√
INT_LLIM	Internal low limit (2's complement)	1100 1001b	√	√
EXT_HLIM	External high limit (2's complement)	0111 1111b	√	√
EXT_LLIM	External low limit (2's complement)	1100 1001b	√	√
MFR_ID	ASCII for letter "T" (TelCom)	0101 0100b	√	
MFR_REV	Serial device revision #	**	√	
CRITICAL	CRITICAL limit (2's complement)	N/A		√***

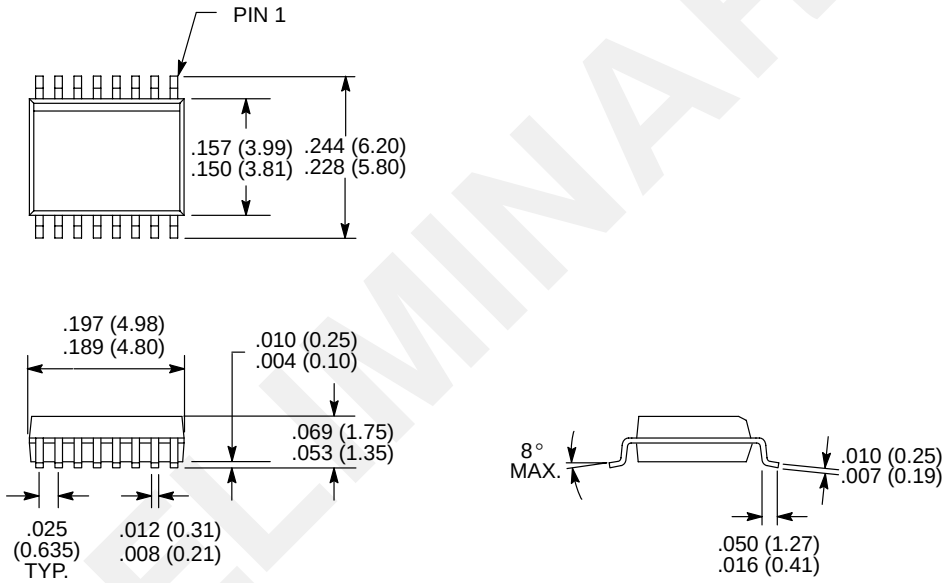
***NOTE:** The INT_TEMP and EXT_TEMP register immediately will be updated by the A/D converter after POR. If STBY is low at power–up, INT_TEMP and EXT_TEMP will remain in POR state (0000 0000b).

**MFR_REV will sequence 01h, 02h, 03h, etc. by mask changes.

***CRITICAL only can be written via the CRIT[1:0] pins. It cannot be accessed through the SMBus port.

PACKAGE DIMENSIONS

16–Pin QSOP
PLASTIC PACKAGE
CASE TBD
ISSUE TBD



Dimensions: inches (mm)

Notes

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