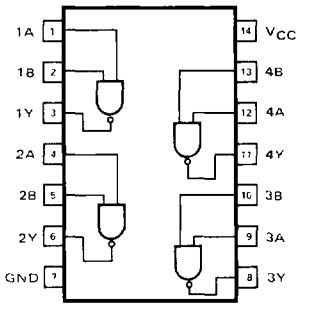
QUAD 2-INPUT NAND GATE W/OPEN COLLECTOR OUTPUTS — 54/7403

SPEED/PACKAGE AVAILABILITY

54	F	74	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

PIN CONFIGURATION

A,F,W PACKAGE



Positive logic: $Y = \overline{AB}$

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		35	45		17	32	2	5 (C_L=50pF)	7.5	ns
								7.5		
t_{PHL} High-to-low		8	15		15	28	2	4.5 (C_L=50pF)	7	ns
								7		

Load circuit and typical waveforms are shown at the front of section.

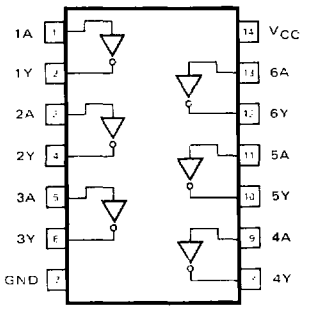
HEX INVERTER — 54/7404

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

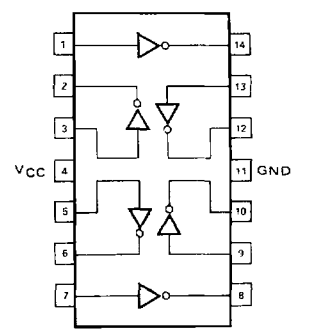
PIN CONFIGURATION

74,74H, 54/74LS,54S
A,F,W PACKAGE



Positive logic: $Y = \overline{A}$

54,54H
W PACKAGE



SWITCHING CHARACTERISTICS V_{CC}= 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		12	22		6	10		5	15	2	3 (C_L=50pF) 4.5	4.5	ns
t_{PHL} High-to-low		8	15		6.5	10		9	15	2	3 (C_L=50pF) 5	5	ns

Load circuit and typical waveforms are shown at the front of section.

LOGIC